Pinning Fault Mode Modeling for DWM Shifting

Kawsher Roxy, Stephen Longofono, Sebastien Olliver, Sanjukta Bhanja, and Alex K. Jones

***Abstract*—Extreme scaling for purposes of achieving higher density and lower energy continues to increase the probability of memory faults. For domain wall (DW) memories, misalignment faults arise when aligning domains with access points. A previously understudied type of shifting fault, a *pinning fault* may occur due to non-uniform pinning potential distribution caused by notches with fabrication imperfections. This non-uniformity can pin a wall during current-induced DW motion. This brief provides a model of geometric variations varying width, depth, and curvature variations of a notch, their impacts on the critical shift current, and a study of the resulting impact on fault rates of DW memory systems. An increase in the effective critical shift current due to 5% variation predicts a pinning fault rate on the order of 10^{-8} per shift. This results in a mean-time-to-failure (MTTF) of circa 2s for a DW memory system and requires multi-bit error correction for achieving reasonable system lifetimes.**

***Index Terms*—Domain wall memories, spintronic memories, fault-modeling, pinning, process variation.**

I. Introduction

DOMAIN wall memories (DWMs) are formed from ferromagnetic nanowires. These nanowires extend the free layer of the magnetic tunnel junction (MTJ) used to form spin-transfer-torque magnetic random access memories (STT-MRAM). Each DWM nanowire may store multiple data-bits, e.g., 32-512 bits, separated by fabricated notches to form magnetic domains. Domains store these bit values through magnetic polarization. Between adjacent domains storing complimentary bits, a mobile *domain wall* (DW) is formed to balance the exchange and anisotropic energies [1]. Spin-polarized current drives propagation of magnetic domains for stable domains and controlled DW motion. Fast, low-energy access and high endurance makes DWM a promising data storage device [2] and creates potential for logic implementations [3].

To achieve improved density, data shifting is necessary to align data with access points. Thus, shift fault characterization from process variation must be characterized to allow DWM designs to appropriately tradeoff efficiency and reliability. There has been significant effort on power reduction and speed improvement [4]–[7] to optimize DWM shifting overhead; relatively fewer efforts [8], [9] focus on shift *reliability* due in part to insufficient error-modeling, which we address here.

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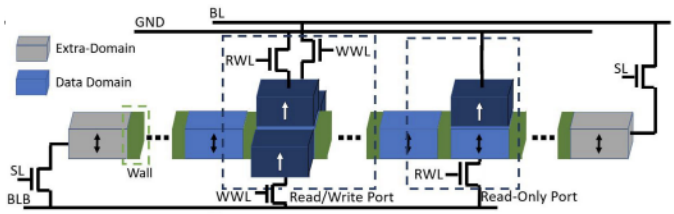


Fig. 1. Anatomy of a DWM nanowire [5].

DWs are held at *pinning sites* from intentionally engineered notches at regular intervals to ensure controlled shifting and alignment. The notches create a potential well that must be overcome to allow DW motion. While many notch shapes have been explored, triangular notches have become standard as they minimize shifting energy while being fairly invariant to thermal effects. Slight over- or under-shifted DWs tend to *relax* toward pinning sites. Notch deformation creates non-uniform pinning strength. Sufficiently deformed notches can keep a DW pinned when applying the rated shift current.

In this brief, we are the first to advance error modeling for DWM by demonstrating and characterizing *uncontrolled nanowire pinning* during DW motion. We model geometric notch variation impact of width, depth, and *curvature* by 10% on the critical shift current as representative fabrication process variation. Our model demonstrates that runtime *pinning faults* occur at a rate of circa $1.6\ 10^{-8}$. Next we discuss the system-level motivation and need for development of this fault model.

II. Motivation

An example of a planar (2D) DWM nanowire with shift write ports is shown in Fig. 1 [5]. The value of each domain is determined by its polarization as illustrated by arrow direction. Access ports (read and/or write locations) are fixed elements. Thus, a domain needs to be shifted and aligned with the access port to be read or written. This requires "padding" domains (shown in gray) on each side of the data domains to prevent data loss. During shifting, a pulse is sent along the nanowire. Once a domain is aligned with the head, an orthogonal current to the nanowire along the access port fixed layer can be used to read or write the domain like an MTJ. Shift based write ports allow writing a domain by shifting orthogonally to the nanowire from fixed magnetization domains, in order to reduce energy due to high writing currents [5].

To build memories from nanowires, a "bundle" of nanowires are grouped together to enable parallel bit-wise access to each element of a memory row. The row data width is determined by the number of nanowires in the bundle. A *domain block cluster* [4], [10]–[13] (DBC), shown for a cache line granularity in Fig. 2, contains ℓ memory rows where ℓ is the number of data domains in each nanowire. Each bit of the cache line is individually accessed by shifting all the nanowires together.

Prior work has demonstrated that misalignment (under- or over-shift) of one or more nanowires in a DBC is possible

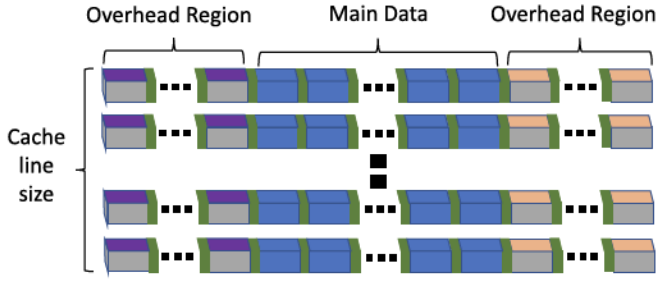


Fig. 2. Domain block cluster (DBC) example.

due to various factors that include current fluctuations in the system. Such faults occur at a rate circa 10^{-5} [8]. In these cases, the entire nanowire uniformly shifts by an incorrect amount. Error correction codes (ECC) alone are insufficient to detect and correct these faults [9] but existing schemes have been proposed to address misalignment resulting in mean-time-to-failure (MTTF) on the order of decades [8], [9].

Uncontrolled nanowire pinning has been demonstrated in early DWM devices [14], [15] which can occur due to process variation. In these cases different parts of the nanowire can shift *different* amounts. When DW motion pushes towards an immutable DW due to uncontrolled pinning, i.e., part of the nanowire shifts one position towards the pinned domain and the remaining part does not shift, a domain is lost at the pinning point. However, if DW motion depins too easily the nanowire may shift one position towards the pinning point and the remainder of the nanowire shifts two positions, duplicating a domain. Both of these effects are *pinning faults*. Either of these pinning faults puts the nanowire and DBC in an unrecoverable state that misalignment protection cannot detect, let alone correct.

Next we discuss in detail the energies of DW motion and pinning potential in a notch.

III. Pinning of a Domain Wall

In this section we describe the expressions that model pinning strength, current-induced depinning, the impact of process variation, and modeling notch deformations.

A. Pinning Potential

The strength of a pinning site is characterized by its pinning strength or *pinning potential*, which depends on the geometry of that notch. The pinning potential per unit area is described in Eq. (1) [16], [17] as follows:

$$V_{pin} \quad \frac{2M_s E\sigma_d}{(q - q_{pin}{}^2} \quad E \quad E_{pin} \quad q \in [q_{pin} - \frac{\sigma_d}{2} \quad q_{pin} + \frac{\sigma_d}{2}] \quad E \quad 0 \text{ otherwise} \tag{1}$$

where q and σ_d are the DW center and width, respectively (Fig. 3(a)), q_{pin} is the pinning site, V_{pin} is the associated pinning potential, and M_s is the saturation magnetization of the material used. The anisotropic and exchange energy per unit area of a notch contributes to the energy density (E_{pin}) of a notch [18]. σ_d and E_{pin} are represented as:

$$\sigma_d \quad \pi\sqrt{\frac{A_{ex}}{K_u}} \quad E_{pin} \quad A_{ex}\frac{\pi^2}{2\sigma_d} + \frac{\sigma_d K_u}{2} \tag{2}$$

respectively, where A_{ex} and K_u are the exchange coefficient and magneto-crystalline anisotropy, respectively [19], [20].

B. Current-Induced Depinning of a DW

A current pulse with adequate amplitude can depin a wall such that it can travel along the nanowire to the next pinning site. During current flow, the *4s* conduction band electrons interact with the *3d* band electrons of magnetic domains generating an exchange interaction torque [21]. At a domain wall the magnetization flips over a plane parallel to the wall. As a result, the conduction electrons bend at the wall while crossing it, amounting to a transfer of momentum between the passing electrons and the local magnetic moment of the wall. This transfer process is adiabatic and included in Eq. (3). Due to the conservation of energy, the electrons exert a force on the wall, which can move it with sufficient current density [22]. The micromagnetics of shifting a DW is governed by the Landau-Lifshitz-Gilbert equation with the inclusion of current-induced torques [23] (assuming the current flows into x-direction) as:

$$\frac{dM}{dt} \quad -\gamma M \quad H_{eff} + \quad M \quad \frac{dM}{dt} - v_j\frac{M}{x} + \beta v_j M \quad \frac{M}{x} \tag{3}$$

where M, H_{eff}, , γ, and β are the magnetization orientation, effective field, Gilbert damping constant, gyromagnetic ratio, and non-adiabatic spin-torque coefficient, respectively. The last two terms that are functions of M x represent the current-induced torques that are responsible for DW shifting with shifting velocity of v_j.

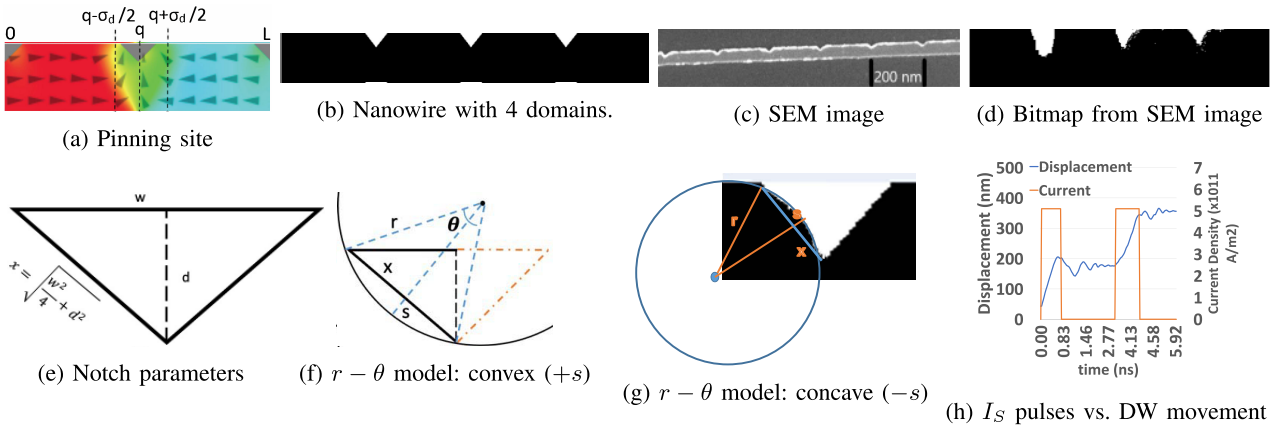
C. Process Variation

As alluded to previously, triangular notches are most common in DWMs as the pinning strength of a triangular notch is sufficient to avoid depinning due to thermal perturbation but small enough to require a relatively low shift current. An ideal triangular notch is symmetrical on the Y-axis. However, process variations can alter the symmetry, which deflects the pinning potential. A non-uniform distribution of pinning potential due to process variation impacts the shift current requirement at each notch.

Figs. 3(b)–3(d) show the shape and geometric deformities of notches in a nanowire having domains of 200nm long and 100nm wide. An ideal notch (Fig. 3(b)) is a symmetrical triangle as shown in Fig. 3(e) with width w 50nm and depth d 30nm. There is geometric variation due to fabrication processes such as lithography and deposition as shown in an scanning electron microscope (SEM) image (Fig. 3(c)). However, notches can have depth and width variation and can be curved as opposed to having perfect line segments (Fig. 3(d)). We adapted the ±5% variation of width and depth of the notches described in models in the literature [18], [24] and expanded this to include ±5% variation in the area increased or decreased by a curved side of the notches described next.

D. Modeling Notch Deformation Using Curvature

To model notch deformation using curvature we interpret one side of the triangular notch as an arc of a circle that passes through the starting and ending points of the ideal notch edge. The ideal notch edge is the chord to this arc. Our method to model the curvature considers both the convex (Fig. 3(f)) and concave (Fig. 3(g)) arcs, where the concave case is reflected about the chord. The arc length is S $r\theta$, where r is the radius of the circle and θ is the angle at the center of the circle to specify the arc. In the case of a perfect notch, the radius r increases asymptotically towards infinity



(a) Pinning site (b) Nanowire with 4 domains. (c) SEM image (d) Bitmap from SEM image

(e) Notch parameters (f) $r-\theta$ model: convex $(+s)$ (g) $r-\theta$ model: concave $(-s)$ (h) I_S pulses vs. DW movement

Fig. 3. Process limitations leading to notch deformities, modeling the notch, and demonstration of motion in the nanowire.

and similarly θ decreases towards zero such that the arc and chord are indistinguishable. The degree of curvature can be quantified by the length of the sagitta s between the curve and the ideal notch edge (chord). The sagitta represents the displacement or deflection of the farthest point of the arc from the mid point of the chord as described in Eq. (4), where x is the length of the chord.

$$s = r - \sqrt{r^2 - x^2/4}. \tag{4}$$

Varying the sagitta (curvature) varies the area displaced by the notch. If the sides of a triangular notch become curved instead of straight lines, the area of the notches is increased or decreased based on the curvature type, i.e., convex notches have increased area and concave notches have reduced area. Similar to the method for width and depth variation, we also considered ±5% variation of area, centered about a perfect notch, where the radius of the circle is infinity which corresponds to a sagitta $s = 0$.

Recalling that Fig. 3(e) shows our ideal triangular notch, the area of the half of the notch is $A = \frac{1}{4}wd$. Fig. 3(f) depicts a deformed convex notch, with the corresponding model for the concave case in Fig. 3(g). The increased area due to the deformed side is given by:

$$\Delta A = \frac{\theta r^2 - (r-s)\sqrt{\frac{w^2}{4} + d^2}}{2} \approx \frac{s\sqrt{\frac{w^2}{4} + d^2}}{2}. \tag{5}$$

For small curvature variation, θ remains sufficiently close to zero such that $S \approx x$. Thus, θ can instead be expressed as the ratio of x to r or as a function of d and w is $\sqrt{w^2/4 + d^2}/r$, which reduces ΔA as shown in Eq. (5). For our experiments, we change the area relative to the ideal half-notch area to form the upper bound on how s is varied.

In the next section we present the results of experiments to study the impact of varying the notch width, depth, and curvature to study the impact of variation.

IV. Results and Discussion

In our experiments our control was a DW nanowire with triangular notches on the top edge of the nanowire with a width of 50nm and a depth of 30nm. Fig. 3(b) shows a conceptual layout of a typical DW nanowire segment with 4 domains. Our experiments vary the notch shape in terms of width, depth, and curvature to determine their impact of shifting behavior. We simulated nanowires with dimensions $3200 \times 100 \times 2$nm, separated into 16 domains by notches every 200nm. The material properties of the nanowire are listed in Table I.

TABLE I
Material Properties Used in Simulation

A_{ex} (J/m)	M_s (A/m)	α	K_u(J/m^3)	a (nm)	$\gamma(s^{-1}\mathrm{T}^{-1})$
2.0×10^{11}	6.5×10^{5}	0.02	10^{6}	0.287	1.76×10^{11}

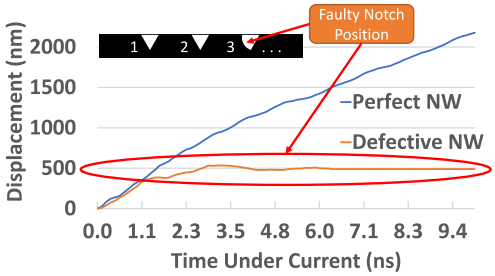


Fig. 4. Domain wall stuck at a faulty notch position.

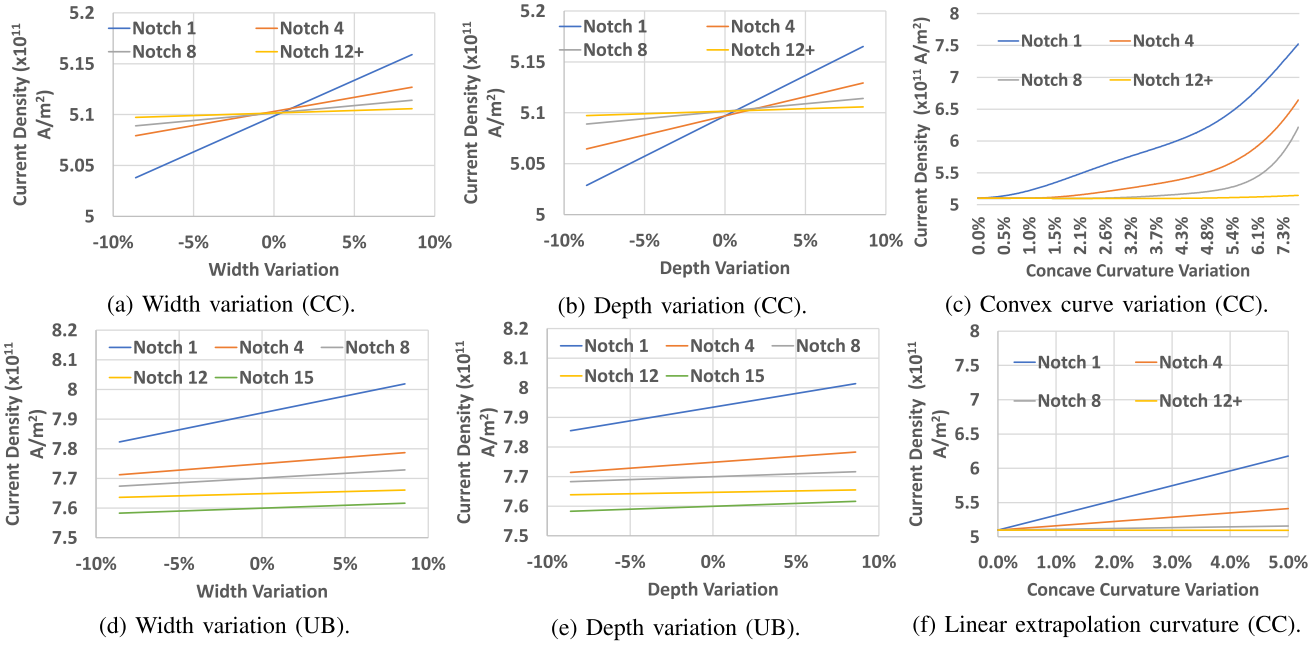
A. Determination of Shifting Current Density Range

We used the open-source micromagnetic simulator, mumax3 [25] to calculate the critical current requirement represented in Eq. (3) ignoring thermal fluctuations and assuming the absence of an external magnetic field. While our experiments varied the notch shape across the variables of interest, we held the nanowire width, thickness, and length constant (no variation). We initialized the nanowire with random magnetization, and allowed the nanowire to relax. To calibrate DW movement, we applied two consecutive current pulses of 0.5ns at a 3ns interval, and tracked the DW position along the nanowire (3ns is the relaxation time after 1-bit shifting). Fig. 3(h) shows the current pulse applied to the nanowire in orange and the subsequent x direction DW displacement in black.

We tuned the shift current to find the critical current density for shifting in this ideal scenario. A nanowire containing 16 domains with no deformed triangular notches requires a minimum current density of $5.1 \times 10^{11} A/m^2$ to successfully shift one bit. We also calculated the upper-bound of shift current density above which the DW shifts by two positions as $7.9 \times 10^{11} A/m^2$. These values serve as the control for comparison with deformed nanowires.

B. Demonstration of Pinning From Notch Deformation

To demonstrate faulty pinning conditions, we applied the critical shift current continuously for 10ns to an ideal nanowire



(a) Width variation (CC). (b) Depth variation (CC). (c) Convex curve variation (CC).

(d) Width variation (UB). (e) Depth variation (UB). (f) Linear extrapolation curvature (CC).

Fig. 5. Change in critical shift current (CC) and associated upper bound (UB) from variation.

and a nanowire with a deformed notch in the 3rd and 7th pinning sites. We introduced a DW at the first notch and measured the distance traveled in both cases. Fig. 4 demonstrates that the wall becomes stuck at the 3rd notch, which is deformed with curvature as shown in the inset of the figure. Domain motion stops after traveling approximately 400nm in the nanowire with the deformed notches, whereas it travels over 2000nm in the ideal nanowire. This phenomenon demonstrates an occurrence of a pinning fault.

In the following sections we relate experiments to quantify the currents required for correct shifting when deformed notches due to perturbations in notch width, depth and curvature at different sites along the nanowire.

C. Notch Width, Depth, and Curvature Variation

To better understand the variation impact we first studied notch width and depth deviation from ideal values of 50nm and 30nm, respectively, at different pinning sites with no curvature. We considered 33 data-points increasing linearly in the range of $\pm 10\%$ for both parameters and calculated the critical currents for shifting. Each parameter was varied in isolation and the test was repeated at different notch positions, such that position 1 is the notch closest to the shifting current.

Fig. 5(a) shows the impact of varying the notch width on the critical shifting current (CC). The CC varies symmetrically about the ideal CC of $5.1 \times 10^{11} A/m^2$, with the largest impact at the notches closest to where shifting current enters the nanowire. The same pattern exists for the CC when depth is varied, shown in Fig. 5(b). Considering the impact on the upper bound current for correct shifting (UB) width variation is shown in Fig. 5(d). The slope varies less per unit change in notch width but notch position has a greater impact. Again, a similar pattern holds for varying notch depth, shown in Fig. 5(e). In all cases, the trend is well-represented by a linear equation; this forms the basis for our models of the impact of notch position, width, and depth on CC and UB, respectively.

Considering approximately 10% variation of area relative to the ideal notch, $\Delta A \leq 0.05wd/4$. Using ΔA from Eq. (5) we translated the curvature variation into a maximum sagitta length s_{max}. Holding the width and depth fixed as endpoints to a chord as in Fig. 3, we varied the sagitta length on $[-s_{max}, 0]$ (concave) and $[0, s_{max}]$ (convex) to produce deformed notches while other parameters remained fixed. Fig. 5(c) depicts the critical current variation for convex notches. Curvature deformity at notches near the shift current source incurs the highest variations and has a significant impact on CC. The trend is not linear, but can be approximated as linear for $\leq 5\%$ variation, shown in Fig. 5(e). The change in UB in all cases is indistinguishable from the perfect nanowire value of $7.9 \times 10^{11} A/m^2$. Similarly, for concave-type deformities, the change in both CC and UB are also indistinguishable.

From these results a measurable impact on CC and UB currents is demonstrated from all parameters, but the relative weights varied significantly with notch position and curvature having larger impacts than depth and width variation. We use this data to populate a fault model in the next section.

D. Modeling Pinning Fault Likelihood

We used a least squares regression to fit a curve approximating the relationship of critical and upper bound currents as a function of variations in width, depth, and sagitta, respectively. After adjusting for notch position, these curves and their respective residuals were combined via the total differential method to produce the uncertainties in our nominal critical ($5.1 \times 10^{11} A/m^2$) and upper bound ($7.9 \times 10^{11} A/m^2$) currents. We assume that a device which varies in any of our parameters by greater than $\pm 5\%$ is discarded at fabrication time, represented by applying a truncated normal distribution on all parameters. For curvature, we model only the effects of convex curvature on the critical shift current, in keeping with our results from Fig. 5(f). To model process variation, each distribution is scaled to match a coefficient of variation of 0.2. Using the resultant distributions, we can quantify the probability P_i that the applied shift current of $6.5 \times 10^{11} A/m^2$ will fall above the critical current plus the uncertainty and below the upper bound current minus the uncertainty at any given notch position i. Since all previous domain positions must shift correctly for domain at notch i to shift correctly,

TABLE II
LIFETIME TO PINNING FAILURE UNDER ERROR CORRECTION

Scrub	ECC-0		ECC-1		ECC-2		ECC-3	
	Ov.	MTTF	Ov.	MTTF	Ov.	MTTF	Ov.	MTTF
No	0%	2 sec	12.5%	33 sec	23.4%	1.0 yr	34.3%	24k yr
Yes	0%	2 sec	12.5%	59 sec	23.4%	2.3 yr	34.3%	34k yr

we define the probability that a DW at notch position i shifts correctly as $Q_i = \Pi_{n=1}^{i} P_i$. Likewise, the cumulative product of Q_i across all notches forms the probability of a correct shift operation, thus we define the probability of pinning as $P_{pin} = 1 - (\Pi_{m=1}^{15} Q_m)$. Based on our simulation results, this model predicts that faults associated with pinning occur with 1.58×10^{-8} probability. When there are fewer DWs than notches, this rate could improve depending on wall positions.

E. DWM System Study

To evaluate the impact of pinning faults, an 8-way 4MB LLC cache and a 8-way 32KB L1 DWM cache architecture [10] with our fault model were integrated into and simulated using the Sniper multi-core simulator [26] presuming four out-of-order cores running at a clock speed of 3 GHz. DWM nanowire data lengths of $n = 32$ and cache lines of 512-bits created DBCs composed of 512*32 = 16Kbs. Workloads were 14 benchmarks from SPEC-CPU2006 [27].

Presuming a 4.55×10^{-5} misalignment fault rate [8], prior work is able to achieve a mean-time-to-failure (MTTF) of 15 years [9] and 69 years [8]. When introducing pinning faults at 1.58×10^{-8} probability, presuming misalignment is corrected through prior work, we added parity nanowires to fix pinning faults with ECC as shown in Table II. Without correction, MTTF is 2s from pinning, and remains <1 min with single error correction (ECC-1). ECC-2 (23.4% overhead) is required to achieve 1 year MTTF. Scrubbing, or writing ECC corrected values when faults are detected, provides some benefit, increasing ECC-2 from one to more than two year MTTF. However, the typical >10 yr lifetime target requires ECC-3.

V. CONCLUSION

In this brief, we describe and characterize the understudied pinning fault mode in DWM shifting. Our model of this variation considers variation in notch width, depth, and curvature predicts a small but non-negligible probability of pinning faults of 1.58×10^{-8}, necessitating techniques to mitigate such faults in DWM circuits and device descriptions. The impact on current variation is significant when notch deformities are close to the shift port, which supports targeted mitigation and/or special attention to notch quality at DWM shift points.

Future work should study methods to detect pinning in DWM nanowires to aid in fault tolerance without 34% overheads needed from general purpose ECC-3. For example, detecting different DW speeds at the extremities could indicate a pinning fault. New fault-tolerance for process variation, quantified by this modeling, is vital to reaping the benefits of DWM in next-generation tiered memory systems.

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