

A Tunable Parallel-Plate Capacitor Using Liquid-Metal Actuation

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Abstract—A tunable parallel-plate capacitor is demonstrated using continuous electrowetting actuation of liquid metal. A 1-mm gap is made in one conductive plate of the capacitor, and the manipulation of conductive materials changes the effective area of the plate. The addition of an electrolyte to fill the gap yields a 5.43-pF difference, while further fine-tuning using the actuation of liquid metal yields a 0.58-pF change in capacitance. The tunable capacitor can be varied at 1 GHz from 2.90 pF to 10.34 pF, resulting in a 1:3.57 change in capacitance.

Index Terms—capacitors, liquid metal, microfluidics, tunable circuits and devices.

I. INTRODUCTION

Tunable electronics play an integral part in the optimization and efficiency of emerging wireless communication technology. Precise tuning of dynamic wireless systems is a necessity, and many times, tunability is a requirement for filters, voltage-controlled oscillators, and phase shifters. There exists an ever-growing need for smaller and more efficient solutions for the next generation of RF front-end components.

Existing methods of tuning capacitance include varactors, microelectromechanical systems (MEMS), and capacitor arrays. Varactors are voltage dependent and require a significant change in voltage to achieve an acceptable tuning range. A design in [1] shows that an applied voltage must be varied from 0 to 15 V to achieve a tuning range of approximately 1:5. MEMS capacitors typically use higher actuation voltages and have a limited capacitance variation [2]. Capacitor arrays or banks have a limited capacitance range, given the amount of area required [3].

Liquid metal has shown great potential in the area of reconfigurable electronics. Galinstan, a non-toxic liquid metal with an electrical conductivity of 2.30×10^6 S/m, remains in a liquid state between -19°C and 1300°C [4]. These characteristics are favorable, and the manipulation of Galinstan as a liquid has been used to effectively tune a variety of components, including patch antennas [5], RF switches [6], and waveguides [7].

Liquid metal has also been used to create capacitors. In [8], a tunable capacitor was demonstrated by moving liquid metal through two parallel tubes. However, this required bulky mechanical pumping. Another example was based on the ability of liquid metal to expand based on temperature, where the liquid metal expands in a narrow path to connect multiple plate capacitors in parallel [9].

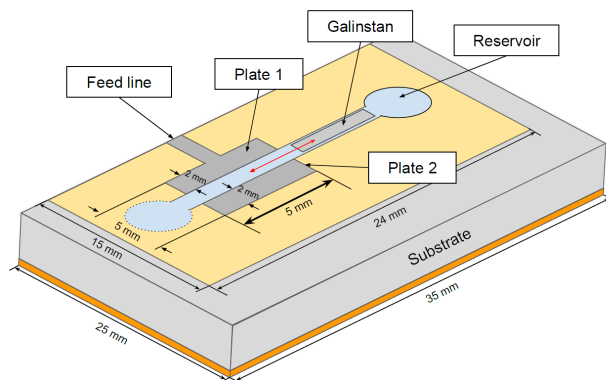


Fig. 1. Tunable parallel-plate capacitor concept. Galinstan is actuated through a channel when a probe is placed at each reservoir and an AC voltage is applied across the channel. Galinstan fills the gap to change the capacitance.

The tunable parallel-plate capacitor presented in this paper incorporates liquid-metal actuation within an electrolyte-filled channel to manipulate the effective area of a parallel plate. In contrast to the two liquid-metal capacitors described above, the design in this paper is based on electrical actuation that is more compatible for tunable electronics. One method of moving liquid metal, using an applied AC voltage, is known as continuous electrowetting actuation (CEW) [10] and is selected from a variety of proven electrical actuation methods, including electrocapillary actuation [11]. CEW is beneficial in this case, as it maintains relative device simplicity and does not require a continuous applied voltage after the liquid metal is moved to the desired location.

The tunable capacitor presented here takes advantage of CEW actuation techniques to provide a low-voltage and low-power means of tuning capacitance, while demonstrating a tuning range of 1:3.57.

II. DESIGN

The tunable parallel-plate capacitor concept is shown in Fig. 1. The top conductor of the capacitor consists of two disconnected $5\text{ mm} \times 2\text{ mm}$ conducting plates separated by a 1-mm-wide gap on the surface of a grounded substrate. Plate 1 is connected to an SMA connector via a 4-mm long 50- Ω microstrip feed line, while Plate 2 is unconnected to any external port.

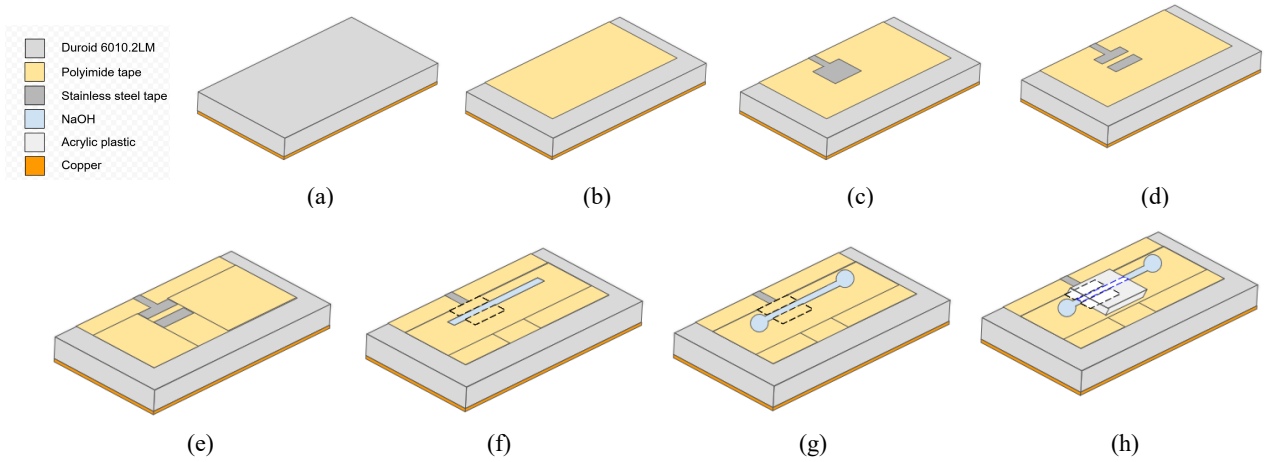


Fig. 2. Fabrication steps: (a) bare substrate, (b) substrate with polyimide layer, (c) full plate capacitor, (d) plate with 1 mm gap, (e) plate with gap and spacer layer, (f) bottom of channel defined, (g) channel and reservoirs fully defined, and (h) acrylic plastic cover affixed.

A reservoir of electrolyte connected to a channel with Galinstan completes the design. A low-voltage AC signal applied to the electrolyte actuates the Galinstan, causing it to move toward and gradually bridge the gap between the two conducting plates. This results in an increase in the effective area of the plate and thus yields a higher capacitance.

A. Fabrication

Fig. 2 illustrates the fabrication steps leading up to the completed design shown in Fig. 1, starting with a 1.27-mm-thick Rogers RT/Duroid 6010.2LM with a relative permittivity of $\epsilon_r = 10.2$ [Fig. 2(a)]. In Fig. 2(b), a single 0.09-mm layer of polyimide tape is secured directly onto the substrate surface to provide a means of sealing the bottom of the channel. Fig. 2(c) shows a full-plate capacitor, with the top plate and 50- Ω microstrip feed constructed from stainless steel tape. A variation of the Rapid, Economical Circuit Prototyping (RECI-P) fabrication method [12] is adapted to cut and apply the stainless steel in the form of a 0.0762-mm-thick metal tape. Typical microstrip line designs use copper, but this design uses stainless steel to allow direct contact between the conductive plates and the contents within the channel. The stainless-steel conductor avoids corrosive effects of the electrolyte and prevents the liquid metal from sticking to the microstrip line. In Fig. 2(d), a 1-mm-wide gap of stainless steel is removed, causing the two remaining half plates to be disconnected.

Figs. 2(e)–(f) illustrate the multi-layer stack-up of polyimide to form the channel that controls the movement of the Galinstan. In Fig. 2(e), two additional single layers of polyimide tape are applied adjacent to the plates, providing a horizontally level surface for the channel layers above. The polyimide channel walls, in Fig. 2(f) and 2(g), are then formed atop the conducting plates and have a height of 0.54

mm. The channel is 1 mm wide and 12 mm long. Connected to this channel are 0.28-mm-high reservoirs to provide a means of egress for the displacement of electrolyte during actuation. The height difference between the channel and the reservoirs aid in preventing Galinstan leakage during actuation. To complete the fabrication, an acrylic plastic lid is secured atop the channel to create a seal [Fig. 2(h)]. The full build of the parallel-plate capacitor with the mounted channel is approximately 35 mm wide and 25 mm long, as shown in Fig. 1.

B. Electrical Actuation of Liquid Metal

An electrolyte and aqueous solution, NaOH, and a liquid metal, Galinstan, are used to bridge the connection between the two conductive plates. CEW actuation is used to manipulate the interfacial tension around Galinstan within an electrolyte-filled channel and induce movement using an applied AC voltage.

The polyimide channel is filled with a solution of 1-M NaOH and a slug of Galinstan. The Galinstan slug is 1 mm wide and 5 mm long to completely fill the gap between the conductive plates. To actuate the Galinstan in the channel, an electrode is attached to each reservoir and a 4- V_{pp} AC signal with a DC offset of 3 V_{DC} is applied across the channel at a frequency of 30 Hz.

III. EXPERIMENTAL RESULTS

A Keysight N9912A FieldFox Vector Network Analyzer (VNA) was used to measure the S_{11} of various device states. Table 1 summarizes the measured resistance R , capacitance C , quality factor Q , and resonance frequency f_0 for seven different cases. Fig. 3 shows representative measurements for three of those cases; for clarity, only the frequency range below resonance, when the device is capacitive, is shown.

The R and C values in Table I are taken directly from measured Smith Chart plots at 1 GHz, which is below resonance for all cases; f_o is also taken directly off of the measured Smith Charts where S_{11} transitions from -180° to $+180^\circ$.

Assuming an equivalent series RLC circuit, the quality factor Q can be found from [13] to be

$$Q = \omega \frac{W_m + W_e}{P_{loss}}, \quad (1)$$

where the stored magnetic energy W_m , stored electric energy W_e , and power loss P_{loss} for a series resonator are:

$$W_m = \frac{1}{4} |I|^2 L, \quad (2a)$$

$$W_e = \frac{1}{4} |I|^2 \frac{1}{\omega^2 C}, \quad (2b)$$

$$P_{loss} = \frac{1}{2} |I|^2 R. \quad (2c)$$

Substituting these into (1) and simplifying yields

$$Q = \frac{1}{\omega_o RC} \left(\frac{\omega + \omega_o}{\frac{\omega_o}{\omega} + \frac{\omega}{\omega_o}} \right), \quad (3)$$

where $\omega_o = \frac{1}{\sqrt{LC}}$. Note that at $\omega = \omega_o$, (3) reduces to the familiar $Q_o = \frac{1}{\omega_o RC}$, as expected. Table I uses (3) to calculate Q at the below-resonance frequency of 1 GHz since all other parameters in that table are recorded at that frequency.

Note that all measurements include the contributions of the SMA connector and microstrip feedline. Although de-embedding is typically performed during the measurement process (e.g. thru-reflect-line calibration, or network analyzer port extension), feedline de-embedding using the VNA was not available at the time of this investigation. However, it should be noted that the SMA connector and feedline were unchanged for all seven cases, and thus case-to-case variations in Table I can still be observed.

Case A is a baseline measurement for the intermediate fabrication step shown in Fig. 2(c). Case B represents the intermediate fabrication step in Fig. 2(d). The 63% decrease in capacitance between Cases A and B is consistent with the 60% decrease in stainless steel surface area arising from the disconnected portion of the plate and gap. Case C refers to the structure with all polyimide layers in place as shown in Fig. 2(h), but with the channel and reservoirs filled with air. Note that the resistance and capacitance of Case C increase compared to Case B due to the polyimide superstrate which has a relative permittivity of $\epsilon_r = 3.5$ and a loss tangent of 0.008.

A. Effect of NaOH in Channel

As shown in Case D, filling the channel with NaOH yields a capacitance increase of 2.87 times that of an air-

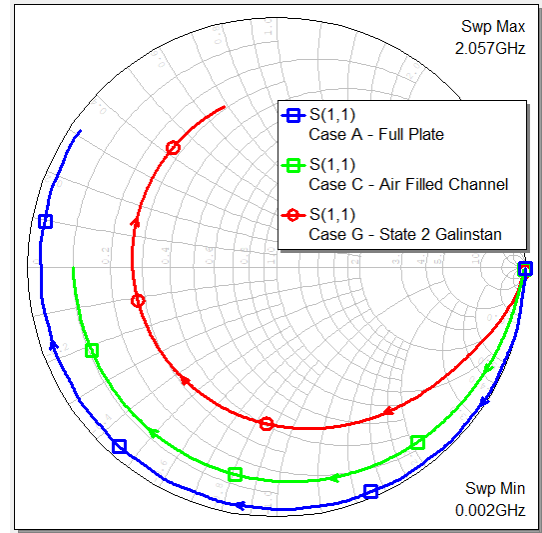


Fig. 3. Measured S_{11} vs. frequency for three of the seven cases in Table I.

TABLE I
MEASURED RESISTANCE, CAPACITANCE, Q -FACTOR, AND
RESONANCE FREQUENCY FOR VARIOUS DEVICE STATES

Case	Device State	R (Ω)	C (pF)	Q	f_o (GHz)
A	Full plate	1.59	4.57	12.98	1.69
B	Plate with gap	1.32	1.68	24.07	2.98
C	Air filled channel	8.15	2.90	3.27	2.06
D	NaOH filled channel	17.36	8.33	0.78	1.42
E	Galinstan State 0	18.95	9.76	0.63	1.37
F	Galinstan State 1	16.12	10.04	0.73	1.34
G	Galinstan State 2	14.90	10.34	0.78	1.32

filled channel. A solution of 1-M NaOH is used, which has a conductivity of 17.6 S/m and loss tangent of 4.649 [14]. Because the channel and reservoirs are filled with this slightly conductive fluid, the effective area of the plate is increased, resulting in an increase in capacitance. The lossy dielectric nature of the NaOH solution also causes an increase in resistance to increase, and decrease in Q .

B. Effect of CEW Tuning

Although CEW permits continuous (non-discrete) motion of the Galinstan into the channel, for simplicity we report the effect of the position of Galinstan in the channel at only three different states, as shown in Fig. 4.

State 0 is the case when the Galinstan slug has no connection to the plates, and States 1 and 2 are the cases when the Galinstan is halfway and fully connecting the two conductive plates, respectively. As shown in Table I, an increase in capacitance from State 0 to State 1 to State 2 is observed as the Galinstan bridges the gap between the two conductive plates.

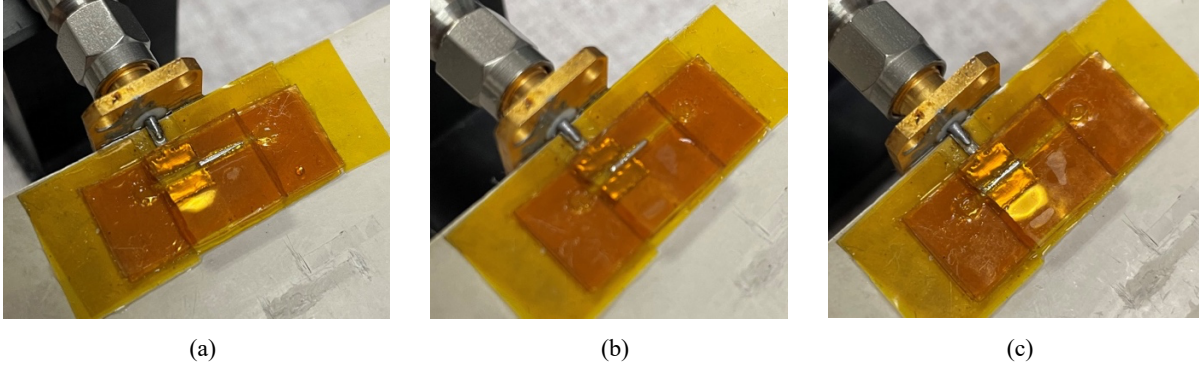


Fig. 4. Tunable capacitor in (a) State 0, (b) State 1, and (c) State 2.

The measured values of the Galinstan states indicate that the capacitance can be fine-tuned within a continuous 0.58-pF capacitance range between State 0 and State 2. If the initial Case C is included, the capacitance tunes from 2.90 pF to 10.34 pF, representing a 1:3.57 tuning range.

IV. MODELING

A. Simulation vs. Experiment Baseline

Since Case A of Table I serves as the basis for all other cases in that table, the full plate was the most logical starting point for modeling, to establish a baseline for comparing simulation with experiment. A Cadence AWR AXIEM model was created for the structure shown in Fig. 2(c). The simulated versus measured S_{11} is shown in Fig. 5, showing reasonably good agreement. Values for R , C , Q , and f_o at 1 GHz are compared in Table II.

B. Intrinsic Equivalent Circuit for Full Plate

The baseline simulation described above provides some degree of confidence in the modeling effort going forward. Fig. 6 proposes an intrinsic equivalent series RLC circuit of the full plate that excludes the effect of the SMA connector and feedline that were omnipresent during measurement. Here, C_a is the capacitance of the full plate, L_a is the parasitic inductance, and R_a is the parasitic resistance due to conductive (stainless steel, copper) and dielectric (polyimide, Duroid) losses.

The S_{11} of the structure shown in Fig. 6(a) is simulated in AWR AXIEM, with the simulation port located at the point where the feedline would have contacted the plate. The S_{11} is then converted to impedance, and f_o is easily determined as the frequency at which the imaginary part of that impedance is zero. The intrinsic capacitance C_a is found from the imaginary part of Z_L , and the intrinsic inductance L_a is found from

$$\omega_o = \frac{1}{\sqrt{LC}}. \quad (4)$$

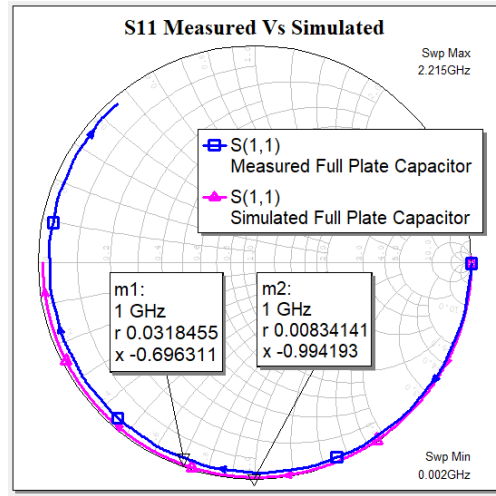


Fig. 5. Comparison of measured and simulated data of the full-plate capacitor with feedline.

TABLE II
MEASURED VS. SIMULATED PERFORMANCE OF FULL PLATE WITH FEEDLINE

	R (Ω)	C (pF)	Q	f_o (GHz)
Measured (1 GHz)	1.59	4.57	12.98	1.69
Simulated (1 GHz)	0.42	3.20	71.22	2.22

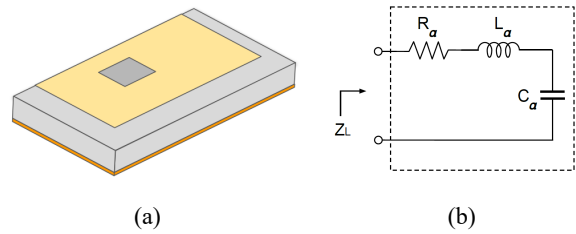


Fig. 6. Full-plate capacitor without feedline: (a) structure, and (b) equivalent circuit.

The intrinsic resistance R_a is found from the simulated $\text{Re}(Z_L)$. The results of this simulation are shown in Table III. Compared to Table II, the resistance and capacitance decreased as a result of excluding the feedline, as expected.

For comparison, calculating the capacitance of a 5 mm $\times$ 5 mm parallel-plate capacitor with two dielectrics (0.09-mm-thick polyimide and 1.27-mm-thick Duroid) excluding fringing yields a capacitance of 1.47 pF.

TABLE III
EQUIVALENT CIRCUIT FOR FULL PLATE WITHOUT FEEDLINE

	R_a (Ω)	C_a (pF)	L_a (nH)	Q	f_o (GHz)
Simulated (1 GHz)	0.28	2.18	0.57	136.75	4.52

C. Intrinsic Equivalent Circuit for Isolated Half Plate

Fig. 2(d) shows two 5 mm $\times$ 2 mm conducting plates separated by a 1-mm-wide gap. Even though each 5 mm $\times$ 2 mm conducting plate constitutes 40% of the footprint of a 5 mm $\times$ 5 mm full plate, for convenience we refer to each as a “half plate”. A proposed equivalent circuit for the isolated half plate with gap is shown in Fig. 7. “Isolated” refers to the fact that the second half plate is nonexistent.

The isolated half plate has a respective resistance, capacitance, and inductance, identified as R_β , C_β , and L_β . Note that these values are expected to differ from R_a , C_a , and L_a of the full plate. Compared to Table III, the 54% decrease in capacitance is an expected result arising from a 60% reduction in the surface area of the plate. However, the cause for the increase in resistance requires more investigation.

For comparison, calculating the capacitance of a 5 mm $\times$ 2 mm parallel-plate capacitor with two dielectrics (0.09-mm-thick polyimide and 1.27-mm-thick Duroid) excluding fringing yields a capacitance of 0.59 pF.

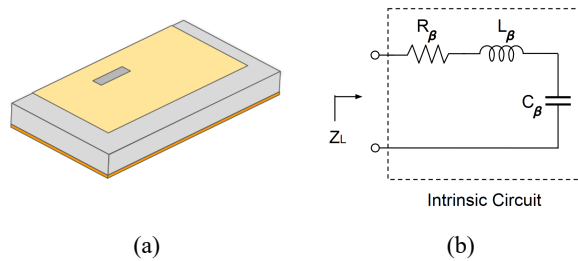
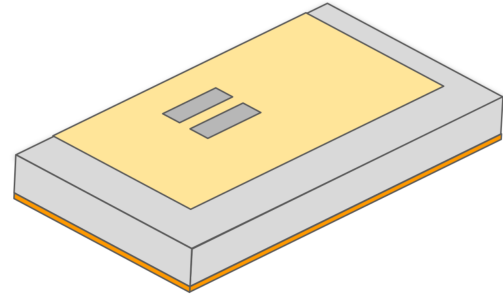


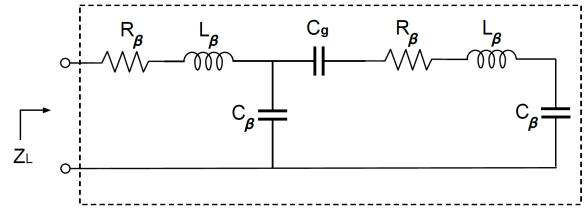
Fig. 7. Isolated half plate: (a) structure, and (b) equivalent circuit.

TABLE IV
EQUIVALENT CIRCUIT FOR ISOLATED HALF PLATE WITHOUT FEEDLINE

	R_β (Ω)	C_β (pF)	L_β (nH)	Q	f_o (GHz)
Simulated (1 GHz)	0.58	1.00	0.34	139.04	8.64



(a)



(b)

Fig. 8. Plate with gap, without feedline: (a) structure, and (b) equivalent circuit.

D. Intrinsic Equivalent Circuit for Plate with Gap

A proposed equivalent circuit for the plate with gap (Fig. 2(d), but without the feedline) is shown in Fig. 8. Each isolated half plate has an associated R_β , C_β , and L_β as described earlier, but here the edge capacitance C_g due to the gap between the two half plates is also included.

To determine C_g , the simulated S_{11} of the structure shown in Fig. 8(a) is fit to the equivalent circuit of Fig. 8(b), using the values of R_β , C_β , and L_β from Table IV. C_g is calculated to be approximately 0.01 pF.

E. De-Embedding via Modeling

AWR AXIEM software was used for all electromagnetic simulations in this study. The simulations were limited however, because Galinstan, NaOH, acrylic superstrate, and the reservoirs were not incorporated into the modeling. Although future work will include these effects – thus changing the values of R , L , and C in Tables III and IV – this paper only includes modeling for the basic cases described above.

In the meantime, however, one could conceivably deembed the intrinsic device from the measured data as shown in Fig. 9. In this figure, the two-port embedding network consolidates the effects of the SMA connector, microstrip feedline, and step-in-width discontinuity from feedline to device.

The results of Fig. 5 showed that there was reasonable agreement between the measured and simulated perfor-

mance (i.e., the “Cascaded S_{11} ” in Fig. 9) of the full-plate capacitor with feedline. VNA-based de-embedding (e.g., using microstrip-based short-open-load calibration standards) would have moved the reference plane directly to the intrinsic device, but this procedure was not available at the time of measurement.

However, by inserting the AWR AXIEM-derived S -parameters of the intrinsic full plate capacitor of Fig. 6(a) into that of the intrinsic device network of Fig. 9, and using the AWR AXIEM-derived “Cascaded S_{11} ” from Fig. 5, one could determine the unknown embedding network in Fig. 9. Since this embedding network models the SMA connector and feedline that remain unchanged throughout the steps in Fig. 2, it should then be possible to use it in de-embedding the results in Table I. However, the process is more complicated, in that the embedding network also includes the step-in-width discontinuity between the feedline and device. Additional investigation will be pursued in future work.

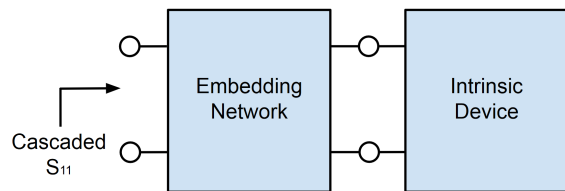


Fig. 9. Modeling-based de-embedding.

V. CONCLUSION

A tunable capacitor was demonstrated to have a 1:3.57 capacitance tuning range. The use of Galinstan and NaOH in a polyimide channel to tune a parallel-plate capacitor shows promising results and serves as a proof-of-concept for further development of liquid-metal tunable devices.

Limitations of this tunable parallel-plate capacitor design are a low Q , attributed to mounting NaOH-filled channels atop the conductive plates. While stainless steel has a lower conductivity than a typical copper design and could have an effect on the Q , Cases C-G in Table I show that the added channel entity atop the conductive plate is, in particular, correlated with a significant drop in Q . This can be further improved for RF applications by using a smaller conductive plate or a different substrate to increase the self-resonant frequency of the device, thus improving the Q .

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