

DOI: 10.1002/ ((please add manuscript number))

Article type: Full Paper

Influences of native oxide on the properties of ultrathin Al₂O₃-interfaced Si/GaAs heterojunctions

*Md Nazmul Hasan, Yixiong Zheng, Junyu Lai, Edward Swinnich, Olivia Grace Licata, Mohadeseh A. Baboli, Baishakhi Mazumder, Parsian K. Mohseni, Jung-Hun Seo**

Md Nazmul Hasan, Yixiong Zheng, Junyu Lai, Edward Swinnich, Olivia Grace Licata, Prof. Baishakhi Mazumder, Prof. Jung-Hun Seo*

Department of Materials Design and Innovation,
University at Buffalo, the State University of New York,
Buffalo, New York, U.S.A, 14260

*Email: junghuns@buffalo.edu

Mohadeseh A. Baboli, Prof. Parsian K. Mohseni

Microsystems Engineering Ph.D. Program,
NanoPower Research Laboratories,
Department of Electrical and Microelectronic Engineering
Rochester Institute of Technology, Rochester, NY 14623, USA

Keywords: Heterogeneous integration, ultra-thin oxides, micro-transfer printing.

The structure property of non-ideal Si/GaAs heterostructures that were integrated with the ultra-thin oxide (UO) tunneling interfacial layer has been systematically investigated. Si nanomembranes (NMs) were oxidized in different time periods prior to the hetero-integration process to create the non-ideal single-side passivated Si/GaAs heterostructure. The atomic level oxygen distribution and the degree of oxygen content in Si NM and GaAs were carefully investigated using atom probe tomography (APT) and X-ray photoelectron spectroscopy (XPS) to trace changes in the chemical composition and reactional mechanism across the UO interface when the surface of Si NM was exposed to air for

different periods of time. The induced negatively charges at the UO layer caused oxygen diffusion to the GaAs layer and formed the unwanted GaAs oxide layer. This native oxide stack noticeably degraded the thermal properties of the Si/GaAs heterostructure as Si NMs became more oxidized. This study revealed that the poor surface passivation on one side of the heterointerface leads to a both-side oxidation, thus severely deteriorating the transport properties across the heterojunction formed with the UO layer.

1. Introduction

Semiconductor heterojunctions are important building blocks that enable various modern electronics and optoelectronic applications such as heterojunction bipolar transistors (HBTs), high electron mobility transistors (HEMTs), light-emitting diodes (LEDs), and lasers.^[1-5] These heterojunctions are routinely grown on lattice-matched or slightly lattice-mismatched substrates via molecular-beam epitaxy (MBE) or metalorganic vapor-phase epitaxy (MOVPE). The growth of heterostructures using these methods is largely restricted by their lattice parameters, thus, it is impossible to grow high-quality heterostructures that have different lattice constants or different crystal structures.^[6, 7] Therefore, despite the advent of numerous new semiconductors in past decades, their implementation in the formation of heterostructures is limited or not possible by their material parameters.

To overcome this issue, various studies have been performed; the first approach was to use a wafer bonding method to physically bond two different materials together.^[8-10] However, this method suffers from a substantially thick interfacial layer (> 10 nm) due to the presence of native oxide layers from each substrate. It is also difficult to manage the different thermal expansion rates and different degrees of surface roughness from both substrates. Surface-activated bonding (SAB) was introduced to deal with these issues by bonding two different wafers in a vacuum after plasma treatment for native oxide removal.^[11] SAB has been successfully applied to create numerous hetero-integration strategies of two completely

dissimilar semiconductor wafers leading to various applications such as transistors,^[12] photovoltaics,^[13] and other applications.^[14, 15] However, the presence of a few nanometer-thick interfacial layer is still a technological bottleneck that hinders ideal charge transport across the heterojunctions.

The heterojunctions enabled by the semiconductor grafting method via employing an ultra-thin oxide (UO) interface layer was the first approach to tackling the interfacial high density of states that exist between two dissimilar semiconductors.^[16] This method uses a sub-nanometer-thick oxide layer (called the UO layer) to passivate both semiconductor surfaces after native oxide removal and to facilitate charge transport via quantum tunneling. Following the grafting method, various heterostructures of two largely dissimilar semiconductors and their device applications have been demonstrated.^[3, 16, 19-21] While the first UO heterointegration paper (Ref. 16) successfully demonstrated the best possible Si/GaAs heterojunction with well-suppressed native oxide growth both on Si and GaAs surfaces prepared in a controlled environment (e.g., the nitrogen-filled glovebox and the unified UO growth system), this manuscript presents the systematic analysis when the one side of the heterointerface is not well passivated, namely, the Si nanomembrane (Si NM) side in this case. As is well-known, it is relatively easy to achieve a native oxide-free GaAs surface with the UO layer, because some degree of native oxide on the GaAs surface can be effectively removed by purging additional trimethylaluminum (TMA) cycles in the atomic layer deposition (ALD) system prior to Al₂O₃ deposition. On the other hand, the opposite side of the interface (i.e., the Si NM surface) is prone to oxidation because it is inevitable that the Si NM surface is exposed to air after the releasing process and before the integration process onto the UO-coated GaAs surface. Also, Si oxidation can occur during rinsing with deionized (DI) water and nitrogen (N₂) drying process, producing a thin unavoidable native oxide with the thickness range of 0.2 ~ 0.4 nm.^[23] Although the best practice for the UO-interfaced heterointegration is to keep to-be-bonded

surfaces from any unwanted surface oxidation, it is possible that ~~the~~ one side of the UO interface can be oxidized when improper environmental or process conditions are present.

With these reasons as the primary motivation, this work studies the importance of proper surface passivation during the integration process by intentionally introducing the imperfect Si/GaAs interface to reveal the degradation mechanism at the nano and the atomic scales. ~~Then,~~ The atomic level oxygen distribution and the degree of oxygen content in Si NM and GaAs were carefully investigated using atom probe tomography (APT) and X-ray photoelectron spectroscopy (XPS) to trace changes in chemical composition and reactional mechanism across the UO interface when the surface of Si NM is exposed in air for different periods of time. Interestingly, it was found that a substantial amount of oxygen atoms ~~were~~ diffused from the Si native oxide layer and Al₂O₃ UO layer to the GaAs side and formed a 3 ~ 4 nm thick oxidized GaAs (GaAsO) layer. This thick native oxide layer also deteriorated the thermal properties of the Si/GaAs structure. The thermal boundary conductance across the Si-Al₂O₃-GaAs structure decreased by 12% when two different oxidized samples were measured and compared.

Result and Discussion

Figure 1(a) shows a schematic illustration of the sample preparation steps to create the Al₂O₃-interfaced Si/GaAs heterojunction with the Si NM having a native oxide layer. Details of the fabrication process can be found in the methods section. It is noted that various native oxide-free UO-interfaced heterojunctions can be found elsewhere. ^[16] In brief, the fabrication starts with the Si nanomembrane (NM) preparation. As shown in **Figure 1(a1)**, a top 50 ~ 70 nm Si device layer in insulator (SOI) substrate was partially doped by boron implantation to create the p⁺/p- structure that helps to form Ohmic contact later. After the doping process, the entire top Si layer was patterned and immersed in hydrofluoric (HF) acid to wet etch the buried SiO₂ layer (**Figure 1(a2)**). Once the buried SiO₂ layer was completely etched, the released top

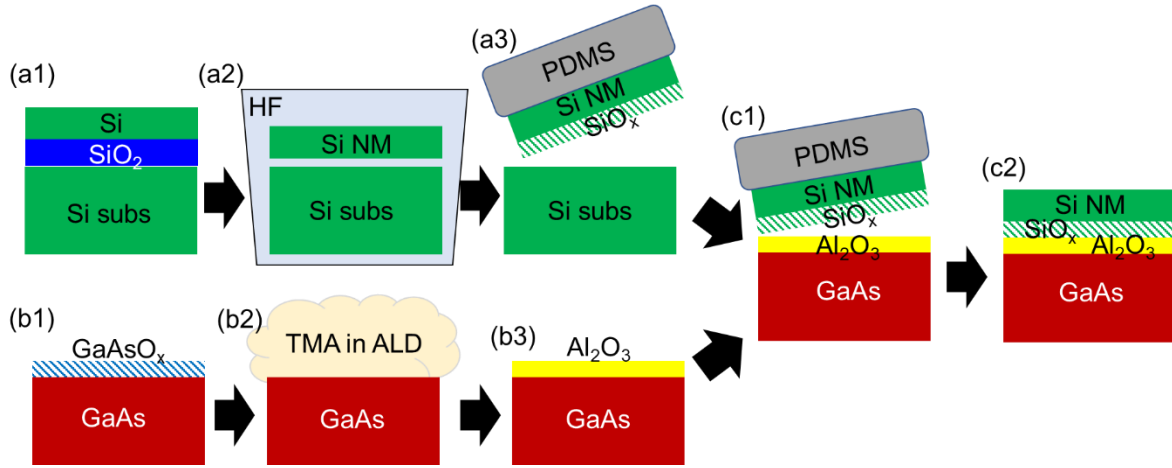


Figure 1. The schematic illustration of the sample preparation steps to create an Al_2O_3 -interfaced Si/GaAs heterojunction with native oxide on the Si NM side, (a1)-(a3) a creation of Si NM from the SOI host wafer and expose Si NM to air for different time periods, (b1)-(b3) an Al_2O_3 UO layer deposition on GaAs epitaxy substrate with native oxide removal process, (c1)-(c2) Si/GaAs heterogeneous integration via a micro-transfer printing method.

Si layer (now called Si NMs) was picked up using an elastomeric polydimethylsiloxane (PDMS) stamp, as shown in **Figure 1(a3)**. In this step, the Si NMs were exposed for two different time periods; 3 min and 10 mins prior to the following integration process. Meanwhile, a thin 0.7 nm of Al_2O_3 layer was deposited as a UO layer on the n-/n+ GaAs substrate using atomic layer deposition (ALD) as shown in **Figure 1(b1)-(b3)**. Prior to the Al_2O_3 deposition, 20 cycles of pre-purging with TMA precursor were performed on the n-GaAs substrate to remove native oxide from the GaAs surface. (**Figure 1(b2)**) The oxidized p+/p- Si NMs were gently transfer-printed onto the Al_2O_3 coated n-/n+ GaAs substrate using a PDMS stamp as shown in **Figure 1(c1)** followed by thermal annealing at 300 °C for 5 min using a rapid thermal annealing (RTA) system to enhance the bonding strength.

Prior to the device characterization, we performed various material and structure-property investigations. The optical microscope image shown in **Figure 2(a)** confirms that no visual defect sites, mechanical cracks, or fractures were found on Si NM. The uniform pink color of the Si NM implies that the transfer-printed Si NM was bonded uniformly to the Al_2O_3 coated GaAs surface. **Figure 2(b)** shows a scanning electron microscope (SEM) image of the

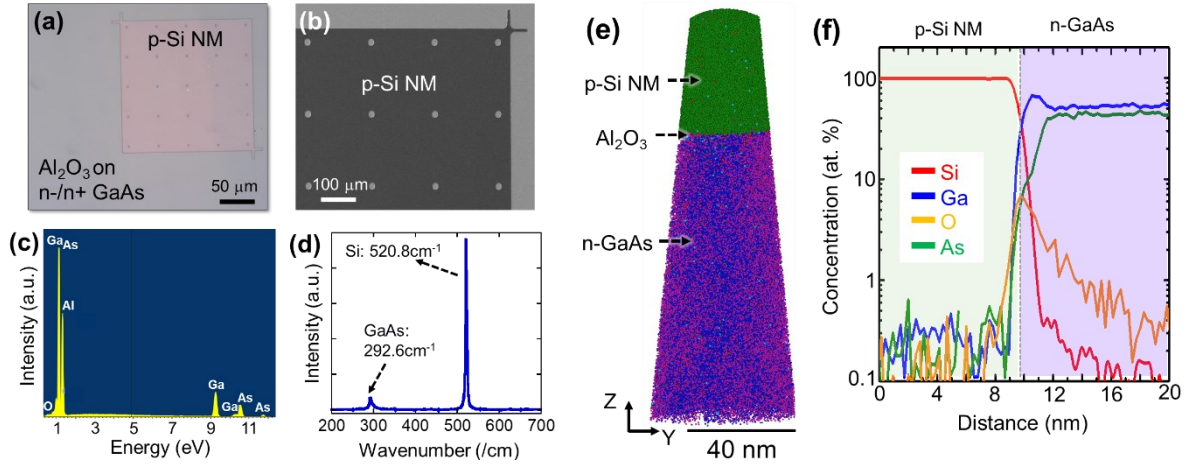


Figure 2. (a) Optical microscopic and (b) Scanning electron microscopic image of transferred Si NM on the Al₂O₃ coated GaAs substrate. (c) EDX spectrum taken from the Al₂O₃ coated GaAs substrate, (d) Raman spectrum taken from the transferred Si NM on the Al₂O₃ coated GaAs substrate, (e) 3D APT image taken from ± 50 nm at the Si/GaAs heterointerface, (f) Atom concentration (Si, Ga, O, As) as a function of distance taken from APT.

transfer-printed Si NM on the Al₂O₃-coated GaAs substrate. The elemental composition analysis captured by energy-dispersive X-ray spectroscopy (EDS), shown in **Figure 2(c)**, indicates a particle-free, clean Si NM and Al₂O₃-coated GaAs substrate. Raman spectroscopy was carried out to investigate the strain from the Si/GaAs heterostructure that could have been induced during a transfer-printing or thermal annealing process. **Figure 2(d)** presents the Raman spectrum taken from the center of the Si/GaAs heterostructure. Raman modes at 292.6 cm⁻¹ for GaAs and 520.8 cm⁻¹ for Si confirm that the Si/GaAs heterostructure does not experience any strain. Although the surface of the Si NM layer in the Si/GaAs heterostructure was exposed in air for 10 min prior to the NM transfer to oxidize the surface, the presence of native oxide on the Si NM surface was not detected by Raman spectroscopy, thus it was not possible to quantify the degree of the surface oxidation on Si NM. We speculated that a few nanometer thin SiO_x native oxide inside of the Si/GaAs heterostructure produced an insufficient level of Raman signal. Therefore, the Si/GaAs heterointerface was analyzed using APT as shown in **Figure 2(e)**. APT provides atomic-level information on defects and chemistry not only from the bulk but also at the buried interface, which is critically useful for examining

interfacial chemistry and impurities.^[24] **Figure 2(e)** shows a three-dimensional atomic map of the Si/GaAs heterostructure revealing the presence of a thin Al₂O₃ layer sandwiched between the Si (green dots) and GaAs (purple and blue dots). The atomic concentration of each element with respect to depth is shown as a 1D concentration profile in **Figure 2(f)**. Several important aspects of the Si/GaAs heterostructure can be observed here. Firstly, the abrupt reduction in As concentration and increase in Ga concentration near the Al₂O₃/GaAs were found. This concentration changes together with the long oxygen profile tail toward GaAs implies that oxygen atoms diffused from SiO_x and Al₂O₃ and formed GaO_x. At the same time, this chemical reaction pushes As ions inward, thus As ions become partially depleted in the first 3 ~ 4 nm, while some of the diffused oxygen atoms bonded with As (As-O). Previous studies on the Al₂O₃/GaAs structure also reported the movement of As ions from the Al₂O₃/GaAs interface due to oxidation.^[25] Also, oxygen diffusivity in GaAs is high (much higher than the diffusivity in Si), thus oxygen diffusion toward GaAs can occur at a lower energy,^[26] such as a low temperature annealing process, instead of toward the Si side.

Figure 3 presents a more systematic analysis of the Si/GaAs heterointerfaces with different Si oxidation times (i.e., 3 min and 10 min in the air). **Figure 3(a)** shows the oxygen profile that was extracted from the APT results for two differently oxidized samples. As expected, the oxygen diffusion length to GaAs estimated using a full-width half maximum (FWHM) was measured to be ~1 nm for 3 min oxidized Si NM sample, but this value increased to 3 ~ 4 nm for 10 min oxidized Si NM sample. The XPS spectra shown in **Figure 3(b) and (c)** also confirmed the presence of small oxygen atoms on both sides of the heterointerface, namely the Si-O bond from the Si/Al₂O₃ side and the As-O bond from the Al₂O₃/GaAs side. Interestingly, the XPS spectra show that a strong Si-O bond and As-O bond were formed when Si NM was exposed to air for 10 min. However, when Si NM was exposed to air for 3 min, a nearly unnoticeably small Al-O bond signal was found, while the Si-O bond was sufficiently strong. Such difference in the As-O bond is probably attributed to the development of native

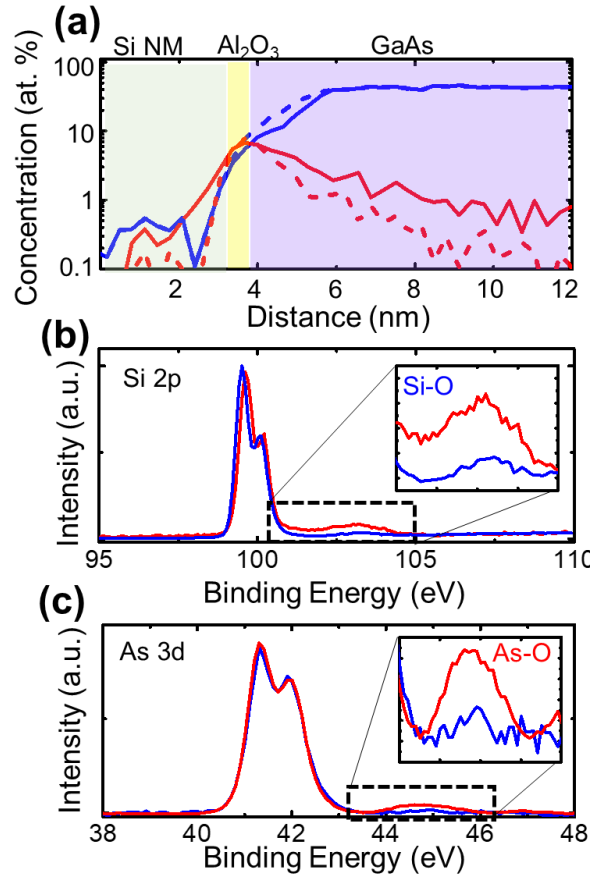


Figure 3. (a) Oxygen (red) and As (blue) concentration as a function of distance taken from APT. The dashed line and the solid line indicate samples with different Si NMs that were oxidized for 3 min and 10 min, respectively (b), (c) XPS spectra showing Si_{2p} and As_{3d} binding energies for samples with different Si NMs that were oxidized for 3 min (blue) and 10 min (red). Insets show the zoom-in of the Si-O bond region and As-O bond region, respectively.

oxide on Si NM surface, because as is known, it takes about 15 ~ 20 min to complete the surface oxidation for Si, therefore, 3min and 10 min of oxidation on the Si NM surface may produce a different amount (thickness) of incomplete native oxide.

As described in the method section, the Si/GaAs heterostructure ~~is~~ consists of four differently doped layers. The GaAs substrate has n-/n+ epitaxy layers-and the Si NM has a p+/p-layer formed by ion implantation. Therefore, the Si-GaAs heterointerface has a lightly doped p-n junction whose Fermi levels are expected to be 0.27 eV for Si and 0.14 eV for GaAs, respectively. In the ideal Si/GaAs heterojunction, the built-in potential (V_{bi}) would be 0.7 eV from $\{4.05 \text{ eV } (\chi_{Si}) + 1.12 \text{ eV } (E_{g,Si}) - 0.27 (E_F)\} - \{4.07 \text{ eV } (\chi_{GaAs}) + 0.14 (E_F)\}$, however, the

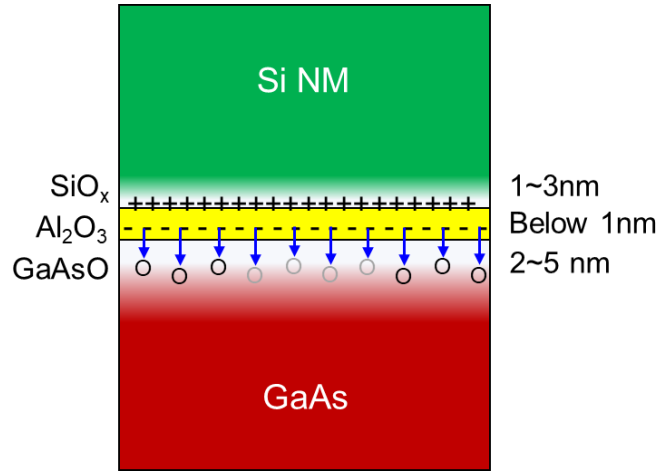


Figure 4. A cross-sectional illustration of the induced charges at the Si/GaAs interface.

V_{bi} from the $1/C^2$ -V curve was measured to be 0.59 eV, as shown in **Figure S1**, which is a direct evidence of some Fermi-level pinning at the interface. Given these results, it is possible to draw a chemical reaction across the Si/GaAs heterointerface as shown in **Figure 4**.

Figure 5 presents the measured D_{it} from Si/GaAs heterostructures with Si NMs that were oxidized for 3 min and 10 min. D_{it} values increased from 5.4×10^{12} states/cm²-eV to 1.2×10^{13} states/cm²-eV when Si NMs were oxidized for 3min and 10 min, respectively. Also, the variation of D_{it} values became wider as the Si NMs were oxidized longer. Compared with the D_{it} of the ideal Si/GaAs heterojunction shown in Ref 16, these D_{it} values were severely higher and their distributions were wider. This trend can be explained by uneven native oxide

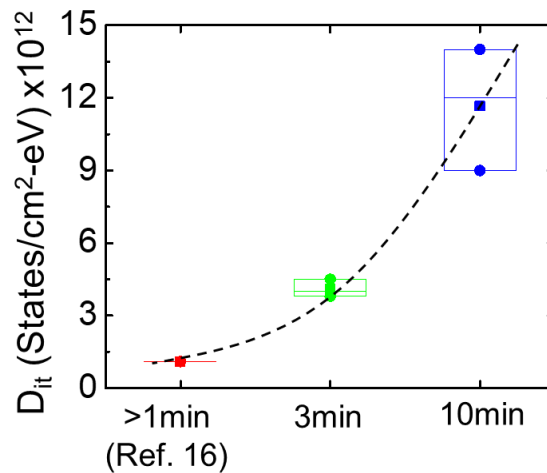


Figure 5. Measured interface defect density (D_{it}) taken from Si/GaAs heterostructures with Si NMs that were oxidized for 3 min and 10 min and compared these values with the ideal case from Ref. 16.

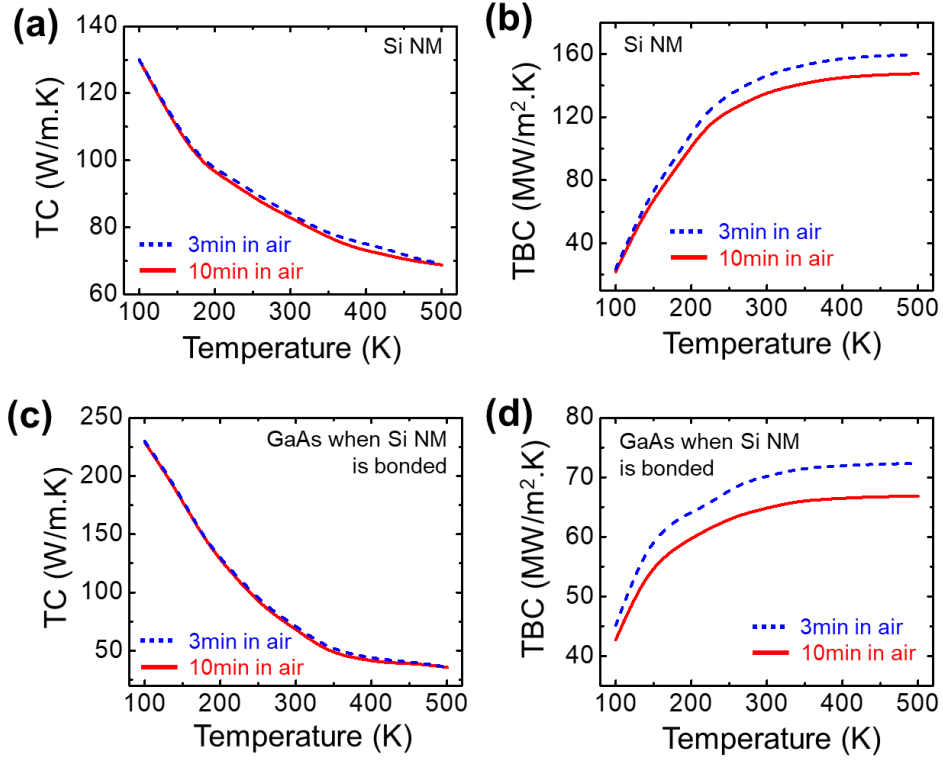


Figure 6. Measured thermal conductivity of (a) Si NM and (c) GaAs when they are bonded with Si NMs that were oxidized for 3 min (blue dashed line) and 10 min (red solid line) and thermal boundary conductance of (b) Si NM and (d) GaAs when they are bonded with Si NMs that were oxidized for 3 min (blue dashed line) and 10 min (red solid line) from 100 K to 500 K with 40 K intervals.

thicknesses in Si NM and GaAs surfaces. Unlike the thin-films grown by an epitaxy growth method, the oxidation process occurred at random locations, thus the thickness of the native oxide layer can vary by up to 50 %.^[27] The uneven oxide thicknesses in Si NM and GaAs lead to uneven charge distributions, thus causing wide variation in D_{it} . When widely distributed D_{it} values were observed, it is a direct evidence of the presence of a native oxide, thus the transport property across the heterojunction can be degraded.

In fact, when a stack of native oxides is presented at the heterointerface, a phonon transport is also deteriorated, because native oxides typically have numbers of dangling bonds that effectively shorten a phonon mean free path. To investigate changes in the thermal properties of Si/GaAs heterostructures, Raman thermometry was employed to extract thermal conductivity and thermal boundary conductance under a wide range of temperature conditions (from 100 K to 500 K with 40 K intervals). As shown in Ref 28, 29, and **Figure S2**, these

thermal property values can be directly extracted from the Raman shifting as a function of different temperature conditions.^[28,29] As shown in **Figure 6(a) and (b)**, the thermal conductivity (TC) of Si was measured to be 129.9 W/m·K and 128.2 W/m·K at 100 K for Si NM with 3 min and 10 min oxidation, respectively and gradually decreased to 82.9 W/m·K and 81.7 W/m·K at room temperature. The TC of GaAs showed a similar trend: 228.9 W/m·K and 227.7 W/m·K at 100 K for Si NM with 3 min and 10 min oxidation, respectively and gradually decreased to 68.5 W/m·K and 67.4 W/m·K at room temperature. This trend can be explained by the phonon–phonon scattering rate being sensitive to temperature because fewer states are occupied.

Unlike TC values, the thermal boundary conductance (TBC) value which measures the conductivity of phonon transport across the interface varied noticeably. The TBC of Si/Al₂O₃ at room temperature was measured to be 147 MW/(m²·K) and 147 MW/(m²·K) for Si NM with 3 min and 10 min of oxidation, respectively and Al₂O₃/GaAs to be 70.2 MW/(m²·K) and 70.2 MW/(m²·K) for the samples with 3 min and 10 min oxidized Si NMs, respectively. Such a different result in TC and TBC can be explained by the nature of TBC whose value is sensitive to the interface quality—namely a lower surface state at the interface reduces phonon transmission across the heterointerface, thus a higher TBC can be obtained.^[30] On the other hand, TB represents the bulk thermal property which indicates that the bulk properties of Si and GaAs remained unchanged. Therefore, the low TBC values imply that the phonon transport across the UO heterointerface was severely degraded by the stack of oxide layers.

Conclusions

In conclusion, the structural, electronic, and thermal transport properties of Al₂O₃-interfaced Si/GaAs heterostructures with the presence of native SiO₂ has been systematically investigated. Si NMs were oxidized for different time periods prior to the hetero-integration process to create the non-ideal single-side passivated Si/GaAs heterostructure. The atomic level

oxygen distribution and the degree of oxygen content in Si NM and GaAs were carefully investigated using APT and XPS to trace the changes in chemical composition and reactional mechanisms across the UO interface when Si NM surface was exposed to air for different periods of time. The negatively induced charges at the UO layer caused oxygen to diffuse to the GaAs layer and formed the unwanted GaAs oxide (GaAsO_x) layer. This native oxide stack noticeably degraded the thermal properties of the Si/GaAs heterostructure as Si NMs became more oxidized. Such a thick oxide stack at the heterointerface causes the following issues: (i) The generation of unwanted surface states from the presence of SiO_x and GaAsO_x , thus resulting in poor D_{it} values and tunneling efficiency, (ii) Uneven D_{it} variation across the surface due to the uneven oxide thicknesses in the Si NM and GaAs surface, (iii) Unreliable electrical and thermal behavior due to the presence of a thick oxide stack. (iv) More importantly, this study revealed that poor surface passivation on a one side of the heterointerface leads to two-sided oxidation, thus severely deteriorating the transport properties across the heterojunction that is formed by the UO layer. Therefore, this study clearly demonstrates that for semiconductor grafting-related heterogeneous heterojunction fabrications that involve GaAs, maintaining native oxide-free conditions at the interface is essential and critical to achieving epitaxy-like heterojunctions.

Experimental Section

p-Si/n-GaAs hetero-diode fabrication: The fabrication started with the boron ion implantation onto the SOI wafer. A top 50 nm ~ 70 nm Si device layer in insulator (SOI) substrate was partially doped by the boron implantation to achieve $1 \times 10^{20} \text{ cm}^{-3}$ of boron concentration to create p⁺/p- structure that helps to form Ohmic contact.^[31] A 500 μm x 500 μm sized Si NMs were patterned by a photolithography and defined using a reactive ion etcher (RIE) using SF_6/O_2 gases. A diluted HF: DI water (1:3) solution was used to etch a buried oxide layer of the SOI wafer for 7 hours in order to separate top p⁺/p- Si NM from the SOI wafer. The n⁺/n- GaAs

wafers which have a 500 nm thick heavily Si-doped ($5.8 \times 10^{18} \text{ cm}^{-3}$) n+ layer and a 500 nm thick lightly Si-doped ($1 \times 10^{16} \text{ cm}^{-3}$) n- layer were grown by metalorganic vapor phase epitaxy (MOVPE) using an Aixtron 3×2-inch close coupled showerhead reactor. After the cleaning process, the Al₂O₃ UO interfacial layer was deposited using an atomic layer deposition (ALD) system at 300 °C. The thickness of deposited Al₂O₃ was calibrated using ellipsometry, and it was found that the deposition rate was 1 angstrom per cycle. Prior to the Al₂O₃ deposition, 20 cycles of pre-purging with trimethylaluminum (TMA) precursor were performed on the n-GaAs substrate to remove a native oxide from the GaAs surface. The released Si NMs were picked up and transfer-printed onto a Al₂O₃ coated GaAs substrate using an elastomeric stamp (PDMS, Polydimethylsiloxane), followed by mild annealing (300 °C for 3 min) using rapid thermal annealing (RTA) to enhance the bonding strength. A cathode metal of Pd(30nm)/Ge(40nm)/Au(100nm) and an anode metal of Ti(10nm)/Au(150nm) were deposited on n-GaAs and p-Si side to finish the diode fabrication.

X-ray photoelectron spectroscopy (XPS) measurement: A Kratos Axis system with a monochromated Al-K α (energy of 1486.7 eV) X-ray source was used to capture the different core level (CL) spectra. The CL binding energy and valence band binding energy spectra of Si (2p), Al (2p), and As (3d) were collected with a pass energy of 26 eV and an exit angle of 45°. The center of the peak width was considered to be a CL binding energy position of each spectrum.

Atom probe tomography (APT) sample preparation: APT samples were prepared in an FEI Dual Beam 875 focused ion beam (FIB) through the standard wedge lift-out technique,^[32] followed by annular milling to create sharp needle-like tips with an end radius less than 100 nm. APT acquisitions were carried out in a CAMECA, Inc. Local Electrode Atom Probe (LEAP®) 5000XR, equipped with a reflectron lens and ultraviolet ($\lambda = 355 \text{ nm}$) laser pulsing capabilities. The APT analysis conditions consisted of 50 K base temperature, 5 pJ pulse energy,

0.3-2.0% detection rate, and 120-200 kHz pulse frequency. The Si-GaAs sample displayed in this work is a representative sample.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

Acknowledgments

This work was supported by the National Science Foundation (Grant number: ECCS- 1809077) and partially by the seed grant by Research and Education in energy, Environment, and Water (RENEW) Institute at the University at Buffalo.

Received: ((will be filled in by the editorial staff))

Revised: ((will be filled in by the editorial staff))

Published online: ((will be filled in by the editorial staff))

References

- [1] T. Kazior, J. LaRoche, D. Lubyshev, J. Fastenau, W. Liu, M. Urteaga, W. Ha, J. Bergman, M. Choe, M. Bulsara, presented at 2009 IEEE MTT-S International Microwave Symposium Digest **2009**.
- [2] K. H. Lee, S. Bao, D. Kohen, C. C. Huang, K. E. K. Lee, E. Fitzgerald, C. S. Tan, presented at 2015 IEEE 65th Electronic Components and Technology Conference (ECTC) **2015**.
- [3] D. Liu, S. J. Cho, J. Park, J. Gong, J.-H. Seo, R. Dalmau, D. Zhao, K. Kim, M. Kim, A. R. Kalapala, *Applied Physics Letters* **2018**, 113, 011111.
- [4] H. Zhou, J.-H. Seo, D. M. Paskiewicz, Y. Zhu, G. K. Celler, P. M. Voyles, W. Zhou, M. G. Lagally, Z. Ma, *Scientific reports* **2013**, 3, 1.
- [5] H. Yang, D. Zhao, S. Chuwongin, J.-H. Seo, W. Yang, Y. Shuai, J. Berggren, M. Hammar, Z. Ma, W. Zhou, *Nature Photonics* **2012**, 6, 615.
- [6] O. Moutanabbir, U. Gösele, *Annual Review of Materials Research* **2010**, 40, 469.
- [7] J. E. Ayers, T. Kujofsa, P. Rago, J. Raphael, *Heteroepitaxy of semiconductors: theory, growth, and characterization*, CRC press, **2016**.
- [8] D. Pasquariello, K. Hjort, *IEEE Journal of Selected Topics in Quantum Electronics* **2002**, 8, 118.
- [9] K. Tanabe, K. Watanabe, Y. Arakawa, *Scientific reports* **2012**, 2, 349.
- [10] A. Tauzin, E. Lagoutte, T. Salvétat, J. Guelfucci, Y. Bogumilowicz, B. Imbert, F. Fournel, S. Reboh, F. P. Luce, C. Lecouvey, presented at AIP Conference Proceedings **2015**.
- [11] T. R. Chung, L. Yang, N. Hosoda, H. Takagi, T. Suga, *Applied surface science* **1997**, 117, 808.
- [12] J. Liang, S. Shimizu, S. Nishida, N. Shigekawa, M. Arai, *ECS Solid State Letters* **2015**, 4, Q55.
- [13] K. Derendorf, S. Essig, E. Oliva, V. Klinger, T. Roesener, S. P. Philipps, J. Benick, M. Hermle, M. Schachtner, G. Siefert, *IEEE Journal of Photovoltaics* **2013**, 3, 1423.
- [14] J. Liang, T. Miyazaki, M. Morimoto, S. Nishida, N. Watanabe, N. Shigekawa, *Applied Physics Express* **2013**, 6, 021801.
- [15] J. Liang, S. Masuya, S. Kim, T. Oishi, M. Kasu, N. Shigekawa, *Applied Physics Express* **2018**, 12, 016501.
- [16] D. Liu, S. J. Cho, J.-H. Seo, K. Kim, M. Kim, J. Shi, X. Yin, W. Choi, C. Zhang, J. Kim, *arXiv preprint arXiv:1812.10225* **2018**.
- [17] M. Kim, J.-H. Seo, U. Singiseti, Z. Ma, *Journal of Materials Chemistry C* **2017**, 5, 8338.
- [18] J.-H. Seo, E. Swinnich, Y.-Y. Zhang, M. Kim, *Materials Research Letters* **2020**, 8, 123.
- [19] Z. Ma, J.-H. Seo, US patent, 8,866,154, 2014.
- [20] D. Liu, S. J. Cho, J. Park, J.-H. Seo, R. Dalmau, D. Zhao, K. Kim, J. Gong, M. Kim, I.-K. Lee, *Applied Physics Letters* **2018**, 112, 081101.
- [21] S. J. Cho, D. Liu, A. Hardy, J. Kim, J. Gong, C. J. Herrera-Rodriguez, E. Swinnich, X. Konstantinou, G.-Y. Oh, D. G. Kim, *AIP Advances* **2020**, 10, 125226.
- [22] J. Gong, K. Lu, J. Kim, T.K. Ng, D. Kim, J. Zhou, D. Liu, J. Kim B. S. Ooi, Z. Ma, *Japanese Journal of Applied Physics* **2022**, 61, 011003.
- [23] M. Morita, T. Ohmi, E. Hasegawa, M. Kawakami, M. Ohwada, *Journal of Applied Physics* **1990**, 68, 1272.
- [24] B. Mazumder, J. Sarker, *Journal of Materials Research*, **2021**, 36, 52–69.
- [25] V. M. Mikoushkin, A. P. Solonitsyna, E. A. Makarevskaya, D. A. Novikov, *Semiconductors* 2019, 53, 1918–1921.

- [26] S. M. Sze, Y. Li, K. K. Ng. *Physics of semiconductor devices*. John wiley & sons, **2021**.
- [27] Y. Tu, J. Tersoff, *Thin Solid Films*, **2001**, 400, 95–100.
- [28] M. N. Hasan, C. Li, J. Lai, J.-H. Seo, *Electronic Materials*, **2021**, 2(4) 495-503.
- [29] Y. Zheng, J.-H. Seo, *Nano Express* **2020**, 1, 030010.
- [30] Y. Zheng, E. Swinnich, J.-H. Seo, *ECS Journal of Solid State Science and Technology* **2020**, 9, 055007.
- [31] J.-H. Seo, K. Zhang, M. Kim, W. Zhou, Z. Ma, *NPJ Flexible Electronics* **2017**, 1, 1.
- [32] K. Thompson, D. Lawrence, D. Larson, J. Olson, T. Kelly, B. Gorman, *Ultramicroscopy* **2007**, 107, 131.