

Constant Switch Stress Control of Hybrid Switched Capacitor DC-DC Converters

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Abstract—This work proposes the constant switch stress (CSS) control algorithm to achieve both active balance and output regulation for hybrid switched capacitor (SC) DC-DC converters. CSS control is a hysteresis-based solution that highlights simple implementation and fast transient response. Discontinuous conduction mode (DCM) is possible at light load to reduce the switching loss. Another unique operation mode (CSS mode) protects semiconductor devices from overstress at heavy load. For load levels in between, pseudo constant switching frequency can be maintained by dynamically adjusting the hysteresis window. The performance of CSS control is validated on a 5-level flying capacitor multilevel (FCML) converter prototype.

Index Terms—DC-DC converter, hybrid switched capacitor, capacitor voltage balance, hysteretic control

I. INTRODUCTION

While commonly used in step-down DC-DC power conversion, buck converters suffer from relatively poor active- and passive-component utilization [1]–[4] and low power-density of inductors, especially at small size [5]. At high step-down ratios, short duty-cycle pulse widths also complicate gate driving and timing of the control loop. As an alternative, switched capacitor (SC) converters use capacitors for energy storage and show better performance in size-constrained applications [6]. However, the intrinsic charge sharing introduces extra loss, and implementing output regulation impacts tradeoffs between efficiency and power-density [7].

Hybrid SC converters, which combine inductor(s) with SC networks, can achieve higher energy density than buck and better regulation characteristics than pure SC converters [2]–[4]. This work focuses on a category of hybrid SC, so called *direct-conversion* topologies [7], which feature a single inductor

connecting the SC network to the output node, as shown in Fig. 1. The exemplary 2:1 SC can be replaced by more complex networks, such as Dickson, series-parallel, Fibonacci, etc., to form their hybrid version [2]. Although showing promising performance, maintaining flying capacitor voltage balance is challenging, especially for direct topologies [7]–[9]. Flying capacitors have a nominal (balanced) DC voltage in ideal operation, but voltage deviation (imbalance) can result from non-idealities or even be intrinsic to certain topologies [8]–[12]. The imbalance leads to increased ripple quantities and higher switch voltage stress, therefore, active balancing control is often required for such converters [13]–[21].

Various control methods have been developed to regulate the voltage on flying capacitors. Current mode control achieves balance by aligning the inductor valley or peak current [14], with its variations further improving the light-load stability and transient response [16], [17]. However, high-bandwidth inductor current sensing is often difficult due to challenges in instrumentation. Although it was shown in [18] that balance can be achieved by only sensing the inductor current ripple, it still requires accurate zero crossing detection and peak/valley current matching. Voltage mode algorithms were explored to eliminate the need for current sensing. Phase-shift control balances flying capacitors by adjusting the phase of PWM signals [19], but it requires digital PID compensation and has only been demonstrated on a 3-level converter. Modified ripple injection control can potentially be used in multiple hybrid SC topologies [20], [21], but it leads to variable switching frequency and is only applicable to integrated designs due to complexity of instrumentation.

This paper proposes a new voltage mode scheme, constant switch stress (CSS) control, to achieve both active balance and output regulation. Featuring simple implementation, CSS control is a hysteresis-based algorithm, where only two comparators and a digital logic circuit (here, implemented in an FPGA) are needed for the basic function. More components can be included to further improve the performance. For example, with a zero crossing detector (ZCD), DCM operation can be achieved to reduce the switching loss at light load; with a digital to analog converter (DAC), the hysteresis window can be dynamically adjusted to maintain stable switching frequency across a wide load range. Additionally, the unique CSS operation mode protects semiconductor devices from

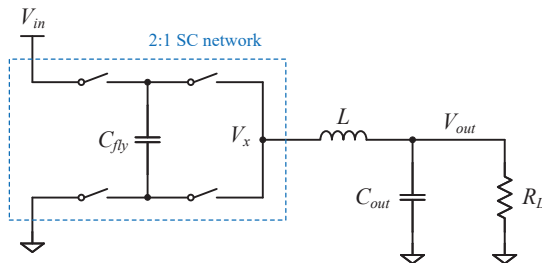


Fig. 1. A direct hybrid SC converter where the inductor connects the 2:1 SC network and the output node.

overstress at heavy load. CSS control only requires sensing the switching node voltage (marked by V_x in Fig. 1) and output voltage thus is applicable to all *direct* hybrid SC topologies. The rest of this paper is organized as follows: section II introduces the motivation and general principle of CSS control; section III explains the practical hardware implementation as well as error analysis; section IV reports the experimental results and section V concludes this work.

II. CONTROL PRINCIPLE

Pure SC converters are always balanced since the voltage on flying capacitors are directly constrained by Kirchhoff's voltage law (KVL). In hybrid SC converters, the same constraints can be duplicated by regulating the switching node voltage, V_x , in certain switching states. To illustrate this concept, the example in Fig. 1 is examined more closely. If V_{out} is below $V_{in}/2$, there are 4 switching states ($\varphi_1 - \varphi_4$) in a period: the switching node is connected to ground in φ_2 and φ_4 ; the equivalent circuits in φ_1 and φ_3 are shown in Fig. 2. If V_x is somehow regulated to $V_{in}/2$ in both φ_1 and φ_3 , from inspection, the flying capacitor voltage has to be $V_{in}/2$ as well, meaning that balance is automatically achieved. This conclusion is also true for more complex topologies. The rest of this section provides a universal and rigorous proof.

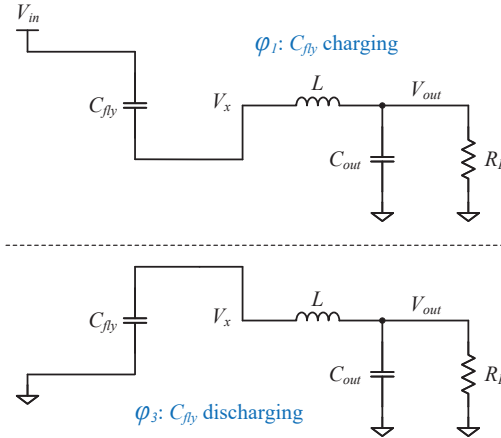


Fig. 2. Equivaent circuits of the 2:1 hybrid SC converter during φ_1 and φ_3 .

The flying capacitor multilevel (FCML) topology belongs to the direct hybrid SC family and features no parallel flying capacitor networks in any switching state. This eliminates charge sharing even with mismatched flying capacitance but also makes balancing especially challenging. To investigate the relationship between V_x regulation and active balance, a 5-level FCML converter will be used as an example with its schematic shown in Fig. 3.

Similar to the previous 2:1 hybrid SC case, the switches configure flying capacitors into different connections over a period, resulting in multiple switching states. When V_{out} is below $V_{in}/4$, flying capacitor connection in each state along with the state diagram are visualized in Fig. 4. These states

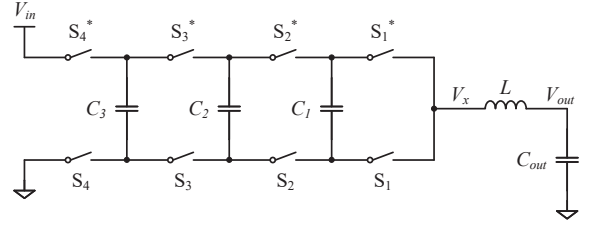


Fig. 3. Schematic of a 5-level FCML converter.

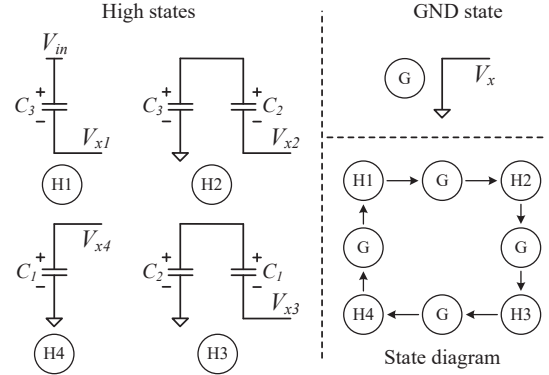


Fig. 4. Flying capacitor connection and state transition diagram of the 5-level FCML converter ($V_{out} < V_{in}/4$).

are classified into two categories: the *high* states ($H_1 - H_4$) where the switching node is connected to one or more flying capacitors, and the *GND* state (G) where the switching node is connected to ground. The high states govern the charge transfer of flying capacitors and will be the focus of active balancing analysis.

Illustrated in Fig. 5, in high state H_j ($j = 1, 2, 3, 4$): the switching node voltage is denoted as V_{xj} ; the initial and final time are defined as t_{ij} and t_{fj} , respectively. Referring to the capacitor connection in Fig. 4, in high state H_1 , for example, KVL can be applied at t_{i1} and t_{f1} :

$$V_{x1}(t_{i1}) = V_{in} - V_{C3}(t_{i1}), \quad (1)$$

$$V_{x1}(t_{f1}) = V_{in} - V_{C3}(t_{f1}). \quad (2)$$

Averaging (1) and (2) yields

$$\frac{V_{x1}(t_{i1}) + V_{x1}(t_{f1})}{2} = V_{in} - \frac{V_{C3}(t_{i1}) + V_{C3}(t_{f1})}{2}. \quad (3)$$

For simplicity of notation, the algebraic average of initial and final value is introduced:

$$\tilde{X} = \frac{X(t_{ij}) + X(t_{fj})}{2}, \quad (4)$$

where X is a general quantity which can represent the switching node voltage, flying capacitor voltage, etc. Hence,

$$\tilde{V}_{x1} = V_{in} - \tilde{V}_{C3}. \quad (5)$$

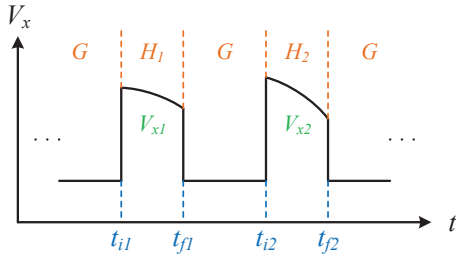


Fig. 5. Illustration of several notations using exemplary V_x waveform.

Similar relationships can be derived for other high states, H_2 , H_3 , H_4 , respectively:

$$\tilde{V}_{x2} = \tilde{V}_{C3} - \tilde{V}_{C2}, \quad (6)$$

$$\tilde{V}_{x3} = \tilde{V}_{C2} - \tilde{V}_{C1}, \quad (7)$$

$$\tilde{V}_{x4} = \tilde{V}_{C1}. \quad (8)$$

Equations (5)-(8) can be packed into matrix form:

$$\begin{bmatrix} \tilde{V}_{x1} \\ \tilde{V}_{x2} \\ \tilde{V}_{x3} \\ \tilde{V}_{x4} \end{bmatrix} = \begin{bmatrix} 0 & 0 & -1 \\ 0 & -1 & 1 \\ -1 & 1 & 0 \\ 1 & 0 & 0 \end{bmatrix} \begin{bmatrix} \tilde{V}_{C1} \\ \tilde{V}_{C2} \\ \tilde{V}_{C3} \end{bmatrix} + \begin{bmatrix} 1 \\ 0 \\ 0 \\ 0 \end{bmatrix} V_{in}, \quad (9)$$

or simply denoted as

$$\tilde{\mathbf{V}}_x = \mathbf{C} \cdot \tilde{\mathbf{V}}_C + \mathbf{W} \cdot V_{in}, \quad (10)$$

where $\tilde{\mathbf{V}}_x$ and $\tilde{\mathbf{V}}_C$ are vectors of the switching node voltage and flying capacitor voltage, respectively. Matrix $\mathbf{C}$ captures the flying capacitor connections in each high state.

It was shown in [10] that if the SC network is controllable (active balance is possible), Matrix $\mathbf{C}$ must be full-rank. An intuitive explanation is that flying capacitor connections in all high states have to be linearly independent to achieve voltage balance. Under this circumstance, $\tilde{\mathbf{V}}_C$ can be uniquely determined by solving (10):

$$\tilde{\mathbf{V}}_C = \mathbf{C}^\dagger \cdot (\tilde{\mathbf{V}}_x - \mathbf{W} \cdot V_{in}), \quad (11)$$

where $\mathbf{C}^\dagger$ is the pseudoinverse of matrix $\mathbf{C}$ (because it is not a square matrix and simple inverse cannot be applied). If the switching node voltage during high states is regulated to

$$\tilde{\mathbf{V}}_x = \begin{bmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \end{bmatrix}^T \cdot V_{in}, \quad (12)$$

the solution given by (11) is

$$\tilde{\mathbf{V}}_C = \begin{bmatrix} \frac{1}{4} & \frac{2}{4} & \frac{3}{4} \end{bmatrix}^T \cdot V_{in}, \quad (13)$$

which is the balanced voltage. In other words, regulating $\tilde{\mathbf{V}}_x$ to the correct value will force flying capacitors to balance. For a N -level FCML converter, this correct value is V_{in}/N . For other direct hybrid topologies (Dickson, series-parallel, Fibonacci, etc.), this value is given by the output voltage of their pure SC version. This important conclusion serves as the foundation of CSS control.

III. CONTROL FEATURE ANALYSIS

Although the previous conclusion provides a simple method to achieve active balance, regulation of $\tilde{\mathbf{V}}_x$ is not straightforward, as it depends on both the initial and final values of the switching node voltage. This section will explain the practical implementation as well as error analysis of CSS control.

A. Practical Implementation

Referring to Fig. 4, if the charge transfer during high state H_j is denoted as Q_j , the charge balance of C_1 would require $Q_3 = Q_4$, because it is charged in H_3 and discharged in H_4 . Eventually, the charge balance of all flying capacitors require:

$$Q_1 = Q_2 = Q_3 = Q_4. \quad (14)$$

Charge Q_j can be expressed as the voltage drop from initial to final moment on the switching node multiplies the equivalent flying capacitance:

$$Q_j = (V_{xj}(t_{ij}) - V_{xj}(t_{fj})) \cdot C_{eq,j}. \quad (15)$$

Assuming all flying capacitors have equal capacitance, C_{fly} (error caused by unequal capacitance will be analyzed later), observing Fig. 4 gives:

$$C_{eq,j} = \begin{cases} C_{fly}, & j = 1, 4 \\ C_{fly}/2, & j = 2, 3 \end{cases} \quad (16)$$

Substituting (15) and (16) into (14) yields

$$V_{xj}(t_{ij}) - V_{xj}(t_{fj}) = 2[V_{xk}(t_{ik}) - V_{xk}(t_{fk})], \quad (17)$$

where $j = 2, 3$ and $k = 1, 4$, indicating that voltage drop on the switching node during H_2 and H_3 are twice that of H_1 and H_4 because the equivalent flying capacitance is halved. Additionally, adding up (5)-(8) gives

$$\tilde{V}_{x1} + \tilde{V}_{x2} + \tilde{V}_{x3} + \tilde{V}_{x4} = V_{in}, \quad (18)$$

setting another constraint on the switching node voltage.

Illustrated in Fig. 6, in CSS control, a design variable ΔV is chosen and the final value of V_{xj} is regulated as below:

$$V_{xj}(t_{fj}) = \begin{cases} \frac{V_{in}}{4} - \Delta V, & j = 1, 4 \\ \frac{V_{in}}{4} - 2\Delta V, & j = 2, 3 \end{cases} \quad (19)$$

Solving (17)-(19) directly yields

$$\tilde{\mathbf{V}}_x = \begin{bmatrix} \frac{1}{4} & \frac{1}{4} & \frac{1}{4} & \frac{1}{4} \end{bmatrix}^T \cdot V_{in}, \quad (20)$$

which forces the flying capacitors to balance, according to the conclusion in section II. As (17) and (18) are inherent to the topology, the controller only needs to realize (19) to achieve active balance.

A comparator-triggered controller is ideal to regulate the final value of V_{xj} . As shown in Fig. 7, the desired final value indicated by (19) is produced by subtracting ΔV or $2\Delta V$ from $V_{in}/4$, depending on which high state the converter is in. Once V_x reaches this value, a state transition from H_j

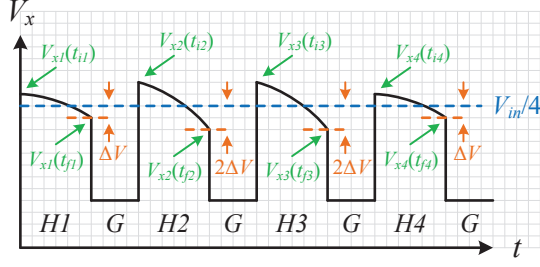


Fig. 6. Illustration of the switching node voltage waveform under CSS control.

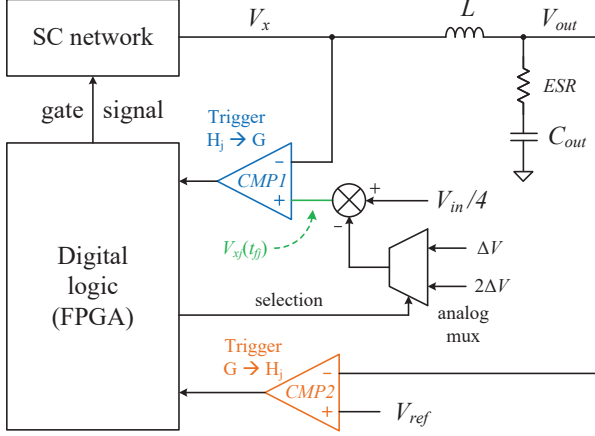


Fig. 7. Simplified diagram of CSS control.

to G is triggered by $CMP1$ so that V_{xj} is clamped at the desired final value, thus achieving active balance. The output voltage is regulated by a second loop, where V_{out} is compared against a reference voltage, V_{ref} . During the ground state G , once V_{out} falls to V_{ref} , a state transition from G to H_j is triggered by $CMP2$ to deliver more charge to the output. Note that a series resistance is added to the output bypass capacitor to compensate for the inductor current dynamics, which is a commonly used technique in hysteretic control.

B. Multi-mode Operation

The previous control diagram only includes basic function, but more features can be added to further improve the performance, resulting in multi-mode operation.

At light load, discontinuous conduction mode (DCM) can be implemented with a zero crossing detector (ZCD) to prevent negative inductor current and to reduce the switching loss. As shown in Fig. 8, during the ground state G , the ZCD senses the inductor current polarity by measuring the voltage drop across the switch on resistance, R_{on} (this representation is only an example here; many other ZCD schemes can be implemented in practice). Once the inductor current falls to zero, the converter transitions to the DCM state D , where the SC network presents high impedance and keeps the inductor current at zero. Similar to the basic operation, a high state H_j is triggered by $CMP2$ when V_{out} falls below V_{ref} .

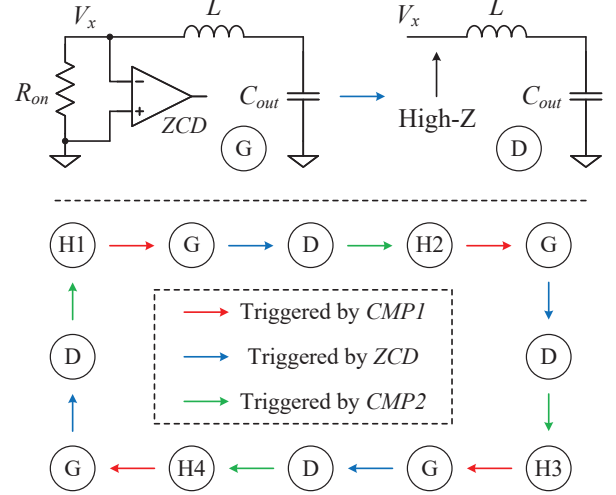


Fig. 8. Illustration of the DCM operation.

Before discussing other operation modes, the previously introduced design variable, ΔV , needs to be further analyzed, as it has three important roles: setting the final value of V_{xj} , governing the charge transfer during each high state H_j , and representing the maximum voltage stress on switches.

Referring to Fig. 6, the charge transfer in each high state, Q_j , can be expressed as

$$Q_j = 2C_{fly}\Delta V. \quad (21)$$

It can also be expressed in terms of the load current, I_{out} , and switching frequency, f_{sw} :

$$Q_j = \frac{I_{out}V_{out}}{f_{sw}V_{in}}. \quad (22)$$

Equating (21) and (22) yields

$$f_{sw} = \frac{I_{out}V_{out}}{2C_{fly}V_{in}\Delta V}. \quad (23)$$

If ΔV is a constant quantity, (23) shows that the switching frequency varies with operating conditions of the converter (V_{in} , V_{out} , I_{out}). In certain applications, a constant switching frequency may be preferred due to concerns on the electromagnetic interference (EMI), ripple, etc. Hence ΔV should be dynamically adjusted to maintain a relatively stable f_{sw} , as illustrated in Fig. 9.

In this work, the voltage $V_{in}/4$ is produced by a resistor divider followed by an analog buffer. A current-sinking DAC draws current from the $V_{in}/4$ node through a resistor R , creating a voltage drop proportional to the current and generating the desired final value of V_{xj} :

$$V_{xj}(t_{fj}) = \frac{V_{in}}{4} - I_{DAC}R. \quad (24)$$

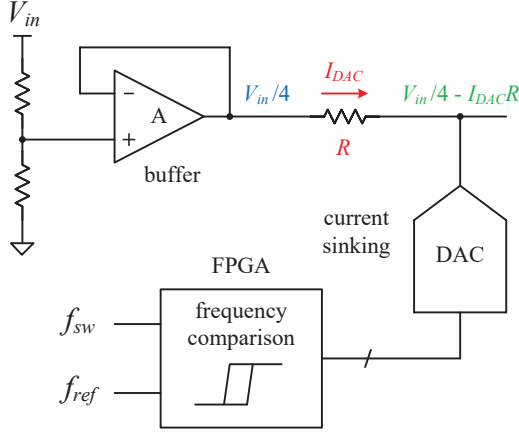


Fig. 9. ΔV is dynamically adjusted to maintain a relatively constant f_{sw} .

Comparing (24) and (19) gives:

$$I_{DAC} = \begin{cases} \frac{\Delta V}{R}, & j = 1, 4 \\ \frac{2\Delta V}{R}, & j = 2, 3 \end{cases} \quad (25)$$

indicating that I_{DAC} needs to be multiplied by 2 during H_2 and H_3 . The input of the DAC is controlled by the FPGA, where f_{sw} is compared against a reference frequency, f_{ref} . If f_{sw} is too high, the current I_{DAC} is increased, providing a larger ΔV . This action brings f_{sw} down according to (23). Similar negative feedback also works when f_{sw} is too low, and f_{sw} is kept relatively constant around f_{ref} . The operating mode where ΔV is dynamically adjusted is hereby named constant switching frequency (CSF) mode.

However, ΔV cannot be arbitrarily adjusted, because it is also related to the maximum voltage stress on switches. Fig. 10 shows the current conduction path during high state H_3 . Neglecting switch *on* resistance, the voltage stress on S_2 is equal to the switching node voltage, V_{x3} . Referring to Fig. 6, the maximum of this value is

$$V_{x3,max} = \frac{V_{in}}{4} + 2\Delta V. \quad (26)$$

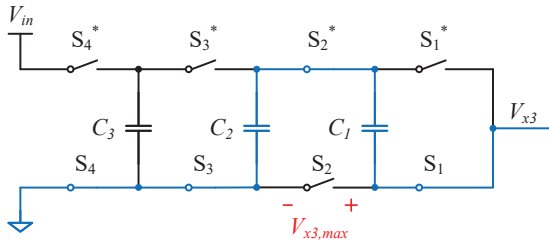


Fig. 10. Current conduction path in high state H_3 .

Therefore, ΔV has an upper limit:

$$\Delta V_{max} = \frac{V_{sw,max}}{2} - \frac{V_{in}}{8}, \quad (27)$$

where $V_{sw,max}$ stands for switch voltage rating (with some margin in practice). When ΔV is at ΔV_{max} , even if f_{sw} is still higher than f_{ref} , ΔV cannot be increased to bring down f_{sw} due to safety concerns. From another perspective, when the load current becomes too high, f_{sw} is allowed to exceed f_{ref} , since it is the only way to deliver the required current to the output without overstressing the switches. The operating mode where ΔV reaches maximum is hereby called constant switch stress (CSS) mode.

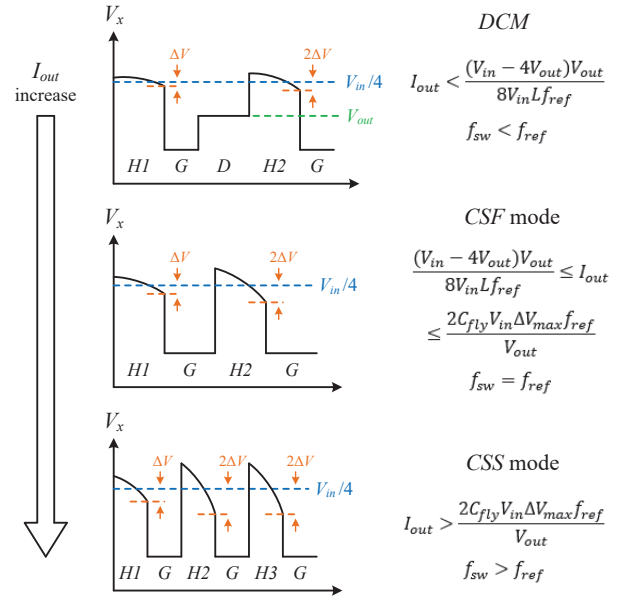


Fig. 11. Summary of multi-mode operation under CSS control.

Fig. 11 summarizes multi-mode operation of the converter under CSS control. At light load, DCM operation eliminates negative inductor current, reducing the switching frequency as well as the associated losses. At medium load, ΔV can be dynamically adjusted to maintain relatively constant switching frequency. At heavy load, the switching frequency is allowed to exceed f_{ref} to prevent switch overstress.

C. Error Analysis

The objectives of CSS control are active balance and output regulation. However, the accuracy of both may be affected by random error as well as systematic error.

The flying capacitors may not have the same capacitance because of mismatch and derating, invalidating (16). In the presence of comparator offset and loop delay, the actual final value of V_{xj} will also deviate from (19). These effects can be lumped together and modeled as an error term:

$$\tilde{V}_{x,e} = \tilde{V}_x - \tilde{V}_{x,0}, \quad (28)$$

where $\tilde{V}_{x,0}$ is the ideal portion given by (12), $\tilde{V}_{x,e}$ stands for the error caused by non-idealities. Referring to (11), the subsequent balancing error is

$$\tilde{V}_{C,e} = \frac{\partial \tilde{V}_C}{\partial \tilde{V}_x} \cdot \tilde{V}_{x,e} = C^\dagger \tilde{V}_{x,e}. \quad (29)$$

Here the *Euclidean norm* is used to quantify the magnitude of an error vector:

$$\|\tilde{V}_{x,e}\| = \sqrt{\tilde{V}_{x1,e}^2 + \tilde{V}_{x2,e}^2 + \tilde{V}_{x3,e}^2 + \tilde{V}_{x4,e}^2}. \quad (30)$$

According to attributes of the Euclidean norm,

$$\|\tilde{V}_{C,e}\| \leq \|C^\dagger\|_2 \cdot \|\tilde{V}_{x,e}\|, \quad (31)$$

where $\|C^\dagger\|_2$ represents the spectral norm of $C^\dagger$, which is about 1.31 for a 5-level FCML converter. The relationship in (31) determines the upper bound of the balancing error: for a small $\|\tilde{V}_{x,e}\|$, $\|\tilde{V}_{C,e}\|$ is comparably small.

Different from active balance, regulation of output voltage mainly suffers from systematic error. Pictured in Fig. 12, the error comes from the fact that V_{out} is regulated by a single-bounded hysteretic loop. Its DC value is defined by the lower bound, V_{ref} , and the ripple, ΔV_{out} :

$$V_{out,DC} = V_{ref} + \frac{\Delta V_{out}}{2}. \quad (32)$$

If C_{out} is sufficiently large,

$$\Delta V_{out} \approx \frac{(V_{in} - 4V_{out})V_{out}R_o}{4V_{in}Lf_{sw}}, \quad (33)$$

where R_o is the series resistance of the output capacitor. The DC error can be compensated by setting V_{ref} 'half a ripple' lower. However, during transients, excessive V_{out} overshoot may occur because there is not a well-defined upper bound. To solve this issue, another comparator, *CMP3*, is needed to detect such transients and override *CMP1* to trigger a ground state, but it should not be active in steady state operation. This treatment is shown in Fig. 13. It is interesting to notice that

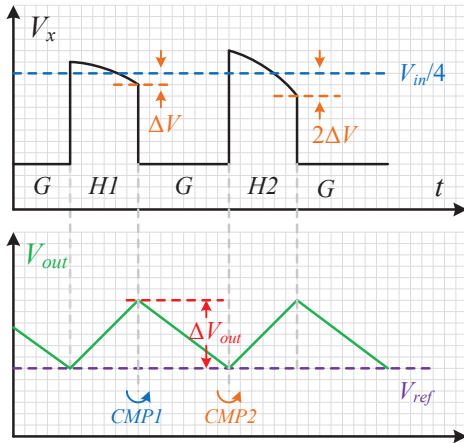


Fig. 12. Illustration of systematic error in V_{out} regulation.

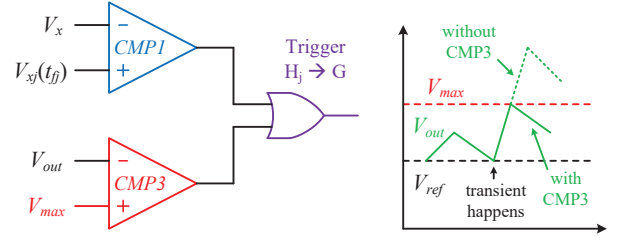


Fig. 13. Introducing *CMP3* to limit the maximum V_{out} overshoot.

CMP3 leads to a trade-off between active balance and output voltage regulation, which is left for future research.

IV. EXPERIMENTAL RESULTS

A 5-level FCML converter is built to test the performance of CSS control. Fig. 14 shows annotated photo of the board with a list of components used. The corresponding schematic with testing circuits is also shown in Fig. 15.

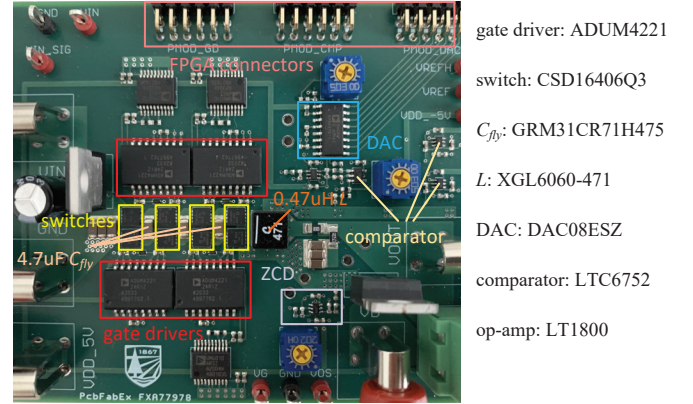


Fig. 14. Photo of the evaluation board with component list.

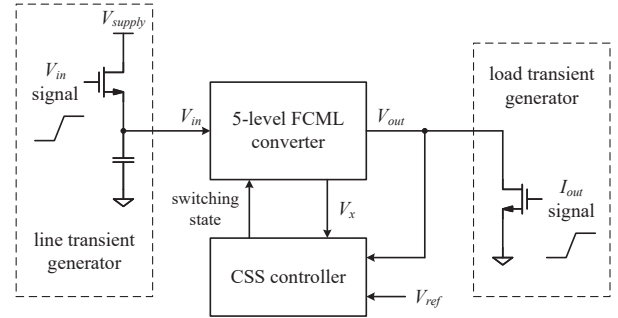


Fig. 15. Simplified schematic of the board with testing circuits.

Fig. 16 shows the oscilloscope measured steady state waveform in the basic operation (refer to Fig. 7). The waveform and the control diagram are consistent: the transition from a high state to the ground state is triggered by V_x reaching its

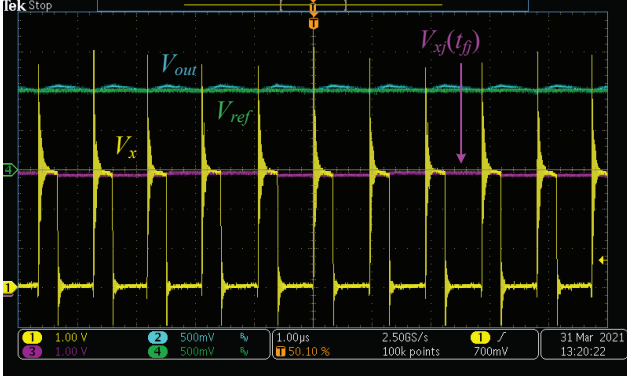


Fig. 16. Steady state waveform in basic operation (12V:1V).

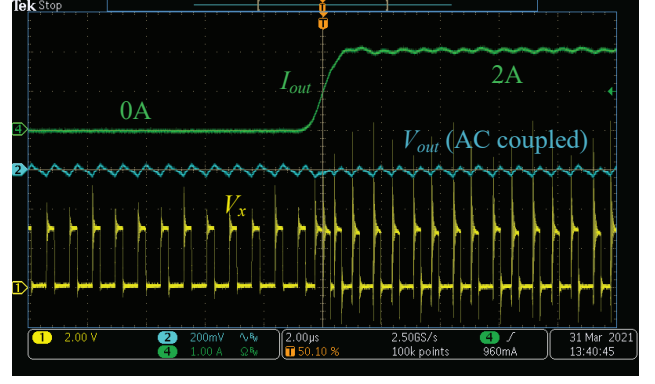


Fig. 18. Waveform in load transient test (I_{out} : 0 → 2A).

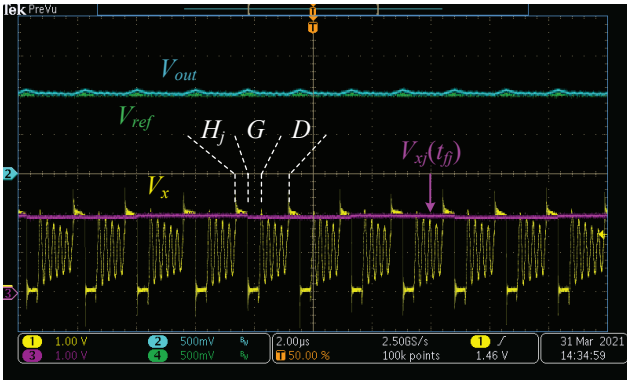


Fig. 17. Steady state waveform in DCM operation (8V:1V).

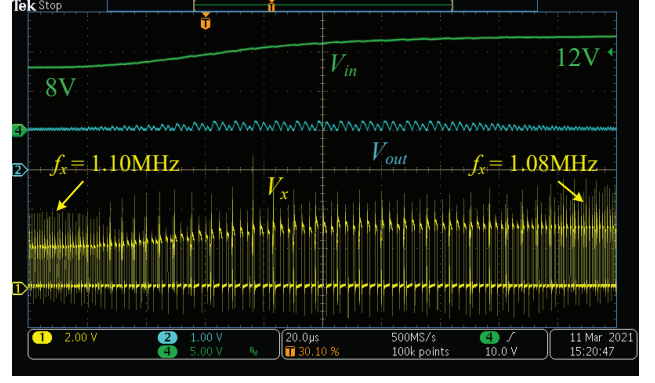


Fig. 19. Waveform in line transient test (V_{in} : 8V → 12V).

desired final value $V_{xj}(t_{fj})$ given by (19); the transition from the ground state to the next high state is triggered by V_{out} falling to V_{ref} . In this configuration, both active balance and output regulation are achieved only by two comparators and a digital logic on the FPGA.

The steady state waveform in DCM operation is measured. The DCM state, D , is triggered by the ZCD when inductor current falls to zero. Ideally V_x should be equal to V_{out} in this state, however, in practice, the residual inductor current and parasitic capacitance at the switching node cause oscillation, leading to the waveform shown in Fig. 17. From both V_{out} and V_x waveform, the three different states, H_j , G , and D can be clearly identified. The switching frequency is also reduced compared to the basic operation.

Fig. 18 shows the waveform in load transient test, where I_{out} changes from 0 to 2A within 2 μ s (1A/ μ s). During the transient, ground state G is shortened significantly to quickly ramp up the inductor current, which can be seen from the 3 consecutive pulses of V_x . Meanwhile, balance is maintained by regulating the final value of V_x . Additionally, no obvious undershoot is observed on V_{out} waveform.

Fig. 19 shows the result in line transient test, where V_{in} changes from 8V to 12V within 100 μ s (40V/ms). Balance is

maintained, however, as explained in section III-C, large V_{out} overshoot can occur due to the lack of a well-defined upper bound. In this test, the overshoot is limited to 200mV by a third comparator, $CMP3$. Lower tolerance of overshoot can be achieved, but at the price of slower balancing dynamics. It is also worth noticing that due to dynamic tuning of ΔV , the switching frequency remains roughly the same before and after the transient.

V. CONCLUSION

This paper presents CSS control, a novel voltage mode algorithm to achieve both active balance and output voltage regulation for hybrid SC converters. The control theory and characteristics are explained. Featuring fast transient response and simple implementation, the performance of CSS control is validated by the experiment on a 5-level FCML converter. The challenge of V_{out} overshoot is partly addressed, but still requires future attention.

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