

High-Frequency Resonant Switched-Capacitor Converters with Multi-Winding Current Ballasting: Analysis and Optimization

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Abstract—This work explores analysis and optimization of multi-winding current-ballasting in high-frequency coupled magnetic structures for direct-conversion resonant switched-capacitor (ReSC) DC-DC converters, a technique that can mitigate AC conduction losses, improving efficiency at high frequency. While past work has explored merged-LC resonators which combine capacitance and inductance into a single structure, here we show similar benefits can be achieved with separately lumped capacitors in direct-conversion ReSC topologies. We develop a state-space model to determine optimum per-winding current density profiles and show that such profiles can be achieved by presenting a unique (flying) capacitance to each winding in a multiphase ReSC architecture. A hardware prototype with planar air-core test structures is used for validation and also to explore practical limitations.

I. INTRODUCTION

Pervasive demands for higher levels of integration and smaller physical size have led to increasing switching frequencies of DC-DC and other power management circuits [1]–[6]. However, while passive component size can generally be reduced at higher frequencies, AC losses in magnetic components often limit the extent and viability of frequency, size, and power-density scaling [1]. In particular, for highly- and fully-integrated DC-DC converters which use air-core magnetics (and/or where core materials are impractical due to frequency and integration constraints [7]), strong AC current crowding effects can be a major source of loss which can impact both efficiency and power density [8]–[10].

This work explores methods to counteract or mitigate high-frequency winding losses with the goal of providing a roadmap to viable highly- or fully-integrated DC-DC converters; a particular emphasis is on air-core magnetics with spiral geometries, however other technologies and architectures may benefit from the approach. Illustrated conceptually in Fig. 1, we explore opportunities to leverage *current ballasting*: using a uniquely segmented capacitive impedance to force a desired (i.e. optimal) current density profile in the magnetic component winding structure. While similar current ballasting concepts have been described previously in [8]–[12], here we focus on the use of capacitive ballasting in ‘direct-conversion’ resonant switched-capacitor (ReSC) DC-DC converters.

The direct-conversion ReSC configuration, shown in Fig. 2, differs from ‘indirect-conversion’ or ‘tank’ ReSC converters in that inductor(s) are coupled between the SC stage and output node [13]–[17]. While behaviorally similar, the direct configuration has important differences related to the shape of the inductor current waveform, which is a unidirectional – always flowing to the output [15]. Direct topologies can operate in a

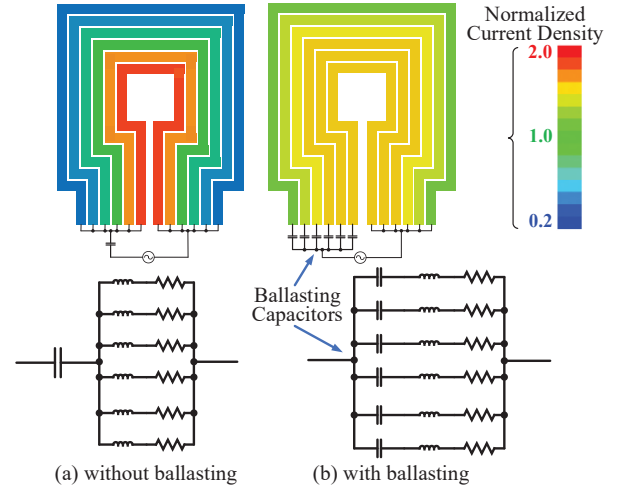


Fig. 1: Multi-trace spiral inductor w/o and w/ ballasting

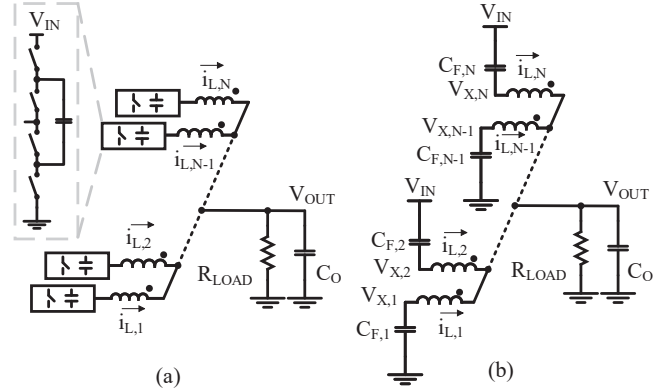


Fig. 2: (a) Example multiphase ReSC Converter. (b) Equivalent circuit of the converter in a given clock phase.

wider variety of operating modes including continuous conduction modes (CCM) above the nominal resonant frequency [16]. Due to separate SC and inductive stages, direct topologies are more straightforward to implement with discrete components and therefore more widely explored in the literature [17].

Here we develop a concise and accurate state space model of multi-winding strongly-coupled magnetic structures in which each winding can be independently ballasted by a unique capacitive impedance. In this paper we will: 1) use the state-space model to develop a simplified 2nd-order model which provides better insight and useful closed-form relationships for key circuit parameters; 2) prove that arbitrary (resonant) current ballasting can be achieved in these structures by tuning or fixing the unique capacitance presented to each winding; 3) illustrate

achievable benefits and also practical limitations of capacitive ballasting (and the model itself) using both simulation and measurement results.

II. GENERAL CURRENT BALLASTING CONCEPT

The current ballasting concept can be described by considering Fig. 1 which shows a single-turn planar-spiral inductor where a single wide trace is split into multiple (narrower) parallel traces. In Fig. 1(a), these traces are resonated with a single capacitance, effectively operating in parallel. At high frequency, oscillating magnetic fields induce eddy currents in the winding structure. With the highest flux density in the center of the spiral, and assuming the trace widths are small enough such that eddy-current effects within individual traces are minor (e.g. less than an effective skin-depth), these eddy-current effects reinforce current flow in the inner traces while counteracting current flow in outer traces.

Importantly, current crowding results in both a modest decrease in inductance at higher frequency and a potentially significant increase in conduction loss. Specifically, current crowding can result in poor utilization of the overall conductance of the trace segments with only a fraction of the winding area being used to conduct current. More specifically, these effects can cause the current density profile to deviate from an ‘optimal’ distribution. For example, it is shown later that trace currents would ideally follow a distribution that goes inversely with trace effective series resistance (ESR), matching the known optimization for multi-phase buck converters, i.e. [18].

In Fig. 1(b) each winding is presented with a unique capacitance, representing part of an overall capacitance used to resonate the structure. While magnetic-field-induced effects are still present at high frequencies, the unique capacitive impedances work to counteract undesired current crowding. For example, if a given trace is induced to have higher current, the voltage on the associated capacitor will increase, providing a ballasting (counteracting) effect. Here also, the benefit of splitting a single wide trace into multiple parallel traces is apparent: assuming the trace width is narrow enough such that induced eddy current effects do not cause appreciable current crowding within the trace, the scheme can alleviate both inter- and intra-trace current crowding; *such can be loosely described as counteracting both proximity and skin effects in the structure.*

While this explanation is somewhat simplified, in this paper we will describe this process in more detail with a quantitative treatment to identify exactly how to segment the capacitance in order to achieve a desired current or current density in the winding traces. As shown in Fig. 2, this configuration can be achieved by segmenting (interleaving) the flying capacitance of a generic resonant switched capacitor (ReSC) converter. While a nominally 2:1 ReSC converter is shown in Fig. 2(a), other direct-conversion topologies from those known in literature [11] could be used in a similar fashion. Here, one terminal of each trace is connected to a flying capacitor, while the other terminal is connected to the output. With the inductor split into N traces, the SC stages can be operated either in-phase or exactly out of phase with one another. As a result, we can obtain an equivalent circuit as shown in Fig 2(b); a further simplified perspective for a single ‘ m^{th} ’ trace is shown in Fig. 3.

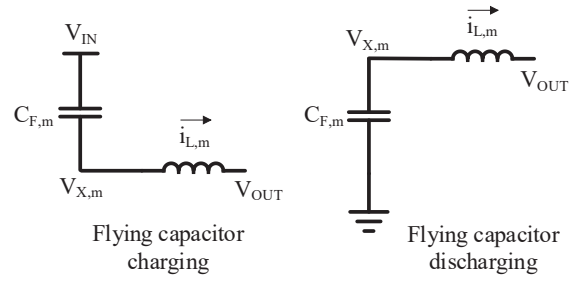


Fig. 3: Simplified equivalent circuit for a single (m^{th}) trace of a nominally 2:1 direct-conversion ReSC converter.

III. ANALYSIS OF CONVERTER DYNAMICS

The dynamics of the circuit can be classified into four parts, namely, charging and discharging of the flying capacitors, current flow through the inductor traces and output ripple across the bypass capacitors. In this work we make the simplifying assumption of a fixed input voltage V_{IN} and a single bypass capacitor at the output; although other configurations and considerations are possible [12], these are less important for the analysis at hand.

The dynamics of the flying capacitor $C_{F,m}$ of the m^{th} ballast trace follow as:

$$i_{L,m} = C_{F,m} \frac{d(V_{CF,m})}{dt} = -C_{F,m} \frac{dV_{X,m}}{dt}, \quad (1)$$

where $i_{L,m}$, $V_{CF,m}$, and $V_{X,m}$ are the m^{th} trace current, flying capacitor voltage, and switching node voltage respectively as illustrated in Fig. 3. Due to the assumption of fixed V_{IN} (or large input bypass capacitance), these dynamics are the same whether the capacitor is charging or discharging.

To express the dynamics of the inductor is not as straightforward due to the mutual coupling between individual traces. For the N trace structure, the inductances can be compactly expressed using the inductor matrix, $\mathbf{L}$:

$$\mathbf{L} = \begin{bmatrix} L_{11} & L_{12} & \cdot & \cdot & L_{1N} \\ L_{21} & L_{22} & \cdot & \cdot & L_{2N} \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ L_{N1} & L_{N2} & \cdot & \cdot & L_{NN} \end{bmatrix}, \quad (2)$$

where the left diagonal elements represent the self-inductance of the individual traces while the other elements capture the mutual inductances. For example, L_{11} is the self-inductance of the innermost trace (1st trace) while L_{12} is the mutual inductance of the 1st and 2nd trace. L_{21} refers to the same mutual inductance and is equal to L_{12} . Therefore, $\mathbf{L}$ is a symmetric matrix. The governing equation for the m^{th} trace which relates the voltage across the trace and the current is,

$$V_{X,m} - V_{OUT} = \sum_{k=1}^N L_{mk} \frac{di_{L,k}}{dt}. \quad (3)$$

Finally, the output ripple across bypass capacitor, C_O , may be calculated by applying KCL at V_{OUT} node,

$$\frac{dV_{OUT}}{dt} = -\frac{V_{OUT}}{C_O R_{LOAD}} + \frac{\sum_{k=1}^N i_{L,k}}{C_O}. \quad (4)$$

For compactness, we can define two column vectors, one each for the switching node voltages and trace currents as:

$$\mathbf{V}_X = [V_{X,1} \ V_{X,2} \ \dots \ V_{X,N}]^T, \text{ and} \quad (5)$$

$$\mathbf{i}_L = [i_{L,1} \ i_{L,2} \ \dots \ i_{L,N}]^T. \quad (6)$$

From Fig. 2, we observe that there are N individual traces, N flying capacitors and one output bypass capacitor network whose initial conditions (inductor currents for the traces and capacitor voltages) can be independently set for an individual clock phase. We can hence conclude that the order of the system is $2N+1$. To form the state-space equation first we define the state vector for a particular clock phase, ϕ_j ,

$$\mathbf{x}_j = [\mathbf{V}_{X,j} \ V_{OUT,j} \ \mathbf{i}_{L,j}]^T, \quad (7)$$

where subscript j represents the index of the clock phase at which we are analyzing. We form the state-space equation,

$$\frac{d\mathbf{x}_j}{dt} = \mathbf{A}_C \mathbf{x}_j, \quad (8)$$

where system matrix $\mathbf{A}_C$ depends only on the network characteristics and is independent of the clock phase, j . The exact formulation of $\mathbf{A}_C$ is shown in Appendix A.

Under steady-state if we know the initial conditions at the beginning of the clock phase, we can determine the final state at the end of the clock phase, i.e., $t = D_j T_s$, where, D_j is the fraction of the overall clock period, T_s , for phase, ϕ_j . This may be expressed in matrix exponential form as,

$$\mathbf{x}_j(D_j T_s) = e^{\mathbf{A}_C D_j T_s} \mathbf{x}_j(0). \quad (9)$$

During every clock phase, the final conditions of the last cycle will follow a state transition to arrive at the initial conditions of the next cycle. The analysis is simplified by assuming periodic steady state operation; i.e., the initial conditions must be equal to the final conditions across the switching period. For the nominal 2:1 ReSC converter in Fig. 2, the same is true across the half-period, assuming duty cycle $D_1 = D_2 = 0.5$ and that *flying capacitors operate at their nominal (balanced) voltage level*. Thus, for the charging ($j = 1$) to discharging phase ($j = 2$) transition, we can write,

$$V_{IN} - V_{X,m,1,final} = V_{X,m,2,final}. \quad (10)$$

This relation remains the same during the discharging to charging phase transition. The state transition can therefore be generically written as,

$$\mathbf{x}_{next}(0) = \mathbf{A}_T \mathbf{x}_j(D_j T_s) + \mathbf{B}_T V_{IN}, \quad (11)$$

where $\mathbf{x}_{next}(0)$ is the initial condition of the state following $\mathbf{x}_j$; $\mathbf{A}_T$ and $\mathbf{B}_T$ are the state transition and input matrices respectively and are described in more detail in Appendix A.

The state transition model (11) can be used to formulate a discrete time (DT) state-space model of the system. For simplicity, we continue the analysis for the 2:1 direct-conversion ReSC converter, however the procedure followed is general in nature. Let us start observing the converter from the k^{th} clock cycle assuming that $D_1 = D_2 = 0.5$. Using (9) and (11), we can relate the initial condition of the charging phase of the $(k+1)^{th}$ cycle to the final condition of the discharging phase of the k^{th} cycle by,

$$\mathbf{x}_1((k+1)T_s) = \mathbf{A}_T e^{\mathbf{A}_C \frac{T_s}{2}} \mathbf{x}_2(kT_s + \frac{T_s}{2}) + \mathbf{B}_T V_{IN}. \quad (12)$$

We can perform a similar procedure to relate the initial condition of the discharging phase of the $(k+1)^{th}$ cycle to the final condition of the discharging phase of the k^{th} cycle. If we assume a sampling interval of T_s but with an offset of $\frac{T_s}{2}$, we establish the DT state-space equations,

$$\mathbf{x}_1[k+1] = \mathbf{A}_T e^{\mathbf{A}_C \frac{T_s}{2}} \mathbf{x}_2[k] + \mathbf{B}_T V_{IN} \quad (13)$$

$$\mathbf{x}_2[k+1] = \mathbf{A}_T e^{\mathbf{A}_C \frac{T_s}{2}} \mathbf{x}_1[k+1] + \mathbf{B}_T V_{IN}. \quad (14)$$

We can define a DT state-vector, $\mathbf{X}[k]$, such that,

$$\mathbf{X}[k] = \begin{bmatrix} \mathbf{x}_1[k] \\ \mathbf{x}_2[k] \end{bmatrix}. \quad (15)$$

Then, using (13) and (14), we can obtain the overall state-space equation of the converter as DT system embedding the CT individual clock phase dynamics as,

$$\mathbf{X}[k+1] = \mathbf{A} \mathbf{X}[k] + \mathbf{B} V_{IN}, \quad (16)$$

where $\mathbf{A}$ is the overall converter system matrix and $\mathbf{B}$ is the overall converter input matrix, which are provided in Appendix A. Finally, an assumption that the converter operates in periodic steady-state provides the constraint that:

$$\mathbf{X}[k+1] = \mathbf{X}[k]. \quad (17)$$

This leads to a closed-form expression for the steady state state-vector, $\mathbf{X}_{SS}$, using (16) and (17),

$$\mathbf{X}_{SS} = (\mathbf{I} - \mathbf{A})^{-1} \mathbf{B} V_{IN}. \quad (18)$$

This closed-form expression makes intuitive sense because it states that the steady-state voltages and currents are linearly dependent on the input, V_{IN} (this is due to the assumption of resistive load R_{load} ; if the load were modelled as a current source this dependency would shift to a function of output I_{load}). This is true only if the initial conditions decay in the steady state. For most practical converters, which have finite parasitic resistances in the traces and capacitors, (and for example, where natural or active balance is achieved) this would indeed be the case.

A. Single resonant frequency mode of operation

The generic analysis of the dynamics using state-space equips us with a powerful closed-form expression to understand the $(2N+1)$ order converter system. As a result, the system may have multiple resonant frequencies. But for most practical converter scenarios, we would like the converter to have a single resonance frequency; here we prove that under typical operating conditions the converter will operate as a reduced (effectively 2nd) order fundamental resonant system.

We prove by contradiction that the trace currents will be phase aligned, i.e., we assume phase shifts among the currents and voltages to analyze the system in steady state. Furthermore, we assume perfect Zero Current Switching (ZCS) when the individual phase transition occurs. The time domain expression during a single-clock phase for the switching node of the generic m^{th} trace is,

$$V_{X,m,j}(t) = V_{OUT} + V_{m,j} \cos(\omega t + \varphi_m), \quad (19)$$

where V_{OUT} is assumed constant, i.e. has negligible variation compared to the AC component of the switching node voltage, which has amplitude $V_{m,j}$. The phase shift, φ_m , is representative of the timing mismatch for the individual switching node voltages. Finally, the angular resonance (and switching) frequency is denoted by ω . If we arbitrarily choose φ_1 (phase shift of the first trace) as a reference, as is shown in Appendix B, we can form a system of linear equations for the $\sin(\varphi_1 - \varphi_m) = \sin(\Delta\varphi_m)$ terms to obtain,

$$\begin{bmatrix} (\omega^2 L_{22} C_{F,2} - 1) V_{2,j} & \cdot & \omega^2 L_{2N} C_{F,N} V_{N,j} \\ \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot \\ \omega^2 L_{N2} C_{F,2} V_{2,j} & \cdot & (\omega^2 L_{NN} C_{F,N} - 1) V_{N,j} \end{bmatrix} \begin{bmatrix} \sin(\Delta\varphi_2) \\ \cdot \\ \cdot \\ \sin(\Delta\varphi_N) \end{bmatrix} = 0. \quad (20)$$

Here, (20) represents a set of homogenous linear equations. From standard linear algebra we know that the system will have only the trivial solution, i.e., all the $\sin(\Delta\varphi_m)$ terms are zero if the determinant of the coefficient matrix is non-zero. If the determinant of the coefficient matrix were equated to zero, it would form an $(N-1)^{th}$ order polynomial equation of ω . Carefully looking at the coefficient matrix we realize that any term relating to the first trace is absent. This implies, that the solutions for the angular resonant frequency, ω , is independent of the first trace. We realize this to be a contradiction especially for a mutually coupled network. Finally, we should remember, the choice of the reference phase was arbitrary. Hence, choosing the phase for another trace voltage as the reference would lead to ω being independent of the parameters of the reference trace but depend on the first trace. This contradiction confirms that (20) has only the trivial solution,

$$\sin(\varphi_1 - \varphi_m) = 0. \quad (21)$$

This implies from trigonometry that for all traces, $\varphi_m = \varphi_1 + p\pi$, for any integer, p . If, however, p is odd, it would mean the polarity of the inductor currents and switching node voltages are reversed, implying power flow from the output to the source. However, this contradicts the viable steady state operation of the converter. In fact, for all even p , the behavior would be the same as $p = 0$. Hence, we can state that,

$$\varphi_m = \varphi_1. \quad (22)$$

B. Current Scale Factors and Converter Parameters

An important result of the proof leading to (22) is that because all trace currents must be phase aligned, we can also say that these currents are linearly dependent. To simplify the analysis and design process, we define the ratios of these linearly dependent currents using *current scale factors*,

$$a_m = \frac{I_{L,m}(t)}{I_{L,1}(t)}, \quad (23)$$

where a_m is a positive real number and represent *how the m^{th} trace current scales with the current in the first trace*. Later we will choose these scale factors as a key design objective, but for now we determine key converter parameters based on arbitrary a_m values. Taking the time derivative of (3) and using (1) and the definition in (23), we get a second order differential equation for $i_{L,1}(t)$,

$$\frac{d^2 i_{L,1}}{dt^2} = - \frac{a_m}{C_{F,m} \sum_{k=1}^N a_k L_{mk}} i_{L,1}. \quad (24)$$

This results in yet another important insight. The dynamics of every individual clock phase are completely captured by a second order system equation. This shows how the complex $2N+1$ order system collapses to much simpler and intuitive second order system. In fact, (24) resembles the familiar equation $\frac{d^2 y}{dx^2} = -\omega^2 y$ form. Hence, we may conclude that the natural resonance frequency of the system is,

$$f_{res} = \frac{1}{2\pi\sqrt{L_{eff,m} C_{F,m}}}, \text{ where} \quad (25)$$

$$L_{eff,m} = \frac{\sum_{k=1}^N a_k L_{mk}}{a_m}. \quad (26)$$

The intuition gained from the (25) and (26) is that the flying capacitance, $C_{F,m}$, is resonating with an effective inductance, $L_{eff,m}$. This effective inductance is the result of the self-inductance of the trace modified by the current scaling factors and the mutual inductances associated with it. Similarly, due to time and frequency alignment of current waveforms, the capacitance of the m^{th} trace needed to achieve the desired scale factors in (24) follows from

$$C_{F,m} = C_{F,1} \frac{L_{eff,1}}{L_{eff,m}} = C_{F,1} a_m \frac{\sum_{k=1}^N a_k L_{1k}}{\sum_{k=1}^N a_k L_{mk}}. \quad (27)$$

The importance of (27) is that it provides the relationship needed to determine individual flying capacitor values to achieve trace currents, $I_{L,1} \dots I_{L,m}$, segmented according to scale factors $a_1 \dots a_m$ for a given inductance matrix, e.g. (2).

IV. DESIGN STRATEGY FOR A CURRENT-BALLASTED DIRECT-CONVERSION RESC CONVERTER

For a given inductor winding structure and fixed total flying capacitance C_{tot} , the next goal is to determine exactly how to segment this capacitance to individual flying capacitors in order to reduce total conduction loss in the inductor. A first consideration is optimal current distribution among the winding segments. Let us denote the ESR of the generic m^{th} trace to be R_m . The overall conduction loss of the converter solely due to the ESR of the inductors is given by,

$$P_{C,IND} = \sum_{m=1}^N i_{m,rms}^2 R_m. \quad (28)$$

where $i_{m,rms}$ is the rms current of the m^{th} trace. We can derive the optimal $i_{m,rms,opt}$ to minimize the overall loss, $P_{C,IND}$. It is briefly shown in Appendix C that applying the definition of current scaling factors in (23), we get,

$$a_{m,opt} = \frac{i_{m,rms,opt}}{i_{1,rms,opt}} = \frac{R_1}{R_m}. \quad (29)$$

The result (29) is the same as previously shown in the literature for multiphase buck converters [18]. A key intuition developed here is that for spiral geometries with fixed trace width, trace currents optimally scale down (inversely with the trace diameter) from innermost to the outermost traces. Thus, the magnitude of the current scaling factors depends on winding outer/inner diameter and number of traces. An example of such scaling factors is shown in Fig. 4. Here a 6-trace planar-spiral inductor

is considered (matching geometry of experimental designs described in the next section). This example has fixed trace width and spacing, but different inner radius from 1mm to 8mm. It is seen that the smaller inner radius (larger ratio of outer/inner diameter) has a larger spread of ideal scaling factors, a_m , due to larger range of ESR in the coupled traces. With larger inner radius (lower ratio of outer/inner diameter) the spread of trace resistance is smaller. However, this resistance segmentation assumes trace widths small enough that intra-trace current crowding is negligible (i.e. width less than an effective skin depth); if this is not the case, the R_m values may need to be calculated based on an AC resistance or a resistance matrix approach.

Whatever segmentation is used in (29), this can be combined with (27), using an assumption on total capacitance, $C_{tot} = \sum_{m=1}^N C_{F,m,opt}$, to determine optimum capacitance $C_{F,m,opt}$ used to achieve the desired ballasting ratios:

$$C_{F,m,opt} = \frac{C_{tot}}{\left(\frac{\sum_{x=1}^N a_{x,opt} L_{mx}}{a_{m,opt}} \right) \left(\frac{\sum_{k=1}^N \left(\frac{a_{k,opt}}{\sum_{x=1}^N a_{x,opt} L_{kx}} \right) \right)} \quad (30)$$

Finally, applying (31) to (26), we obtain the expression for the natural resonant frequency given optimal segmentation of flying capacitance (optimal a_m values):

$$f_{res} = \frac{\sqrt{\sum_{k=1}^N \left(\frac{a_{k,opt}}{\sum_{x=1}^N a_{x,opt} L_{kx}} \right)}}{2\pi\sqrt{C_{tot}}} \quad (31)$$

The important takeaway from (31) is how the resonant frequency is modified for the optimal current ballasting profile as function of not just the inductors and capacitors, but also on the trace resistance (through $a_{m,opt}$ values). A key advantage of the analysis for a single resonant frequency mode over the generic state-space analysis is the ability to obtain closed-form design equation (30) to select flying capacitors. However, if we plug in the values obtained in (30) and solve state-space framework developed, the results match the single-frequency and phase response conclusions obtained.

V. VERIFICATION: SIMULATION AND HARDWARE TESTING

A first verification of the above theory was completed using simulation (Cadence IC6) compared to the state space model (18). The comparison considers a planar air-core 4-trace inductor of 1mm² area and total flying capacitance constrained to 24nF. The structure is a circular spiral with an inner radius of 0.15mm and trace to trace spacing of 4μm. The steady-state results using state-space solution in (18) and corresponding simulations in SPICE are shown in Fig. 5. As seen in Fig. 5, theory is in good agreement with simulation. Minor differences arise due to finite deadtimes and other nonidealities in the simulation compared to the theoretical model, however the overall ballasting profile is in good agreement, highlighting the accuracy of the state space model and relationships in (30) and (31).

To explore the benefits and also practical limitations of the current ballasting concept, we performed simulations using the ANSYS Maxwell 2D EM package. Simulations were done matching the dimensions of test structures used in a printed-circuit board (PCB) prototype representing a single turn, multi-trace planar-spiral inductor. Important practical considerations for PCB spiral magnetics include minimum trace width and

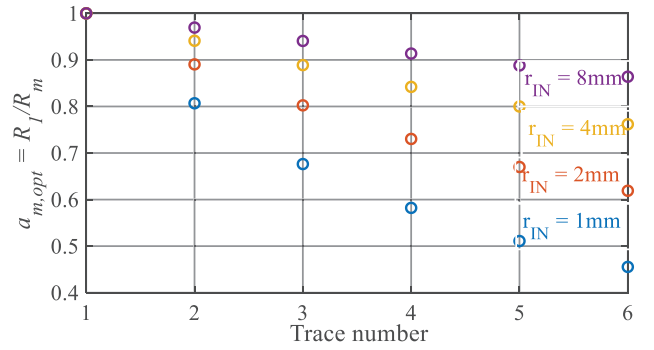


Fig. 4. Example optimal current scaling factors for a 6-trace spiral inductor with fixed trace width and pitch but varying inner radius.

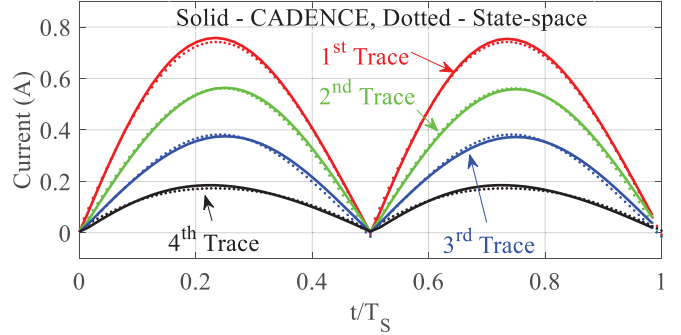


Fig. 5. Ballasted trace currents solved by state-space and simulated in Cadence for a 1mm² planar spiral inductor with 24nF total flying capacitance.

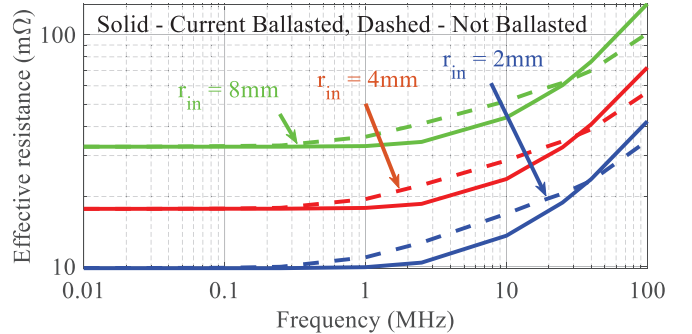


Fig. 6. Comparison of the effective resistance achieved by a current ballasted versus non-ballasted structure for different inner radius test structures.

spacing (here 5 mil). Such constraints can limit the practical benefits of current ballasting as discussed below.

Fig. 6 shows a comparison of ESR achieved by ballasted and non-ballasted planar-spiral PCB windings with approximately the same geometries used for an experimental prototype (discussed next). The simulated structures use 6 single-turn traces, each with 5 mil width and spacing; three sizes are explored from inner radius of 2mm, 4mm, and 8mm. Forced current excitations match a scenario where total capacitance C_{tot} is used to resonate the winding structure at a given frequency. In the ballasted case, unique current excitations are applied to each of the six traces; in non-ballasted case, a single current excitation is applied to the whole structure.

Several observations can be made from Fig. 6. First, at low frequency, ballasting provides little benefit due to limited impact of current crowding. As frequency increases, the benefit of ballasting initially grows; specifically it is seen that the ESR of the ballasted structures stays relatively constant (near the DC

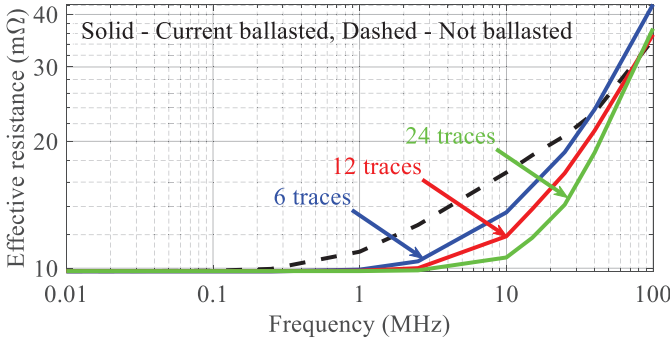


Fig. 7 Comparison of ballasted vs not ballasted for $r_{in} = 2\text{mm}$ structure with winding split into increasingly narrower and higher number of traces.

resistance asymptote) for a wider frequency range than the case without ballasting. However, at higher frequency, the ESR of the ballasted structures eventually increases and the benefit decreases; this effect comes from intra-trace (skin and proximity effect) current crowding due to the relatively wide 5-mil traces.

While this increase in ESR in the ballasted structure might suggest a deviation from the analysis presented in Section IV, more specifically it highlights that using the DC trace resistance as a means to choose current scale factors (29) has limitations. Specifically this result motivates to either: 1) adjust the scaling factors in (29) based on the AC resistance of traces at a given frequency or consider a more complicated treatment using a winding resistance matrix; or 2) ensure that trace widths remain small enough such that skin and proximity effect current crowding are indeed small enough to neglect. Point 1) above motivates extension of this work for more complex AC resistance profile and that affects relationships derived in (29)-(31).

Fig. 7 provides a perspective on item 2) above. Here, a single planar spiral winding ($r_{in} = 2\text{mm}$) is split up into an increasing number of narrower trace segments. Here, the observation is that by using narrower trace widths (same total metal area or DC conductance), the impact of intra-trace current crowding (skin and proximity effects) are moved to higher frequency. This allows the structure to extend and expand the benefits of ballasting to higher frequencies. It also highlights again, some practical implications. For example, for the 12- and 24-trace structures require less than minimum allowed trace width/space for typical printed circuit board processes. This indicates that ballasting may be more practical and beneficial at lower frequencies (and larger structures) in typical PCB implementations; however, for integrated circuit implementations (and/or where finer trace width/space are feasible), the benefits may be more pronounced and/or extend to higher frequency.

To validate and compare to theory and simulation, a PCB prototype with several test structures (matching the geometries explored in Fig. 6) was designed and tested as shown in Fig. 8. The test structures comprise single-turn, 6-trace inductors with inner radius 2mm, 4mm and 8mm. Class I C0G 0402 capacitors were used to resonate the structures. An impedance analyzer having four-terminal-pair (4TP) auto-balancing bridge system [19] has been used for the measurements.

Current ballasting was implemented by choosing appropriate capacitance values based on DC trace resistance (radius). However, due to availability some approximation was

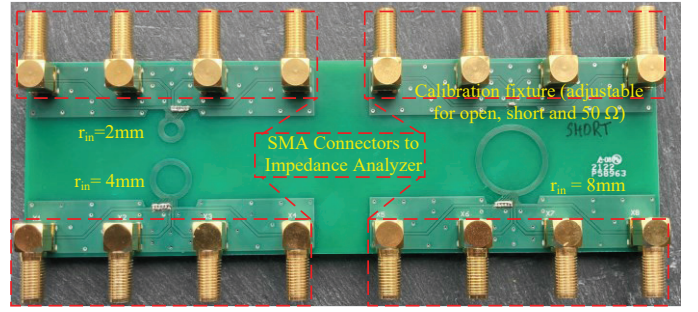


Fig. 8. Designed 2-layer PCB prototype.

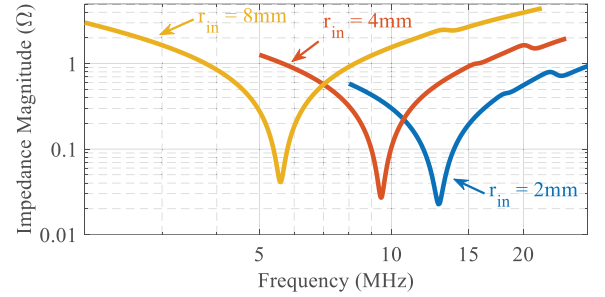


Fig. 9 Measured impedance of ballasted windings

made in exact capacitance values and thus the ballasting profile is only a close approximation of the ideal value as would be given by (29). For comparison to the non-ballasted case, all capacitor terminals were shorted such that the same total capacitance was used, just in parallel with the overall winding structure(s). Capacitor ESR was carefully calibrated to remove this from winding loss comparison.

Fig. 9 shows measured impedance of the ballasted structures. As expected the impedance increases with dimension of the structure due to larger inductance and resistance. Slight kinks are observed at frequencies beyond the primary resonance. These indicate higher-order dynamics of these structures as outlined in the state space model.

TABLE I. COMPARISON OF MEASURED RESISTANCE: CAPACITIVE BALLASTED (R_{BAL}) AND WITHOUT BALLASTING (R_{w/o_BAL})

	$r_{in} = 2\text{mm}$	$r_{in} = 4\text{mm}$	$r_{in} = 8\text{mm}$
$R_{w/o_BAL} \text{ (m}\Omega\text{)}$	23.8	29.3	50.0
$R_{BAL} \text{ (m}\Omega\text{)}$	21.6	26.0	40.1
Ballasting Improvement (%)	9.3%	11.3%	19.8%
$f_{res} \text{ (MHz)}$	13.0	9.6	5.5

Table I shows measured ESR at the resonant frequency for the various structures. We observe that the resistance offered by all three structures are better for the ballasted case than without ballasting. The effect is more pronounced for the largest structure (about 20% reduction in resistance). These results can be compared to the same achieved by EM simulation (Fig. 6). It is seen that while there is indeed a benefit to capacitive ballasting, this benefit is only modest for the PCB test structures in question. Importantly, it can be observed that the larger structure $r_{in} = 8\text{mm}$ has the largest benefit. This is because it is resonating at the lowest frequency, where intra-trace skin and proximity effects are least; however the smallest structure, resonating at

~13MHz has higher loss due to larger per-trace resistance than would be predicted by the DC model alone.

While the results in Table I. might not appear compelling, they provide validation for the underlying concept of direct-conversion current ballasting. More importantly, they highlight key challenges and opportunities for further exploration. Notably, it is clear that for operation at very high frequency, the winding geometry must permit the use of fine pitch metallization (to reduce intra-trace current crowding effects). While this is straightforward in many integrated circuit process technologies, it may be more difficult in discrete implementations, such as in printed circuit boards, where limitations on trace width and spacing constrain useful operating frequencies to the MHz to 10's of MHz regime.

VI. CONCLUSION

In this work, we analyze the dynamics of capacitive current ballasting for magnetic winding structures that can be used for direct-conversion ReSC DC-DC converters. Such techniques can be used to alleviate or mitigate high-frequency current crowding effects that result in poor conductor utilization and overall higher power loss. A state-space model was which provides closed form expressions for important time and frequency-domain parameters of these converters. The analysis is further simplified for single frequency operation showing that such systems can be modelled as a fundamental resonant 2nd order system. We obtain the procedure for tuning the ballasting capacitors in a manner such that any arbitrary current distribution profile may be obtained. We prove that the optimal current distribution profile for conduction loss dominated scenarios is simply the current division ratios determined by the individual trace resistances. The concepts of current ballasting and its benefits at high frequency operations is verified using test inductor structures on a 2-layer PCB.

APPENDIX

A. Derivation of the State-Space Model

The dynamics of all switching node voltages can be expressed as a matrix differential equation:

$$\frac{dV_X}{dt} = -C_F^{-1} i_L, \text{ where} \quad (32)$$

$$C_F = \begin{bmatrix} C_{F,1} & 0 & \cdot & \cdot & 0 \\ 0 & C_{F,2} & \cdot & \cdot & 0 \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ \cdot & \cdot & \cdot & \cdot & \cdot \\ 0 & 0 & \cdot & \cdot & C_{F,N} \end{bmatrix}. \quad (33)$$

Here, we refer to C_F as the flying capacitance matrix.

To embed the dynamics of all trace currents into a matrix differential equation, we rearrange the expression in (3) as:

$$L \frac{di_L}{dt} = V_X - \mathbf{O}_1 V_{OUT},$$

where, the $N \times 1$ vector $\mathbf{O}_1$ is,

$$\mathbf{O}_1 = [1 \quad 1 \quad \cdot \quad \cdot \quad 1]^T, \quad (34)$$

and further simplify to get,

$$\frac{di_L}{dt} = L^{-1} V_X - L^{-1} \mathbf{O}_1 V_{OUT}. \quad (35)$$

We now use (4), (32) and (35) to form the state-space equation (8). We define a system matrix, A_c as,

$$A_c = \begin{bmatrix} \mathbf{Z}_1 & \mathbf{Z}_2 & -C_F^{-1} \\ \mathbf{Z}_2^T & -(C_O R_{LOAD})^{-1} & C_O^{-1} \mathbf{O}_1^T \\ L^{-1} & -L^{-1} \mathbf{O}_1 & \mathbf{Z}_1 \end{bmatrix}, \quad (36)$$

where, the $N \times N$ zero matrix $\mathbf{Z}_1$ is,

$$\mathbf{Z}_1 = [0]_{N \times N}, \quad (37)$$

and the $N \times 1$ zero vector $\mathbf{Z}_2$ is,

$$\mathbf{Z}_2 = [0]_{N \times 1}. \quad (38)$$

We defined the state-transition equation (10) where the $N \times N$ transition matrix, A_T , is

$$A_T = \begin{bmatrix} -I & \mathbf{Z}_2 & \mathbf{Z}_1 \\ \mathbf{Z}_2^T & 1 & \mathbf{Z}_2^T \\ \mathbf{Z}_1 & \mathbf{Z}_2 & I \end{bmatrix}, \quad (39)$$

and the $N \times 1$ matrix, B_T , is

$$B_T = [\mathbf{O}_1 \quad 0 \quad \mathbf{Z}_2]^T. \quad (40)$$

The expanded system matrix and input matrix of the overall converter state-space formulation given by (15) are

$$A = \begin{bmatrix} \mathbf{Z}_3 & A_T e^{A_c \frac{T_S}{2}} \\ \mathbf{Z}_3 & A_T e^{A_c \frac{T_S}{2}} A_T e^{A_c \frac{T_S}{2}} \end{bmatrix}, \text{ and} \quad (41)$$

$$B = \begin{bmatrix} B_T \\ (A_T e^{A_c \frac{T_S}{2}} + I) B_T \end{bmatrix}, \quad (42)$$

where, the $(2N + 1) \times (2N + 1)$ zero matrix $\mathbf{Z}_3$ is,

$$\mathbf{Z}_3 = [0]_{(2N+1) \times (2N+1)}. \quad (43)$$

B. Mathematical Proof for Phase Alignment in Single-Frequency Operation

Let us further modify (18) by expressing the phase shift ($\varphi_m = \varphi_1 + (\varphi_m - \varphi_1) = \varphi_1 + \Delta\varphi_m$) in terms of an arbitrarily chosen reference phase, φ_1 , which is the phase shift in innermost (or the first) trace. Hence, after employing standard trigonometric identities we get,

$$V_{X,m,j}(t) = V_{OUT} + V_{m,j} \cos(\omega t + \varphi_1) \cos(\Delta\varphi_m) - V_{m,j} \sin(\omega t + \varphi_1) \sin(\Delta\varphi_m). \quad (44)$$

The last term in the right side represents the manifestation of timing mismatch from the reference trace (in this case, the first). Now we use (1), (4) and (20) to establish the voltage and current relationship for the m^{th} trace to get,

$$V_{m,j} \cos(\omega t + \varphi_m) = \omega^2 \sum_{k=1}^N L_{mk} C_{F,k} V_{k,j} \cos(\omega t + \varphi_k). \quad (45)$$

We employ the same mathematical technique to arrive at (44) from (19) on (45) and compare both sides for the coefficients of $\cos(\omega t + \varphi_1)$ and $\sin(\omega t + \varphi_1)$ to get,

$$V_{m,j}\cos(\Delta\varphi_m) = \omega^2 \sum_{k=1}^N L_{mk} C_{F,k} V_{k,j} \cos(\Delta\varphi_k), \text{ and} \quad (46)$$

$$V_{m,j}\sin(\Delta\varphi_m) = \omega^2 \sum_{k=1}^N L_{mk} C_{F,k} V_{k,j} \sin(\Delta\varphi_k). \quad (47)$$

Since $\sin(\Delta\varphi_1) = 0$, we can further manipulate (47) to obtain,

$$\omega^2 \sum_{k \neq 1, m}^N L_{mk} C_{F,k} V_{k,j} + (\omega^2 L_{mm} C_{F,m} - 1) V_{m,j} \sin(\Delta\varphi_m) = 0. \quad (48)$$

We can repeat this operation for all traces and compactly obtain (20).

C. Determination of Optimal Current Scaling Factors for conduction loss dominated scenario

We can apply an analysis like [15] in order to get,

$$\sum_{m=1}^N i_{m,rms} = \frac{\pi}{2\sqrt{2}} \left(\frac{V_{OUT}}{R_{LOAD}} \right). \quad (49)$$

If we apply the standard convex optimization techniques using Lagrange multiplier, where we want to determine the optimal $i_{m,rms,opt}$ to minimize the overall loss, $P_{C,IND}$, subject to the constraint (49), we will obtain,

$$i_{m,rms,opt} = \left(\frac{\pi}{2\sqrt{2}} \right) \left(\frac{V_{OUT}}{R_{LOAD}} \right) \left(\frac{1}{\sum_{k=1}^N R_k} \right) \left(\frac{1}{R_m} \right). \quad (50)$$

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