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Selective phosphorus doping of polycrystalline silicon on glass using self-assembled monolayer doping (MLD) and flash anneal

Glenn Packard [a,*], Carolyn Spaulding [b], Alex Taylor [b], Karl Hirschman [a], Scott Williams [b], Santosh Kurinec [a]

[a] Electrical & Microelectronic Engineering, Rochester Institute of Technology, Rochester, NY 14623, USA
[b] Schools of Chemistry & Chemical Engineering, Rochester Institute of Technology, Rochester, NY 14623, USA

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ABSTRACT

We report doping of thin (~60 nm) amorphous silicon (a-Si) on glass substrate to form n + polycrystalline silicon on glass in selective regions using Monolayer doping (MLD) via Flash Lamp Annealing (FLA). The phosphorus monolayer was formed on the exposed regions of SiO_2 patterned a-Si, through functionalization with chemically bound Diethyl vinylphosphonate (DVP) dopant molecules. The samples were capped with SiO_2 and annealed using a single xenon flash pulse (5.0 J/cm^2, 250 μs) to simultaneously crystallize a-Si, incorporate and activate phosphorus dopants. SIMS results show an average concentration of $8x10^{19}$ cm^{-3} in the 60 nm of thin silicon on glass. Electrical results show a resistivity of ~$6.60x10^{-2}$ Ω.cm in doped regions. N-channel field effect transistor devices are successfully demonstrated using this MLD-FLA technique.

1. Introduction

In recent years, many technologies have emerged to address the display industry's increasing demand for improved thin film device performance over commonly used hydrogenated amorphous silicon (a-Si:H). Low Temperature Polycrystalline Silicon (LTPS) is one such promising material due to its superior electronic performance over a-Si:H [1]. LTPS on glass can be formed by annealing a-Si using surface annealing techniques such as Excimer Laser Annealing (ELA) or flash annealing (FLA). FLA in the millisecond range using xenon-filled lamps has become an attractive technology due to its "one-shot-one-wafer" process capability well suited for industrial applications, in contrast to raster-scan ELA which is inherently slow and relatively complex [2]. The purpose of annealing is to crystallize thin a-Si on a substrate and electrical activation of dopants. Dopants are introduced on desired regions by various techniques that include ion implantation, deposition of dopant rich layers on a-Si or plasma immersion [3–6]. These techniques have their own strengths and limitations.

Monolayer Doping (MLD) is an alternative method for introducing dopants into a semiconducting material that has recently attracted much interest for forming ultra-shallow junctions in bulk silicon and silicon-on-insulators (SOI) [7–9]. In MLD, a hydrogen-terminated silicon surface is submerged in a heated solution containing an organic molecule bearing both the dopant of interest and a reactive alkene or alkyne. Over time, the Si-H surface bonds are chemically replaced with Si-organic-dopant bonds, which are trapped in a capping oxide and can be driven into the silicon bulk using an annealing process. The maximum dose of dopant that can be introduced through a single MLD process is strictly limited by the available semiconductor surface bonding sites per unit area making it a valuable technique for realizing ultra-shallow junctions.

Fig. 1 illustrates the differences in annealing temperature and time for conventional (furnace, rapid thermal annealing, spike) and advanced anneals (flash and laser) [10]. With advanced annealing techniques, it is possible to achieve higher temperature (>1200 °C) for increased dopant activation while keeping the anneal time short for restricted dopant diffusion. These advanced annealing techniques also heat only the surface of the substrate rather than subjecting the substrate bulk to high temperatures, which is necessary for thin film processing on materials such as glass or plastics.

Flash Lamp Annealing (FLA) method involves exposure of a sample to a high-intensity pulse from a xenon flashbulb, on the order of tens to hundreds of microseconds in duration. It is a high-yield and scalable process which is fully compatible with glass substrates. Recently, FLA has demonstrated promise in crystallizing amorphous silicon (a-Si) into Low-temperature polycrystalline silicon (LTPS) for making thin film

* Corresponding author.
E-mail address: gmp8087@rit.edu (G. Packard).

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transistors (TFTs) [11–12]. In the domain of FLA LTPS TFTs, MLD shows promise to be a method of dopant introduction that can result in scalable devices without inflicting the lattice damage characteristic of ion implantation.

2. Experimental

In this work, a 60 nm layer of a-Si was deposited via plasma-enhanced chemical vapor deposition (PECVD) on Corning Lotus NXT display glass substrates, with a 200 nm buffer layer of PECVD SiO_2. This layer was then lithographically patterned into mesa structures on the order of 100′s of μm^2.

To allow selective regions of undoped a-Si to be doped n-type with phosphorus using MLD, a masking layer of 100 nm PECVD SiO_2 was deposited and then lithographically patterned with windows that opened into designated regions of the a-Si mesas for phosphorus surface monolayer formation on these regions. MLD was performed using diethyl vinylphosphonate ($C_6H_{13}O_3P$) as source with mesitylene solvent in 1:25 v/v ratio, heated at 120 °C for two hours to produce silicon-vinyl phosphonate surface bonds, as shown in Fig. 2. The MLD-exposed a-Si samples were then exposed to a single FLA pulse to simultaneously crystallize the silicon and incorporate the dopants adhering to the surface. The instrument used was a NovaCentrix PulseForge 3300 Photonic Curing system with two xenon flashbulbs, modified for semiconductor processing. A pulse intensity of 5.0 J/cm^2 delivered over 250 μs with substrate heating at 400 °C were chosen as settings to provide the thin a-Si layer with enough energy to reach a liquid state and recrystallize.

A final 100 nm PECVD SiO_2 layer was deposited as a dielectric layer, and devices were metallized with aluminum to form contacts. The devices were then sintered in 5% H_2/N_2 forming gas at 450 °C for defect passivation and contact improvement. Three exemplary devices were designed on these mesas - (1) n + doped resistors, (2) n + regions separated by undoped region (n + -i-n +) and (3) n-channel metal oxide thin film transistors (NMOS TFTs). These different structures are shown in Fig. 2. Electrical measurements were performed with a HP4145B Parameter Analyzer.

3. Results and discussion

In order to determine the presence and concentration of phosphorus incorporated into a silicon mesa after MLD and FLA activation, Dynamic Secondary Ion Mass Spectroscopy (SIMS) was performed using a Cameca IMS-7f with O_2^+ primary ion beam at 50nA on resistor samples and is shown in Fig. 3a. A near uniform concentration of phosphorus ~$8x10^{19}$ cm^{-3} is observed throughout the film subsurface. Integrating over the total depth of the mesa, a dose of 4.14 × 10^{14} cm^{-2} is estimated.

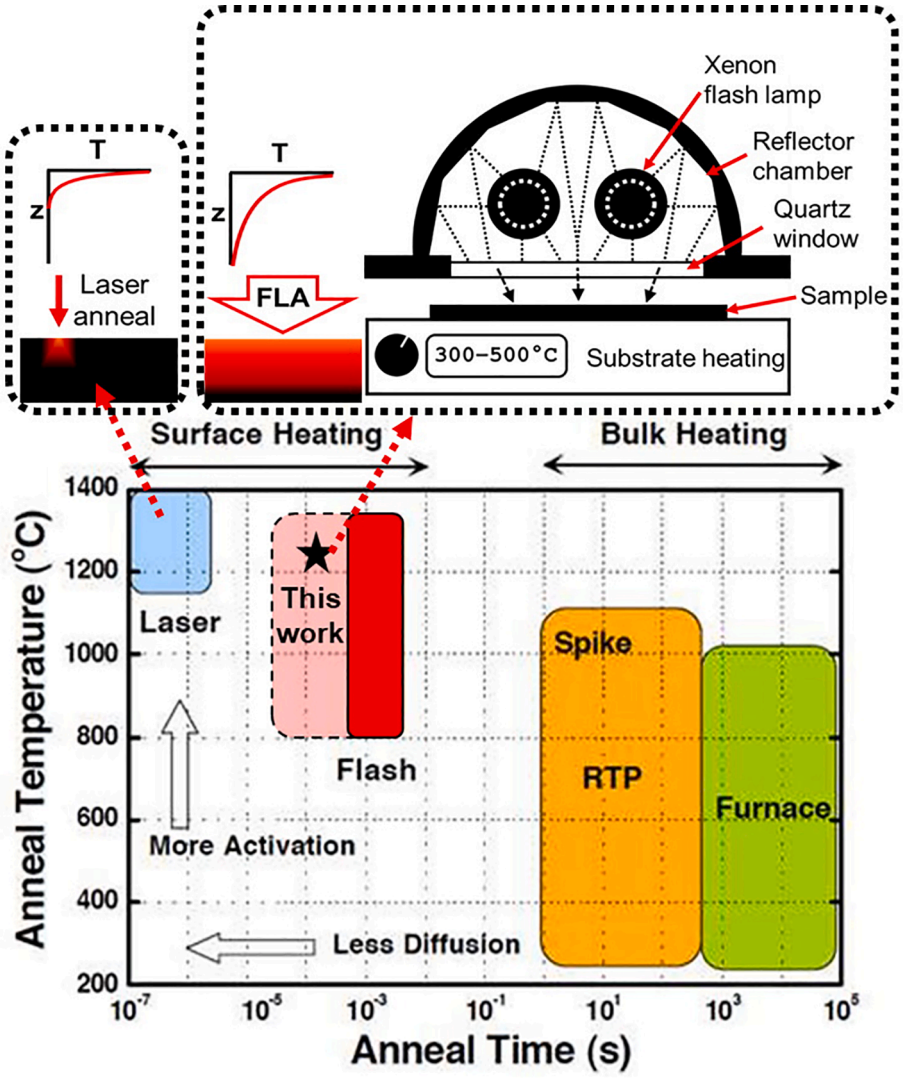

Fig. 1. Bottom: Diagram indicating the design space of Flash annealing (FLA) in comparison with laser and bulk annealing strategies, adapted with permission from [10]. Top Left: Comparison of penetration depth and exposure areas between surface heating methods. Top Right: Illustration of the FLA system.

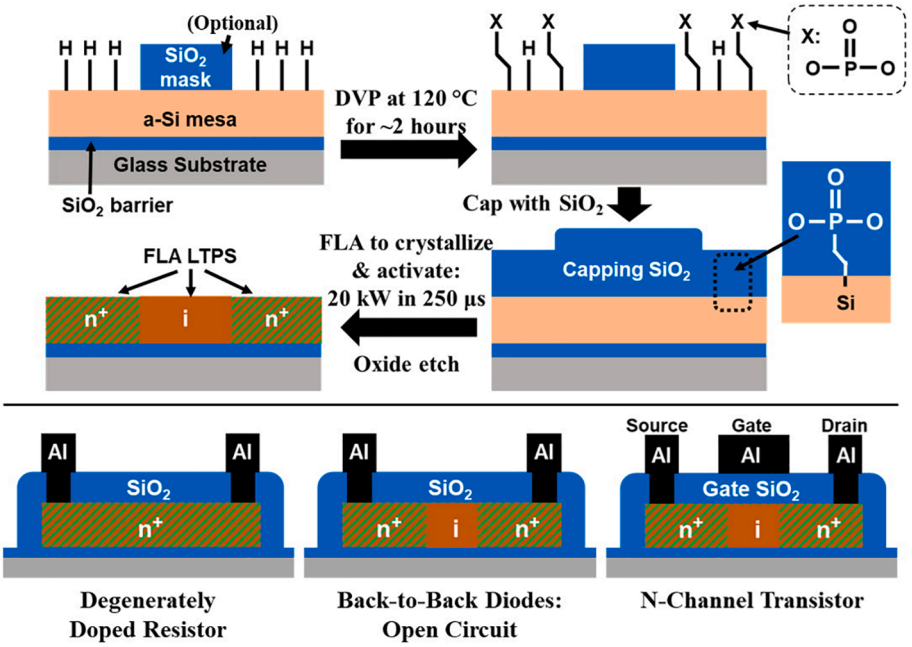

Fig. 2. Top: Illustration of patterned monolayer doping and FLA crystallization process for thin film silicon on glass. Bottom: Design of three different device structures produced in this study.

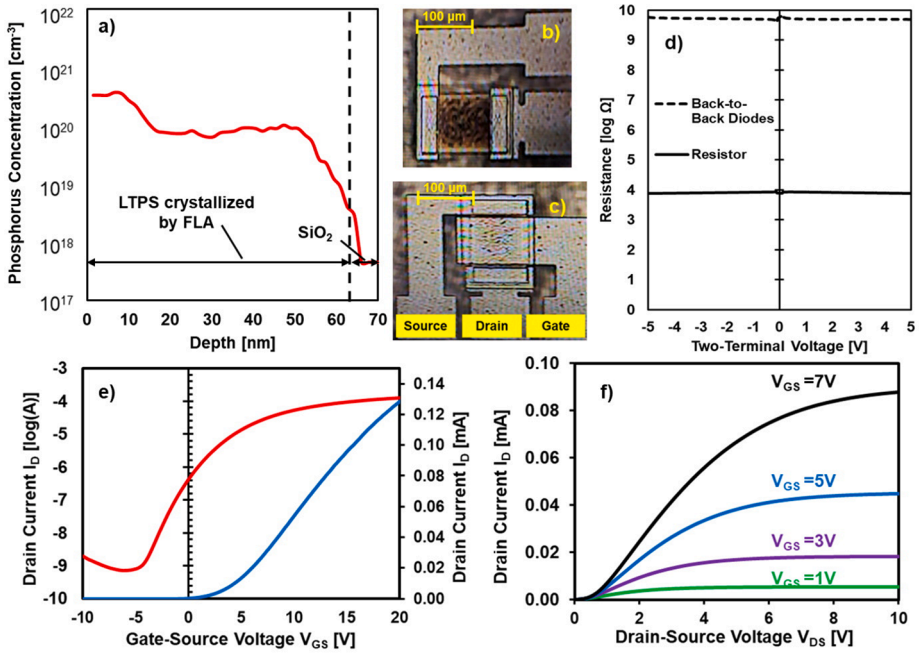

Fig. 3. a) Phosphorus concentration profile obtained by secondary ion mass spectroscopy in monolayer doped, flash annealed, low temperature polycrystalline silicon on glass. b, c) Micrographs of 96 × 96 µm^2 fully depleted resistor and n-channel transistor. d) Two-terminal resistance of resistor and back-to-back diodes. E, f): Electrical characteristics of a typical n-channel TFT fabricated in this study. d) Linear and logarithmic-scale I_D-V_{GS} response at V_{DS} = 5 V. e) I_D-V_{DS} characteristics at V_{GS} from 1 to 7 V.

Compared with the atomic surface density of the silicon (1 0 0) plane of 6.8 × 10^{14} cm^{-2}, this indicates that DVP MLD is able to terminate a-Si surfaces with phosphorus radicals at 61% of the ideal, that FLA activation does not result in significant dopant loss, and that an effective full-thickness melting is achieved during simultaneous FLA crystallization. As dopant amount is dependent on availability of surface silicon bonds, increasing dopant concentration further would require multiple MLD and FLA iterations.

The presence of electrically activated dopant was demonstrated by a 2-probe measurement of polysilicon mesas as resistors. An average sheet resistance of 11 kΩ/square was obtained on n + doped regions and n + -i-n + structure exhibited near open circuit. The sheet resistance of 11 kΩ/square yields a resistivity value of 0.066 Ω cm. This value corresponds to electron concentration-mobility product (nμ) of 9.46x10^{19} (cm V s)$^{-1}$ and for bulk crystalline silicon, an electron concentration of 1.45x10^{17} cm^{-3}. In polycrystalline thin films, some active dopant is lost via dopant segregation at the grain boundaries and mobility is lower due to the presence of grain boundaries in addition to surface scattering. This suggests an active phosphorus concentration in polycrystalline silicon (LTPS) MLD doped films higher on the order of 10^{18} cm^{-3}. Comparing with SIMS data, it indicates a significant dopant activation resulting from MLD.

Fig. 3d and 3e shows the current voltage characteristics of an NMOS TFT fabricated with n + source drain doped with MLD followed by flash

anneal on low-temperature polycrystalline silicon (MLD FLA LTPS NMOS TFT). A threshold voltage of −1.2 V and I_{on}/I_{OFF} ratio of 10^5 is obtained in 96 μm mask-defined channel length devices; metallurgical channel length is likely shorter due to lateral diffusion during melt phase. The channel mobility extracted from maximum transconductance is 61.3 cm^2/Vs. The negative threshold voltage indicates an equivalent of $\sim 5.5x10^{11}$ cm^{-2} in trapped charge at the interface. A desired threshold voltage can be realized by tailoring fabrication strategies, such as with metal gate work function adjustment or enhanced passivation.

4. Conclusions

Monolayer doping using Flash lamp annealing (FLA) has been shown to produce n-type low-temperature thin film polycrystalline silicon on glass substrate. Phosphorus bonded as a monolayer on thin amorphous silicon can be simultaneously crystallized and activated with FLA. Thin film n-channel field effect transistors have been successfully fabricated using MLD for source/drain regions. This technique shows promise to dope silicon on glass selectively without requiring dopants present during amorphous silicon deposition and avoiding energetic damage or the formation of glassy dopant skins as in other doping methods.

CRediT authorship contribution statement

Glenn Packard: Conceptualization, Methodology, Investigation, Writing – original draft, Writing - review & editing, Visualization. **Carolyn Spaulding:** Investigation. **Alex Taylor:** Investigation. **Karl Hirschman:** Methodology, Writing - review & editing, Supervision. **Scott Williams:** Methodology, Investigation, Resources, Writing - review & editing, Supervision. **Santosh Kurinec:** Writing – original draft, Writing - review & editing, Supervision.

Declaration of Competing Interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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