Modeling and Control Method for a Three-level Hybrid Modular Multilevel Converter

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***Abstract*-The modular multilevel converter (MMC) is one of the most favored topologies for medium and high voltage applications. However, the drawbacks such as lots of capacitors and doubled number of devices limit the power density. Recently proposed hybrid multilevel converters with high voltage switches and chain-links have shown the superior performance compared to the traditional MMC. Specifically, this paper focuses on an emerging three-level hybrid modular multilevel converter (3L-HMMC), which can reduce half of submodule (SM) number. Based on the operating principle, a decoupling average model is derived to reveal the internal power relationship between the three-level stacks and chain-links. It can be proven the former plays a role to transfer a part of power from dc side to ac side directly. Therefore, the energy variation of chain-link is smaller, and the dc-link capacitance could be reduced. Besides, an improved trapezoidal arm current allocation is employed to solve the arm current distortion at the voltage zero-crossing point. In order to guarantee the arm current tracking performance, the variable sampling repetitive control based current loop designs are proposed. Finally, the experimental results of a 400 V prototype validates the proposed modeling and control methods.**

***Abstract*- Three-level Hybrid modular multilevel converter (3L-HMMC), average model, power flow, capacitor voltage balancing.**

NOMENCLATURE

V_{dc}	Dc side input voltage
V_{dcp}, V_{dcn}	Upper and lower capacitor voltages of dc bus
V_{mid}	Dc side midpoint voltage
i_{dcp}, i_{dcn}	Positive and negative dc bus currents
i_{mid}	Total midpoint current
v_a, v_b, v_c	Three-phase ac output voltages
i_a, i_b, i_c	Three-phase ac output currents
V_o, I_o	Ac output RMS voltage and current
ω_o	Ac output angular frequency
L_s	Arm inductance
R_s	Equivalent resistance of each arm
C_{sm}	Submodule dc-link capacitance
N	Submodule number per arm
i_{dcpa}, i_{dcna}	Positive and negative dc bus currents of phase a
i_{mida}	Midpoint current of phase a
i_{pa}, i_{na}	Upper and lower arm currents of phase a
i_{coma}	Common mode current of phase a
i_{coma_dc}	Dc component of common mode current i_{coma}
i_{coma_ac}	High-order harmonics of current i_{coma}
v_{Spa}, v_{Sna}	Equivalent dc-side voltage integrated with three-level stack
s_{sq}	Sign function of phase a angle $\omega_o t$
v_{pa}, v_{na}	Upper and lower chain-links (CLs) voltage
v_{Cpa}, v_{Cna}	Sum of dc-link capacitor voltage of upper and lower CLs in phase a
m_{pa}, m_{na}	Upper and lower CLs duty cycle
v_{dc_a}, v_{ac_a}	Decoupling dc and ac side voltages of CLs in phase a
m_{dc_a}, m_{ac_a}	Decoupling dc and ac side duty cycles of chain-links in phase a
$v_{C\Sigma a}$	Sum of upper and lower CL dc-link voltages
$v_{C\Delta a}$	Difference of upper and lower CL dc-link voltages
P_{dc2cl}	Power from dc side to ac through CL
P_{dc2ac}	Power from dc side to ac output directly
i_{cir}	Injected circulating current for arm energy balancing
k_{rc}	Gain of repetitive control
N_s	Number of stored points in repetitive control

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I. INTRODUCTION

Modular multilevel converter (MMC) has become one of the most preferred topologies in medium and high voltage (HV) applications due to the merits of good modularity and scalability, elimination of bulky filters and low harmonics [1]-[5]. However, MMC suffers from the limitations of large number of semiconductor devices and dc-link capacitors, which increases the construction cost and system volume [6], [7].

In order to reduce the number of device and capacitor energy, various “hybrid multilevel converters” have evolved recently [8]. They are derived with the concept of combining HV switches together with chain-links (CLs) constructed by series submodules (SMs). The former can generate two- or three-level voltage waveform, while the later could shape it into multilevel sinusoidal waveform for higher quality. Therefore, the hybrid multilevel converters balance the benefits of MMC and

conventional multilevel converters. The line frequency operation of HV switches also facilitates the series device connection and higher reliability.

Following this idea, in [9]-[11], the alternate arm converter (AAC) is derived from the MMC and 2-level voltage source converter (VSC). However, the SM voltage balancing requires a specific operation condition to balance the SM voltage. Besides, the HV insulated-gate bipolar transistor (IGBT) switching results in significant dc bus current distortions, which requires the additional big dc inductor to smooth the current. In addition to AAC, the hybrid converter with cascaded full-bridge (FB) SMs at ac side was proposed to achieve the dc fault tolerance and a smaller size, but increases the semiconductor losses from the two-level structure and more device number in the conduction path [12], [13]. The controlled-transition full-bridge (CTFB) proposed in [14] uses the CL based on FB SM for voltage synthesis during the controlled transition region, but the CL should take energy from dc side during a small transition time, which causes high inrush current. Besides, a family of parallel hybrid converter (PHC) [15], [16] and derived topologies have been proposed, including the series bridge converter (SBC) [17]-[19], enhanced SBC (ESBC) [20], hybrid series converter (HSC) [21] and hybrid phase converter (HPC) [22]. The major advantage of PHC is the smaller energy storage requirement per unit apparent power compare to MMC and AAC. However, the incapability to operate over a wide range of modulation index and the difficult HV transformer design are the major technical challenges.

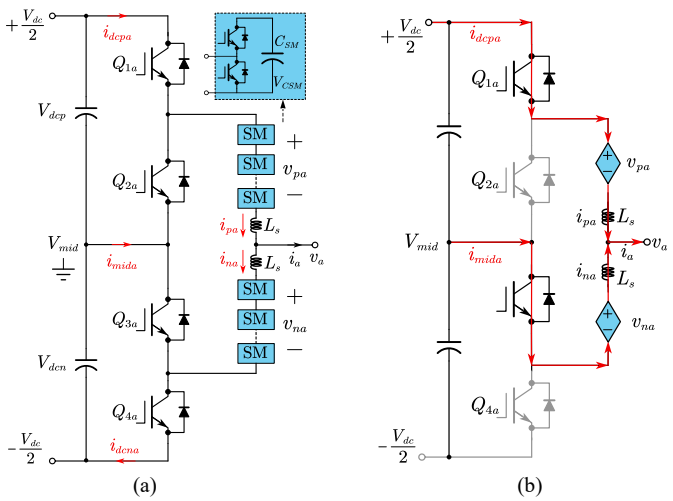
Apart from aforementioned topologies, a modular embedded multilevel converter (MEMC) is proposed in [23], [24], which combines the advantages of three-level VSC and MMC. The MEMC can reduce half of SMs compared to the MMC of same voltage and power rating. Therefore, it shows great potential in applications which are sensitive to the converter size and power density, such as offshore windfarm, emerging electric ship tractions and city in-feed [25]. Through the same concept, [26] proposes a hybrid multilevel dc–ac converter (HMC) and realizes the soft-switching of IGBT stacks. However, the SM capacitor voltage balancing requires extra FB modules, thus undermining the merits of this topology. A similar neutral-point-clamped MMC (NPC-MMC) is derived in [27], which clarifies the required energy storage requirement based on a theoretical analysis. But this paper employs the same current allocation method with the traditional MMC, and large dc side capacitors are necessary to suppress the dc voltage ripple. Then [28] presents a three-level hybrid MMC (3L-HMMC) family with three members, and gives a comprehensive comparison between them and the traditional MMC. It claims that under high power factor, this topology can save around 30% devices, 50% total capacitor and 32% power losses compared to MMC. The power density, efficiency, and construction cost could be improved a lot. But it should be noted that the existence of dc bus capacitor implies this 3L-HMMC is more suitable for the medium voltage (MV) applications, such as renewable energy interfacing, STATCOM and so on. Literature [29] proposed a diode version hybrid modular multilevel rectifier (HMMR) for HVDC case. However, understanding the internal energy flow of 3L-HMMC is the basis of the arm capacitor balancing and midpoint voltage control. This paper aims at providing a clearer modeling, power flow analysis and control strategy of 3L-HMMC.

The rest of this article is organized as follows. Section II presents the basic operation principles, the average decoupling model and the power flow graph of single-phase 3L-HMMC. Then three-phase working modes and influence of dc-side capacitors with different arm current allocation schemes are discussed in section III. A new trapezoidal allocation method is proposed to improve the ac side current quality at the zero crossing point. Next section IV shows the midpoint voltage regulation and a novel SM capacitor voltage balancing method based on the predictive control. And the variable sampling repetitive control (RC) is employed to track the periodic current reference. Finally in section V, the proposed modeling and control methods are validated in a scale-down 3L-HMMC prototype. The steady state and dynamic experiments are implemented to evaluate the performance of whole system.

II. Single-Phase Modeling

A. Topology and Operation Principles

The topology structure of a single-phase 3L-HMMC (phase *a*) is depicted in Fig. 1(a). It consists of two arms and a three-level stack with four devices Q_{1a}, Q_{2a}, Q_{3a} and Q_{4a}. The midpoints of the three-level stack in each phase are connected together as the midpoint voltage V_{mid}. As mentioned in [28], two small capacitors are added across the dc bus to provide the commutation path for the three-level stack, and their voltages are V_{dcp} and V_{dcn}. The positive, midpoint and negative dc currents of phase *a* are denoted as i_{dcpa}, i_{mida} and i_{dcna}, respectively. As for upper and lower arms represented by the subscripts *p* and *n*, they are comprised of *N* series half-bridge (HB) SMs based CL and an arm inductor L_s. Each SM has a dc-link capacitance C_{SM} of rated voltage V_{CSM}. Therefore, the sum of inserted voltage within upper and lower CLs are denoted as v_{pa} and v_{na}, whereas i_{pa} and i_{na} refer to the corresponding arm currents. Two arms are connected together to support the ac side current i_a and voltage v_a with the angular frequency ω_o.



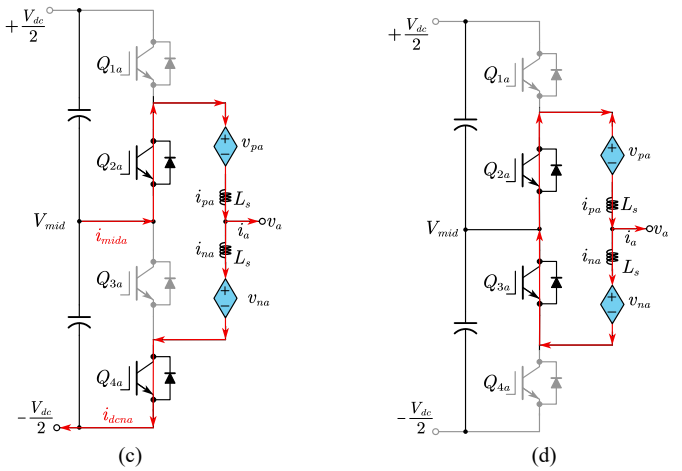


Fig. 1 (a) Topology of single-phase 3L-HMMC. (b) P state. (c) N state. (d) Z state.

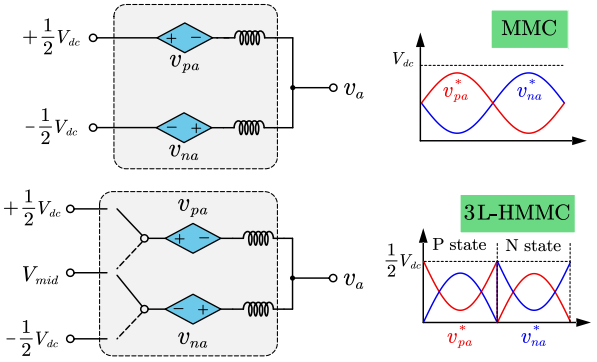


Fig. 2 Arm voltage waveforms of single-phase MMC and 3L-HMMC.

The additional midpoint voltage V_{mid} provides a freedom to reshape and reduce the chain-link voltage stress. In order to get the minimum SM number, the three-level IGBT stack needs to act according to the polarity of v_{a} [28]. When v_{a} is positive, $Q_{1\text{a}}$ and $Q_{3\text{a}}$ are turned on, $Q_{2\text{a}}$ and $Q_{4\text{a}}$ are turned off as in Fig. 1(b). This phase works at P state, which means it is connected between the positive terminal and the midpoint. Therefore, the upper and lower CL voltage references could be calculated as (1) if neglecting the inductor voltage.

$$\begin{aligned} v_{pa}^{*} &= 0.5V_{dc} - v_a \\ v_{na}^{*} &= v_a - V_{mid} \end{aligned} \tag{1}$$

On the contrary, when the output voltage v_{a} is negative, $Q_{2\text{a}}$ and $Q_{4\text{a}}$ are turned on, $Q_{1\text{a}}$ and $Q_{3\text{a}}$ are turned off. Phase a works at N state, which means it is connected between the midpoint and the negative terminal. And the CL voltages are,

$$\begin{aligned} v_{pa}^{*} &= V_{mid} - v_a \\ v_{na}^{*} &= 0.5V_{dc} + v_a \end{aligned} \tag{2}$$

Besides, there is a Z state as the transition between P and N state with $Q_{2\text{a}}$ and $Q_{3\text{a}}$ turned on. The CL voltages at Z state can be calculated as,

$$\begin{aligned} v_{pa}^{*} &= V_{mid} - v_a \\ v_{na}^{*} &= v_a - V_{mid} \end{aligned} \tag{3}$$

This Z state can be used for CL voltage balancing, but the FB SM is necessary to generate the negative CL voltage. If the midpoint voltage is controlled to zero and Z state is neglected, the CL voltage waveform of the single-phase 3L-HMMC could be plotted as Fig. 2. It can be observed that this phase switches between P state and N state by changing the connection. And compared to MMC, the maximum CL voltage is reduced by half to $0.5V_{\text{dc}}$.

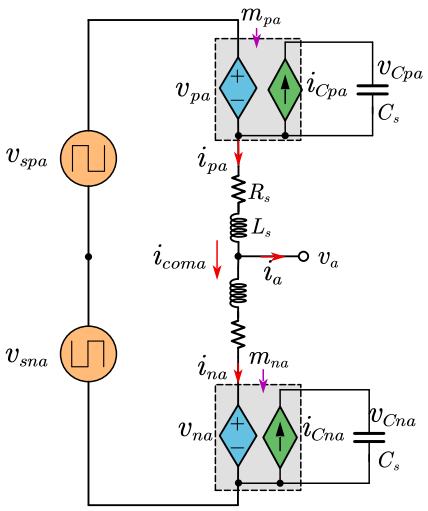


Fig. 3 Equivalent average model of single-phase 3L-HMMC.

B. Decoupling Average Model

To derive the relevant equations governing the 3L-HMMC dynamics, the phase a of 3L-HMMC is still analyzed with the similar average modeling method of traditional MMC. Firstly, the three-level stack is integrated with the dc source for simplification. The new voltage source becomes a square wave source, which could be written as,

$$\begin{cases} v_{spa} = 0.5V_{dc},\ v_{sna} = 0,\ \omega_o t \in [0, \pi) \\ v_{spa} = 0,\ v_{sna} = 0.5V_{dc},\ \omega_o t \in [\pi, 2\pi) \end{cases}$$

$$\Rightarrow \begin{cases} v_{spa} = V_{dc}(s_{sq}+1)/4 \\ v_{sna} = V_{dc}(1-s_{sq})/4 \end{cases},\ s_{sq} = \text{sgn}(\sin(\omega_o t)) \tag{4}$$

where sgn() is the sign function. Then the average model is given in Fig. 3, and an equivalent linear resistor of R_s is added to each arm to represent the losses. The series HB-SMs are represented by the concentrated voltage source and current source, which are controlled by two duty cycles m_{pa} and m_{na}.

$$v_{pa} = \sum_{i=1}^{N} v_{pa\_i} = m_{pa} \cdot v_{Cpa},\ v_{na} = m_{na} \cdot v_{Cna} \tag{5}$$

where the sum of CL dc-link capacitor voltages are denoted as v_{Cpa} and v_{Cna}, respectively. According to the power balance, the average dc-link capacitor current i_{cpa} and i_{cna} could be written as below.

$$i_{Cpa} = m_{pa} i_{pa},\ i_{Cna} = m_{na} i_{na} \tag{6}$$

And the equivalent capacitance is found from (7).

$$C_s \frac{dv_{Cpa}}{dt} = i_{Cpa},\ C_s \frac{dv_{Cna}}{dt} = i_{Cna},\ C_s = \frac{C_{SM}}{N} \tag{7}$$

As for the upper/lower arms, applying Kirchhoff's voltage law (KVL) to Fig. 3 yields,

$$v_{spa} - v_{pa} - L_s \frac{di_{pa}}{dt} - R_s i_{pa} = v_a \tag{8}$$

$$-v_{sna} + v_{na} + L_s \frac{di_{na}}{dt} + R_s i_{na} = v_a \tag{9}$$

Similar to MMC, the addition and subtraction of (8) and (9) decompose two arm variables in the format of differential mode and common mode.

$$v_a - \frac{V_{dc}}{4} \cdot s_{sq} - \frac{v_{na} - v_{pa}}{2} = \left(\frac{1}{2} L_s \frac{d}{dt} + R_s\right)(i_{na} - i_{pa}) \tag{10}$$

$$\frac{V_{dc}}{2} - (v_{pa} + v_{na}) = \left(2L_s \frac{d}{dt} + 2R_s\right)\left(\frac{i_{pa} + i_{na}}{2}\right) \tag{11}$$

In this way, the differential mode variables correspond to ac side circuit, while the common mode variables correspond to dc side circuit. Then the following variables are defined:

$$\begin{cases} v_{ac\_a} = (v_{na} - v_{pa})/2,\ v_{dc\_a} = v_{pa} + v_{na} \\ i_a = i_{pa} - i_{na},\ i_{coma} = (i_{pa} + i_{na})/2 \\ m_{ac\_a} = (m_{na} - m_{pa})/2,\ m_{dc\_a} = m_{na} + m_{pa} \\ v_{C\Delta a} = (v_{Cna} - v_{Cpa})/2,\ v_{C\Sigma a} = v_{Cpa} + v_{Cna} \end{cases} \tag{12}$$

where i_{coma} is the inner common mode current, which is also known as circulating current in many literatures. The dc and ac sides are decoupled through the equivalent voltage sources v_{dc_a} and v_{ac_a} of duty-cycles m_{dc_a} and m_{ac_a}. Using the same math operation, the new dc-link capacitor state variables $v_{C\Delta a}$ and $v_{C\Sigma a}$ represent the difference and sum of upper and lower CL capacitor voltages, respectively. Substituting these variables into (5), (10) and (11) yields the state space equation of CL part.

$$\frac{d}{dt}\begin{bmatrix} i_{coma} \\ i_a \\ v_{C\Sigma a} \\ v_{C\Delta a} \end{bmatrix} = \boldsymbol{A} \cdot \begin{bmatrix} i_{coma} \\ i_a \\ v_{C\Sigma a} \\ v_{C\Delta a} \end{bmatrix} + \begin{bmatrix} \frac{V_{dc}}{4L_s} \\ \frac{V_{dc} s_{sq} - 4v_a}{2L_s} \\ 0 \\ 0 \end{bmatrix}$$

$$\boldsymbol{A} = \begin{bmatrix} -\frac{R_s}{L_s} & 0 & \frac{m_{dc\_a}}{4L_s} & \frac{m_{ac\_a}}{L_s} \\ 0 & -\frac{R_s}{L_s} & -\frac{m_{ac\_a}}{L_s} & -\frac{m_{dc\_a}}{L_s} \\ \frac{m_{dc\_a}}{C_s} & -\frac{m_{ac\_a}}{C_s} & 0 & 0 \\ \frac{m_{ac\_a}}{C_s} & -\frac{m_{dc\_a}}{4C_s} & 0 & 0 \end{bmatrix} \tag{13}$$

According to this equation, the equivalent average model of CL part could be given as in Fig. 4(a). As depicted, each phase is hence entirely defined by four mono-physical conversion elements. It clearly highlights the dynamics of the total Arm energy (related to $v_{C\Sigma a}$), as well as the energy unbalance between the CLs (related to $v_{C\Delta a}$). The common mode terms (i_{coma} and $v_{C\Sigma a}$) represent the main power path from dc side to ac side through the media of CL, whereas the differential mode terms (i_a and $v_{C\Delta a}$) describe the power coupling between upper and lower CLs.

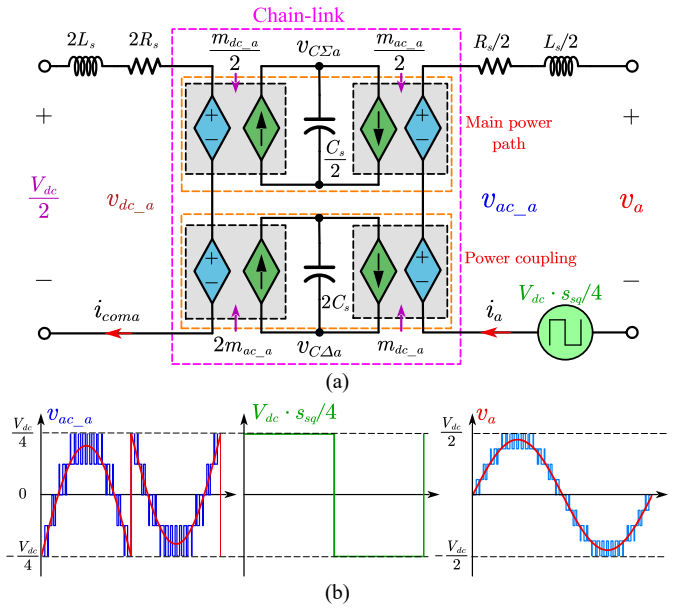


Fig. 4 (a) Decoupled average model of single-phase 3L-HMMC CL part, (b) ac side chopping waveforms and voltage levels.

The key difference of 3L-HMMC from the traditional MMC is the square wave $V_{dc} \cdot s_{sq}/4$, which is inserted with the CL ac voltage v_{ac_a} to shape the desired output voltage v_a. The ac side chopping waveforms with $N = 2$ are shown in Fig. 4(b). It can be seen that due to the additional square wave, the total voltage level becomes $4N+1$ instead of $2N+1$ in the traditional HB-MMC. Therefore, the ac output quality is not degraded with smaller number of SMs. Besides, the dc input voltage in Fig. 4(a) becomes only $0.5V_{dc}$, thereby verifying the half SM number reduction of 3L-HMMC.

Next step is the modeling of the three-level stack, which connects the dc bus with the CLs. So this model is derived from the current relationship between them. As shown in Fig. 2(a), three input currents i_{dcpa}, i_{dcna} and i_{mida} could be expressed by i_{coma} and i_a according to the explained working principle.

$$\begin{cases} i_{dcpa} = i_{pa},\ i_{dcna} = 0, i_{mida} = -i_{na},\ \omega_o t \in [0, \pi) \\ i_{dcpa} = 0,\ i_{dcna} = i_{na}, i_{mida} = i_{pa},\ \omega_o t \in [\pi, 2\pi) \end{cases}$$

$$\Rightarrow \begin{cases} i_{dcpa} = (i_{coma} + i_a/2)(s_{sq} + 1)/2 \\ i_{dcna} = (i_{coma} - i_a/2)(1 - s_{sq})/2 \\ i_{mida} = i_a/2 - i_{coma} \cdot s_{sq} \end{cases} \tag{14}$$

Since i_{dcpa} and i_{dcna} provide the input dc power alternately, the average total dc bus current i_{dc} should be,

$$i_{dc} = \frac{i_{dcpa} + i_{dcna}}{2} = \frac{i_{coma}}{2} + i_a \cdot \frac{s_{sq}}{4} \tag{15}$$

Therefore, the average model of single phase 3L-HMMC is shown in Fig. 5. The input dc bus voltage $V_{dc\Sigma}$ is defined as sum of dc input side capacitor voltage, and the difference value is denoted as $V_{dc\Delta}$ in (16).

$$\begin{aligned} V_{dc\Sigma} &= V_{dcp} + V_{dcn} = V_{dc} \\ V_{dc\Delta} &= (V_{dcn} - V_{dcp})/2 = V_{mid} \approx 0 \end{aligned} \tag{16}$$

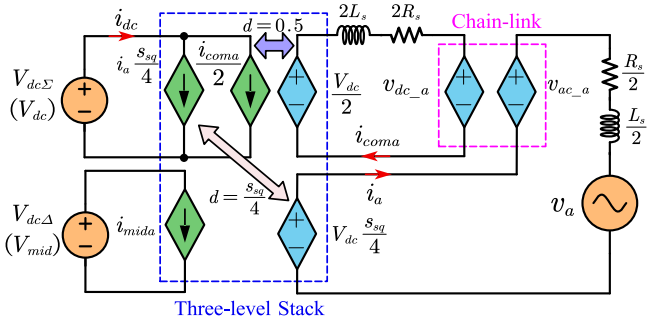


Fig. 5 Complete average model of single phase 3L-HMMC.

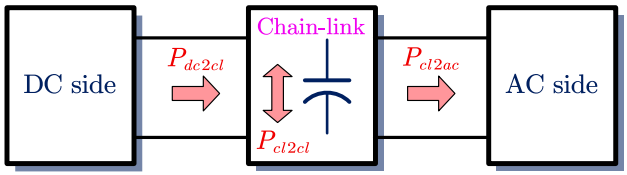


Fig. 6 Power flow of traditional single phase MMC.

The line-frequency switching of three-level stack generates two parallel current sources, one of which is controlled by a duty cycle of 0.5. So the current source value is $i_{coma}/2$, corresponding to half of the circulating current i_{coma} of CL. While the other one has an equivalent duty cycle of $s_{sq}/4$, which generates the square wave voltage $V_{dc}\cdot s_{sq}/4$ in (10). Since the current of this square wave source is i_a, then the current source value of dc side should be $i_a\cdot s_{sq}/4$, and the sum of two current sources matches the result in (15). As for the voltage difference $V_{dc\Delta}$ (V_{mid}) related to i_{mida}, the appropriate ac component injection can help the voltage balancing.

The average model of single-phase 3L-HMMC reveals the relationship of external quantities, forming the outer dynamics. The ac side voltage is composed of CL differential voltage as well as a fundamental frequency square wave. It also illustrates how the internal quantities influence the inner dynamics, such as the common mode current i_{coma} to the $v_{C\Sigma a}$, $v_{C\Delta a}$ and V_{mid}. This is the basis of latter voltage balancing control method.

C. Power Flow Analysis

The power flow of normal operation for the traditional MMC is presented in Fig. 6. The MMC CLs play a role of power exchange between dc and ac side. This implies that the instantaneous power that each phase is exchanging with the dc source is intrinsically independent from the ac side. In order to keep the capacitor energy stable, the dc side power P_{dc2cl} should be compensated by the average ac side power P_{cl2ac}. This is generally called "total energy control" in the literature [1], [2].

The power flow of single-phase 3L-HMMC is shown in Fig. 7. The amplitude of voltages and currents of dc and ac sides are defined as V_{dc}, I_{dc}, V_o and I_o, respectively. So the ac output voltage and current could be expressed as below,

$$v_a = V_o\sin(\omega_o t),\ I_a = I_o\sin(\omega_o t+\varphi) \tag{17}$$

where the power factor phase angle is φ. If the modulation index is defined as $M = 2V_o/V_{dc}$, the active power balance between dc and ac sides yields,

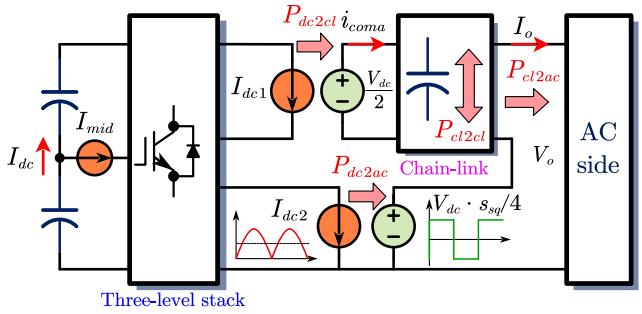


Fig. 7 Power flow of single-phase 3L-HMMC.

$$\begin{aligned} V_{dc}I_{dc} &= \frac{V_oI_o}{2}\cos\varphi = \frac{MV_{dc}}{4}I_o\cos\varphi \\ \Rightarrow I_{dc} &= \frac{MI_o\cos\varphi}{4} \end{aligned} \tag{18}$$

According to Fig. 5, the dc side average current I_{dc} is composed of I_{dc1} and I_{dc2}. The former I_{dc1} equals to the average value of $i_{coma}/2$, and provides the power P_{dc2cl} from dc to ac side through the CL. While the latter I_{dc2} should be the average value of $i_a\cdot s_{sq}/4$.

$$I_{dc2} = \frac{1}{2\pi}\int_0^{2\pi} i_a\cdot\frac{s_{sq}}{4}\cdot d(\omega_o t) = \frac{I_o\cos\varphi}{2\pi} \tag{19}$$

It indicates that partial power is transferred from dc to ac side directly through the three-level stack instead of CL. This power is defined as P_{dc2ac} expressed in (20).

$$P_{dc2ac} = V_{dc}\cdot I_{dc2} = \frac{V_{dc}I_o\cos\varphi}{2\pi} \tag{20}$$

Therefore, the remaining current source I_{dc1} could be derived as,

$$I_{dc1} = \frac{\bar{i}_{coma}}{2} = I_{dc} - I_{dc2} = \left(\frac{M}{4}-\frac{1}{2\pi}\right)I_o\cos\varphi \tag{21}$$

$$P_{dc2cl} = V_{dc}\cdot I_{dc1} = \left(\frac{M}{4}-\frac{1}{2\pi}\right)V_{dc}I_o\cos\varphi \tag{22}$$

It can be observed that if the modulation index satisfies $M = 2/\pi$, I_{dc1} will become zero, which means all the power will flow through the three-level stack. Since the active power delivered by the CL is lower compared to that of the MMC, the dc-link capacitor voltage ripple will be smaller for the 3L-HMMC. This tendency matches the quantitative results in [28].

Similar to MMC, the input power of CL part P_{dc2cl} equals to the output power P_{cl2ac}. The inner circulating power P_{cl2cl} is determined by the common mode current i_{coma}, which consists of the dc component i_{coma_dc} and the ac component i_{coma_ac}. The dc component equals $2I_{dc1}$, and is responsible for the "total energy control". Whereas the ac component i_{coma_ac} will be produced naturally as a result of SM capacitor voltage ripple and CL voltage harmonics. Therefore, a circulating current suppression method is usually required for the MMC [1], [2]. Besides, it could be injected manually for arm capacitor voltage balancing, and higher order harmonics with amplitude I_{coma_h} can be employed to reduce the dc bus current ripple as well.

$$\begin{aligned} i_{coma} &= i_{coma\_dc} + i_{coma\_ac} \\ &= 2I_{dc1} + \sum_{h=1}^{\infty} I_{coma\_h}\cos(h\omega_o t+\varphi_h) \end{aligned} \tag{23}$$

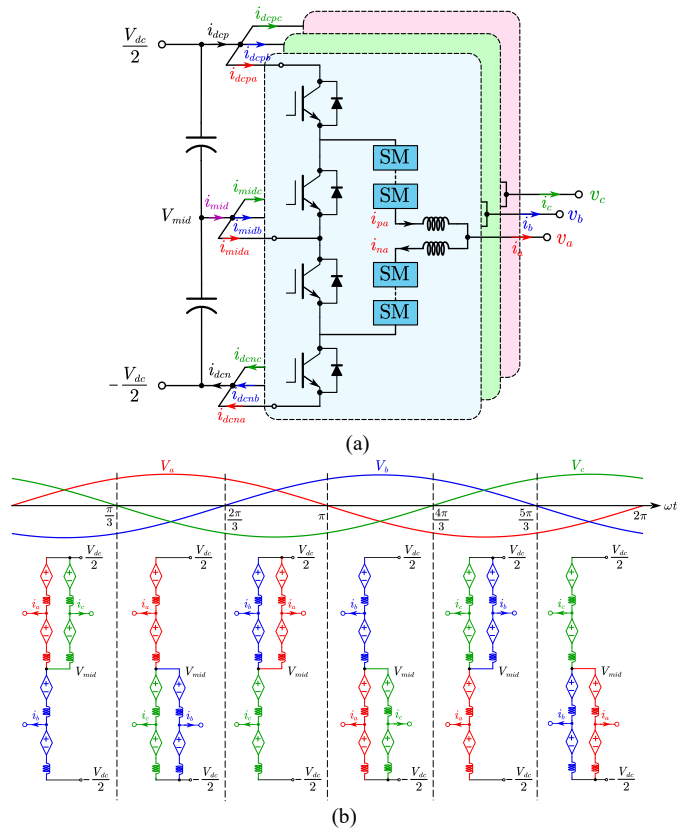


Fig. 8 (a) Three-phase 3L-HMMC and different current variables, (b) three-phase connection during one line-cycle.

III. Three-phase Working Mode

Three-phase 3L-HMMC is connected as in Fig. 8 (a), where the dc side are paralleled and the midpoint is connected together. Applying the working principle of phase *a* to all three phases could obtain the overall working modes of one line-cycle, which can be divided into six segments as depicted in Fig. 8(b). It can be observed that during each segment, two phases are connected in parallel to positive (negative) terminal to share the dc bus current i_{dcp} (i_{dcn}). While the third phase is connected to another terminal and needs to support the whole dc current i_{dcn} (i_{dcp}). Therefore, how to allocate the current distribution among three phases is a freedom and will influence the performance of 3L-HMMC. This section focuses on two types of current allocation method and gives the comparison.

A. Pure Dc Common Mode Current Scheme

Similar to the circulating current suppression in MMC, the simplest common mode current scheme is the pure dc component, which is equally distributed among three phases,

$$i_{coma} = i_{comb} = i_{comc} = 2I_{dc1} = \left(\frac{M}{2} - \frac{1}{\pi}\right) I_o \tag{24}$$

The sum of three-phase midpoint currents can be calculated from (14),

$$\begin{aligned} i_{mid} &= i_{mida} + i_{midb} + i_{midc} \\ &= -\left[s_{sq}(\omega_o t) + s_{sq}\left(\omega_o t - \frac{2\pi}{3}\right) + s_{sq}\left(\omega_o t + \frac{2\pi}{3}\right)\right] 2I_{dc1} \\ &= -2I_{dc1} \cdot s_{sq}(3\omega_o t) \end{aligned} \tag{25}$$

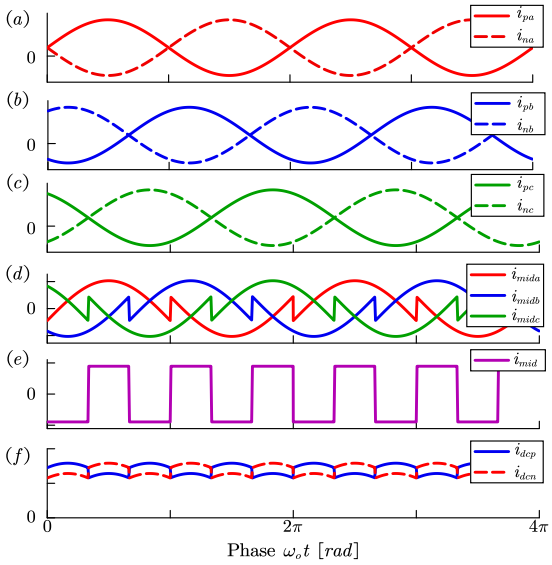


Fig. 9 Three-phase current waveforms with pure dc common mode current, (a) phase *a* arm currents, (b) phase *b* arm currents, (c) phase *c* arm currents, (d) three-phase midpoint currents, (e) total midpoint current, (f) positive and negative dc bus currents.

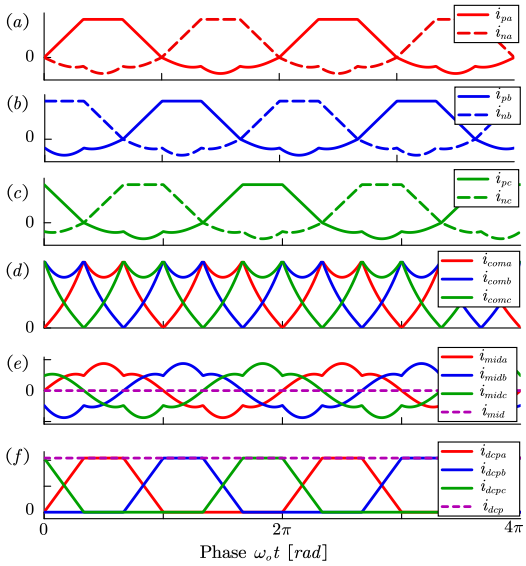


Fig. 10 Three-phase current waveforms with trapezoidal current allocation, (a) phase *a* arm currents, (b) phase *b* arm currents, (c) phase *c* arm currents, (d) three-phase common mode currents, (e) three-phase and total midpoint currents, (f) three-phase and total positive dc bus currents.

Therefore, except for the third harmonic and its multiples, all harmonics are cancelled in the total midpoint current i_{mid} as shown in Fig. 9. This midpoint current equals the difference between negative and positive bus current i_{dcp} and i_{dcn}. And the third order square wave current source will lead to a noticeable voltage ripple on the dc bus capacitor, which should be mitigated by increasing the capacitance.

B. Trapezoidal Arm current Allocation

In order to eliminate the midpoint current, the higher order harmonics could be injected. However, it is hard to design the common current i_{com} directly from (25). But from the dc bus

current point of view, as long as the positive and negative bus current keeps identical and constant, the midpoint current will become zero automatically. Therefore, during each segment the arm current of the single phase which supports bus is determined, while the sum of the left two parallel phase arm currents should keep constant. For example, when $\omega_o t \in (0, \pi/3]$, phase b current is expressed as below according to Fig. 8.

$$i_{nb} = 3I_{dc},\ i_{pb} = i_b + i_{nb} = i_b + 3I_{dc} \tag{26}$$

So during each segment, one phase current could be determined, and there is a freedom to allocate the current between left two parallel phases. As shown in Fig. 10, a trapezoidal current allocation scheme [26] has already been proposed to realize soft switching of IGBT stacks, and the cancellation of three-phase midpoint currents. In this way, the dc bus capacitance could be reduced a significantly, only two small capacitors are required to facilitate the IGBT current commutation. A comparison between pure dc and trapezoidal arm current allocation scheme is shown in Fig. 11. It can be seen that two schemes have the same magnitudes of the dc and first order component, but the even higher order components are injected to the trapezoidal current allocation scheme to eliminate the midpoint current. As for the arm energy variation, which is closely related to the arm capacitor voltage ripple, the trapezoidal current scheme can reduce the amplitude by 13%.

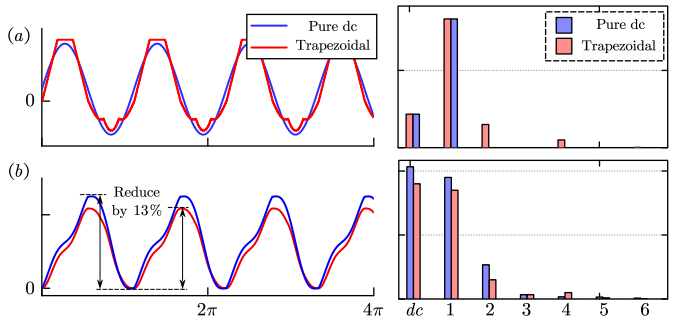


Fig. 11 Comparison between two kinds of arm current allocation schemes, (a) arm current i_{pa}, (b) arm energy variation.

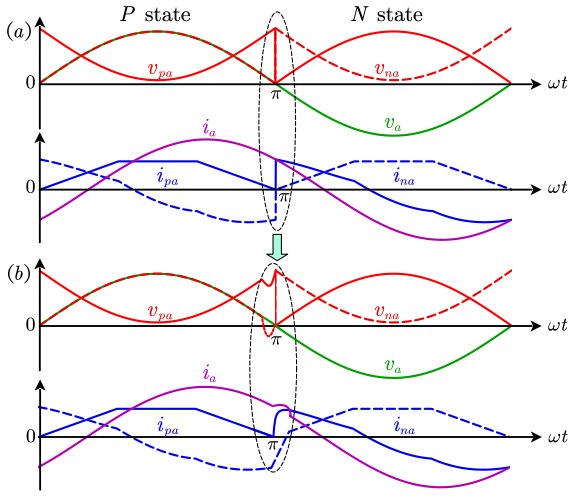


Fig. 12 Phase a waveforms under inductive load with original trapezoidal current scheme, (a) ideal CL voltages and currents, (c) real CL voltages and currents considering arm inductor voltage drop.

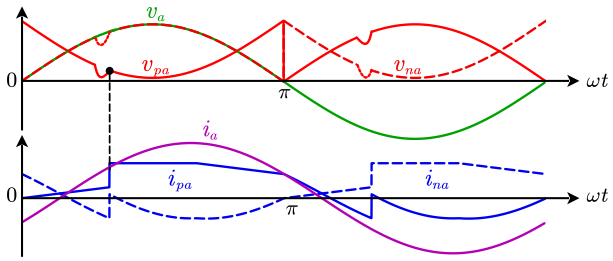


Fig. 13 Improved trapezoidal current allocation scheme.

However, this trapezoidal method must add FB SMs to shape the arm current in non-unity power factor cases. Taking an inductive load as an example, when $\omega_o t = \pi$, phase a is switching from P state to N state as in Fig. 12. The CL voltage is the maximum or minimum value, while both i_{pa} and i_{na} have a positive step at the same time. Since the current is lagging the voltage due to the arm inductor, the actual CL voltages to regulate the arms current should be,

$$\begin{aligned} v_{pa}^* &= 0.5V_{dc} - v_a - L_s \cdot di_{pa}/dt \\ v_{na}^* &= v_a - L_s \cdot di_{na}/dt \end{aligned} \tag{27}$$

It can be seen that v_{na} should be negative enough to track the current step reference, which cannot be satisfied with only HB SMs. As a result, the arm current i_{na} is smaller than the expected value, leading to the distortion in ac output current. In order to solve this issue, the current step point could be moved to the other place such as $\omega_o t = \pi/3$ and $4\pi/3$ as shown in Fig. 13. The constant dc bus current requirement should also be met for the modified trapezoidal arm current allocation. After using this improved method, v_{na} is still positive to support this current step at $\omega_o t = \pi/3$.

IV. Control Method for 3L-HMMC

A. Overall Control scheme

Literature [28] presented a simple control method for single-phase 3L-HMMC. This section will further investigate the control freedoms and the capacitor voltage balancing strategy based on the derived average model. The overall control diagram of 3L-HMMC as a dc-ac inverter is presented in Fig. 14. Similar to the traditional MMC, a hieratical control architecture with inner current loop and outer voltage loop is adopted. The coordination of different control layers guarantees the stable operation of 3L-HMMC.

It is easy to generate the open loop firing signals of three-level stack according to the segment location. But the CL part is relatively difficult, whose internal dynamics have to be controlled to ensure the system stability and a good dynamic performance. According to the average model in Fig. 4, the common mode current of phase j (j=a, b, c) could charge $v_{C\Sigma j}$ through the dc component $i_{comj\_dc}^*$, and change $v_{C\Delta j}$ through the ac component $i_{comj\_ac}^*$. The former represent the average energy, while the latter is equivalent to the CL energy balancing. Two different CL capacitor voltage balancing methods will be illustrated in this section. In addition, the output ac current component i_j^* is obtained though the ac power regulator, which can be controlled by either the proportional-integral (PI) controller on the dq frame, or the proportional-resonant (PR)

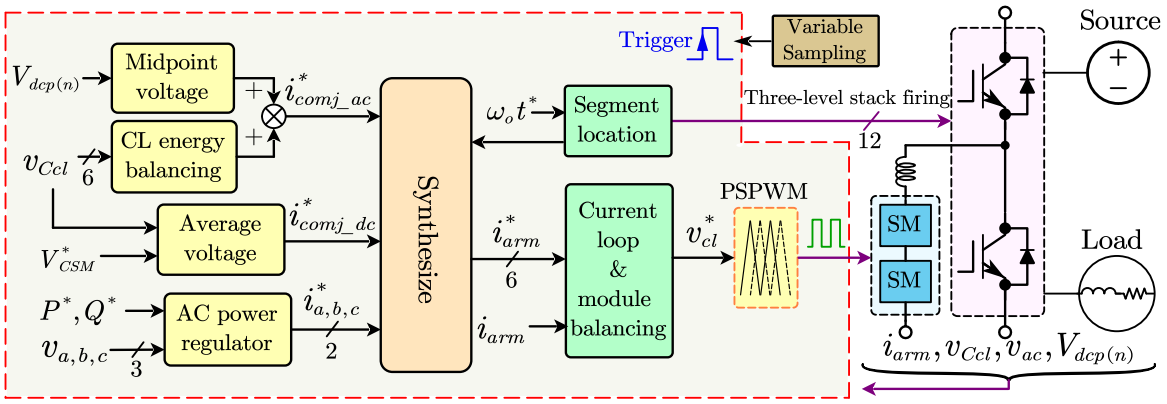


Fig. 14 Overall control diagram of 3L-HMMC.

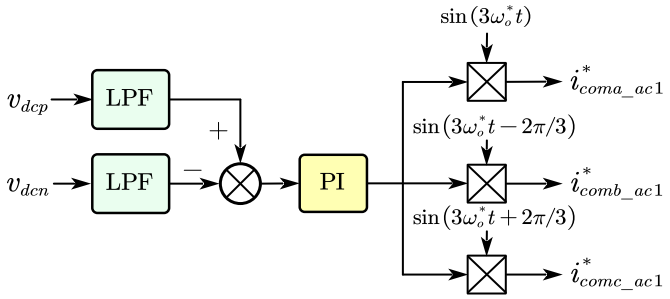


Fig. 15 Midpoint voltage control and common mode current references.

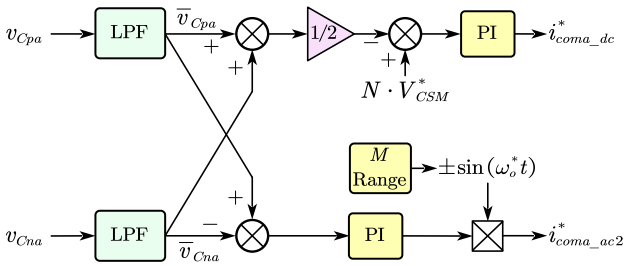


Fig. 16 Common mode current reference for single-phase upper and lower arm capacitor voltage balancing.

controller on the αβ frame. In this way, the arm current reference could be expressed as,

$$i_{arm}^{*} = f(i_j^{*},\ i_{comj\_dc}^{*},\ i_{comj\_ac}^{*},\ \omega_o t),\ j = a,b,c \tag{28}$$

Two kinds of arm current allocation shown in Fig. 10 and 11 can be used here to synthesize the desired arm current. The current loop regulator generates the voltage reference for each CL. After the low level control including SM capacitor voltage balancing and multilevel modulation, the PWM signal for each HB SM could be obtained. The coordination of different level of control guarantees the stable operation of the whole system.

B. Midpoint Voltage Control

According to the power flow diagram in Fig. 7, the dc side capacitor voltage balancing is closely related to the midpoint current. If the ac component is injected to i_{coma}, the midpoint current of phase *a* i_{mida} becomes,

$$\begin{aligned} i_{mida} &= i_a/2 - i_{coma}\cdot s_{sq} \\ &= \underbrace{i_a/2 - 2I_{dc1}\cdot s_{sq}}_{\text{Zero average value}} - \textstyle\sum_{h=1}^{\infty} I_{coma\_h}\sin(h\omega_o t)\cdot s_{sq} \\ s_{sq} &= \sum_{n=1}^{\infty}\frac{1}{n\pi}\sin(n\omega_o t),\ n = 1,3,5,\cdots \end{aligned} \tag{29}$$

S_{sq} could be expanded in the form of Fourier series with only odd terms, and multiplying the odd order common mode current by S_{sq} can generate a dc average value. This dc current can cause the power exchange between the upper and lower dc bus capacitors. In order to avoid the control conflict with the arm energy balancing, the third order component is chosen here. Therefore, the midpoint voltage control diagram can be obtained as Fig. 15.

C. Decoupled CL Capacitor Voltage Balancing

The CL capacitor voltage balancing is also very important for the stable operation of 3L-HMMC. The first method controls the three-phase balancing independently. Considering the different impedance of each arm, the injected common mode current could be different, which means the sum of dc bus current will introduce some ripple. But this method can be applied to two kinds of arm current allocation schemes. According to (13), the dc-link capacitor voltage difference of phase *a* is expressed as,

$$C_s\frac{dv_{C\Delta a}}{dt} = m_{ac\_a}\cdot i_{coma} - \frac{1}{4}m_{dc\_a}\cdot i_a \tag{30}$$

Neglecting the voltage ripple, the second term on the right side of (30) is fixed but the first term could be simplified as,

$$\begin{aligned} m_{ac\_a}\cdot i_{coma} &\approx \frac{V_a - V_{dc}\cdot s_{sq}/4}{NV_{CSM}^{*}}\cdot i_{coma} \\ &= \frac{V_{dc}\cdot i_{coma}}{NV_{CSM}^{*}}\left[\left(\frac{M}{2} - \frac{1}{\pi}\right)\sin(\omega_o t) - \frac{1}{3\pi}\sin(3\omega_o t) - \cdots\right] \end{aligned} \tag{31}$$

Similarly, the odd order ac component can generate a dc value to control the difference of the upper and lower CL dc-link capacitor voltage. It should be noted that if the first order is selected, the polarity of $I_{\text{coma\_1}}$ is also affected by modulation index *M*. Therefore, the diagram of single-phase CL capacitor voltage balancing is presented in Fig. 16. The output sum of the midpoint voltage control and CL capacitor voltage balancing should be the final reference for the $i_{\text{comj\_ac}}^{*}$.

D. CL Capacitor Voltage Balancing With Predictive Control

As explained earlier, three-phase decoupled common mode currents will introduce the dc bus current ripple. So another method for CL capacitor voltage balancing is just using the

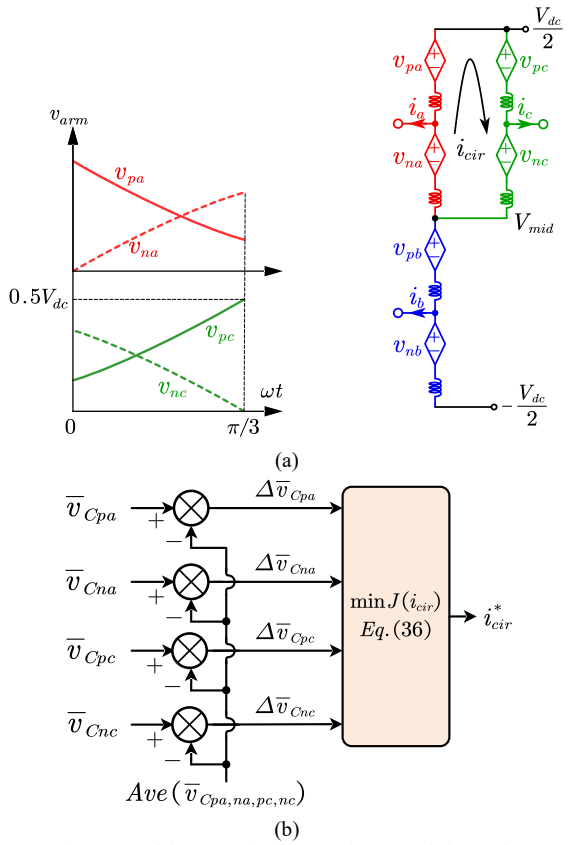


Fig. 17 (a) Phase a and b arm voltage waveforms and three-phase structure when $\omega_o t \in (0, \pi/3]$, (b) control diagram of capacitor voltage balancing.

circulating current inside six arms without influencing the dc and ac sides. Literature [24] proposed to use the circulating current at Z state to balance upper and lower arms. But it requires a negative CL voltage to drive this circulating current according to (3), which means the FB SM should be employed. Besides, the duration of this state is also related to the balancing effect. In order to avoid this problem, injection of discontinuous circulating current during each segment is proposed in this paper.

Since the six segments are symmetric, the example of first segment $\omega_o t \in (0, \pi/3]$ is discussed here. As shown in Fig. 17(a), phase *a* and *c* are paralleled to form a loop, where a circulating current i_{cir} can be injected manually with arbitrary frequency and amplitude. As long as this circulating current flows inside this loop, it only causes energy exchange among four arms without influencing their total energy. So the control target is realizing arm energy equalization.

The dc-link capacitor voltage v_{Ccl} which could be expressed as,

$$v_{Ccl} = \overline{v}_{Ccl} + \tilde{v}_{Carm} \approx \overline{v}_{Ccl} + \frac{N}{C \cdot \overline{v}_{Ccl}} \int v_{cl} \cdot i_{arm} dt \tag{32}$$

The voltage ripple term $\tilde{v}_{Ccl}$ is not controlled here, only the average dc term $\overline{v}_{Ccl}$ is considered in the capacitor voltage balancing. The control target of CL (*pa, na, pc, nc*) capacitor voltage balancing is written as,

$$\Delta\overline{v}_{Ccl} = \frac{1}{4}(\overline{v}_{Cpa} + \overline{v}_{Cna} + \overline{v}_{Cpc} + \overline{v}_{Cnc}) - \overline{v}_{Carm} = 0 \tag{33}$$

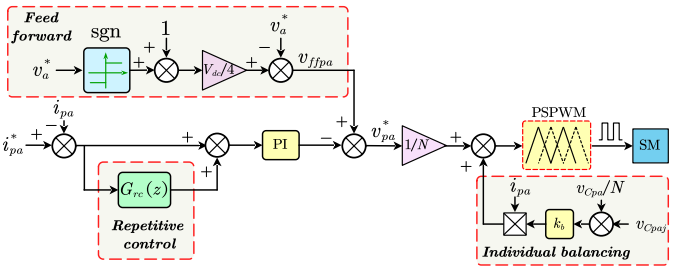


Fig. 18 Block diagram of arm current regulator of upper arm of phase *a*.

Suppose the injected circulating current is i_{cir}, and the control period is T_c (equals to the sampling period). Then in next period the dc average component becomes

$$\overline{v}_{Ccl}[k+1] = \overline{v}_{Ccl}[k] \pm \frac{N \cdot v_{cl} i_{cir}}{C_s \cdot \overline{v}_{Ccl}} \cdot T_c \tag{34}$$

The circulating current does not influence the sum capacitor voltage, which means the CL capacitor voltage difference from the average value becomes,

$$\Delta\overline{v}_{Ccl}[k+1] = \Delta\overline{v}_{Ccl}[k] \pm \frac{N \cdot v_{cl} i_{cir}}{C_s \cdot \overline{v}_{Ccl}} \cdot T_c \tag{35}$$

In order to realize (31), a cost function $J(i_{cir})$ can be defined as,

$$\begin{aligned} J(i_{cir})[k+1] = &\left(\Delta\overline{v}_{Cpa}[k] - \frac{N \cdot v_{pa} i_{cir}}{C \cdot \overline{v}_{Cpa}[k]} \cdot T_c\right)^2 \\ &+ \left(\Delta\overline{v}_{Cna}[k] - \frac{N \cdot v_{na} i_{cir}}{C \cdot \overline{v}_{Cna}[k]} \cdot T_c\right)^2 \\ &+ \left(\Delta\overline{v}_{Cpc}[k] + \frac{N \cdot v_{pc} i_{cir}}{C \cdot \overline{v}_{Cpc}[k]} \cdot T_c\right)^2 \\ &+ \left(\Delta\overline{v}_{Cnc}[k] + \frac{N \cdot v_{nc} i_{cir}}{C \cdot \overline{v}_{Cnc}[k]} \cdot T_c\right)^2 \end{aligned} \tag{36}$$

It is obvious that $J(i_{cir})$ is a quadratic function of i_{cir}, and the minimum $J(i_{cir})$ can be obtained through the derivative. Then the root of this derivative equation corresponds to the optimal circulating current, which could converge four CL capacitor voltages as fast as possible. After obtaining i_{cir} from the input of four CL capacitor voltages as shown in Fig. 17(b), the ac components of two phase common mode currents are deducted,

$$i^*_{coma\_ac2} = -i_{cir},\ i^*_{comb\_ac2} = i_{cir} \tag{37}$$

E. Current Loop Regulator Based on Variable Sampling RC

Compared to MMC, the arm current spectrum of 3L-HMMC is more complicated, which brings the design challenge of the current loop regulator. Therefore, the RC instead of PI controller is selected here to track this irregular but periodic reference. The plug-in RC is very suitable to this case due to due to the effectiveness on periodic error elimination and periodic disturbance rejection.

$$G_{rc}(z) = \frac{k_{rc} z^{-N_s + L}}{1 - Q(z) z^{-N_s}} \tag{38}$$

where k_{rc} is the gain of this repetitive controller, and $Q(z)$ is the stabilization filter, which can improve the robustness. L is the number of samples to compensate the lag of the arm inductor and the digital controller. As a key part of repetitive controller,

TABLE I Electrical parameters of 3L-HMMC system

Parameters	Symbol	Values
Dc bus voltage	V_{dc}	400 V
Ac voltage amplitude (phase)	V_o	127 V
Rated ac frequency	f_o	60 Hz
Ac load	R, L	24 Ω, 2 mH
Arm inductance	L_{arm}	3 mH
Arm equivalent resistance	R_{arm}	0.02 Ω
SM voltage	V_{CSM}	70 V
SM capacitance	C_{SM}	1.32 mF
Number of SM per arm	N	3
Carrier frequency	f_c	14.4 kHz
Delay length of RC	N_s	240

the time delay block z^{-N_S} could postpone the tracking error by a time period of N_sT_c, which is the period of reference signal. So N_s=f_s/f_o, where f_s is the sampling frequency and f_o is fundamental ac line frequency. However, f_s is not always an integral multiple of f_o, such as 1-Hz frequency fluctuation of the 60 Hz power grid, or the new generation aircraft power supply in the range of 360-900 Hz. In these cases, the RC with constant sampling frequency becomes ineffective to track the reference. Therefore, a variable sampling RC is adopted in this paper [31].

The current loop of upper arm of phase *a* is presented in Fig. 18. Besides the repetitive controller, the CL feed forward voltage based on (8)-(9) is added to help improve dynamic response and stability. While the individual balancing control is responsible for the SM level capacitor voltage balancing. The phase-shift PWM (PS-PWM) is employed for multilevel modulation to increase equivalent switching frequency.

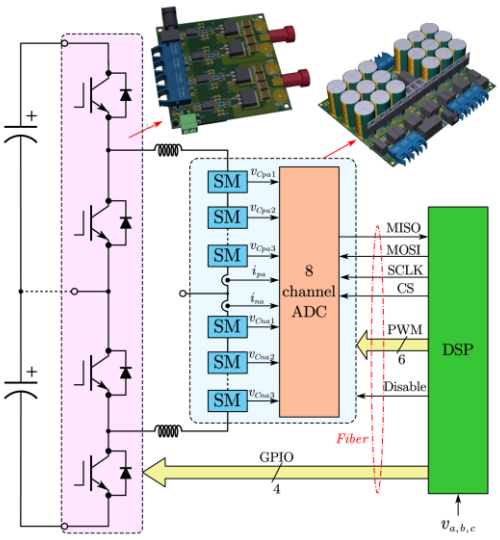
V. Experimental Verification

In order to verify the effectiveness of proposed control scheme, a scale-down three-phase 3L-HMMC prototype was built and the electrical parameters are given in Table I. Single-phase 3L-HMMC configuration is presented in Fig. 19(a) and the picture of whole experimental platform is shown in Fig. 19(b). The SM uses 250 V MOSFET as the switching device while three-level stack uses 450 V discrete IGBT. Each phase employs an 8-channel ADC to measure 6 SM capacitor voltages and two arm currents, and send them back to the central controller TMS320F28388 through SPI communication. And all PWM and communication signals are transmitted via fiber. Six inductors are connected between the arm boards and the three-level stack boards.

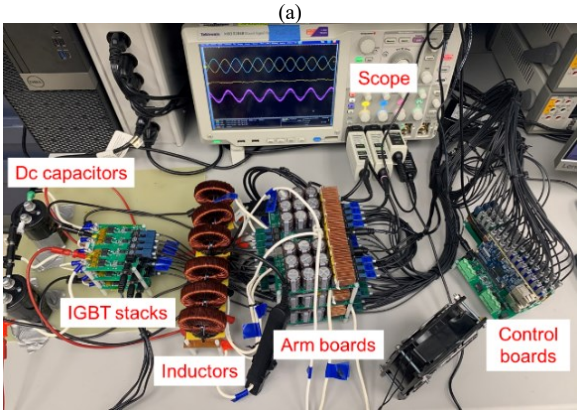
A. Control parameters design

As a key part of system control, the parameters of RC regulator should be designed carefully to guarantee system stability. The equivalent block diagram of the arm current loop is shown in Fig. 20. In this paper, the cascade instead of parallel structure is adopted due to the easier system stability "plant" model. Based on this diagram, the closed loop transfer function can be derived as,

$$i_{arm} = \frac{P(z)\left[z^{N_s} - Q(z) + k_{rc}z^{L}\right]}{z^{N_s} - Q(z) + k_{rc}z^{L}P(z)} \cdot i^{*}_{arm}$$
$$P(z) = \frac{G_{PI}(z)G_p(z)z^{-1}}{1 + G_{PI}(z)G_p(z)z^{-1}} \tag{39}$$



(a)



(b)

Fig. 19 (a) Single phase 3L-HMMC structure, (b) Prototype picture of three-phase 3L-HMMC.

where $P(z)$ represents the closed loop transfer function of the current loop with traditional PI controller. And the discrete transfer function of the arm plant with ZOH transformation is [32],

$$G_P(z) = \frac{1}{R_{arm}}\left(\frac{1 - e^{-R_{arm}T_s/L_{arm}}}{z - e^{-R_{arm}T_s/L_{arm}}}\right) \tag{40}$$

After adding the repetitive controller, the sufficient condition [33] for the system stability is keeping all the roots of the characteristic equation inside the unit cycle as in (41).

$$|H(z)| = |Q(z) - k_{rc}z^{L}P(z)| < 1 \tag{41}$$

This equality is influenced by the low pass filter $Q(z)$, phase lead unit z^{L} and repetitive gain k_{rc}. Usually, the low pass filter is a comb filter with unit gain at low frequency and no phase delay. The filter expressed in (42) is selected in this paper.

$$Q(z) = \frac{z + 6 + z^{-1}}{8} \tag{42}$$

The phase lead number L is selected as 6 to perform phase compensation for $P(z)$. Fig. 21 shows that when f_o=60 Hz and f_s=14.4 kHz, z^6 could perfectly cancel the phase delay from original system.

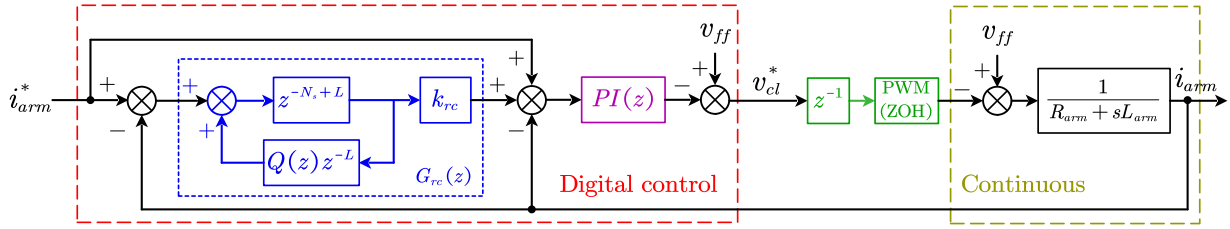


Fig.20 Equivalent block diagram of arm current loop.

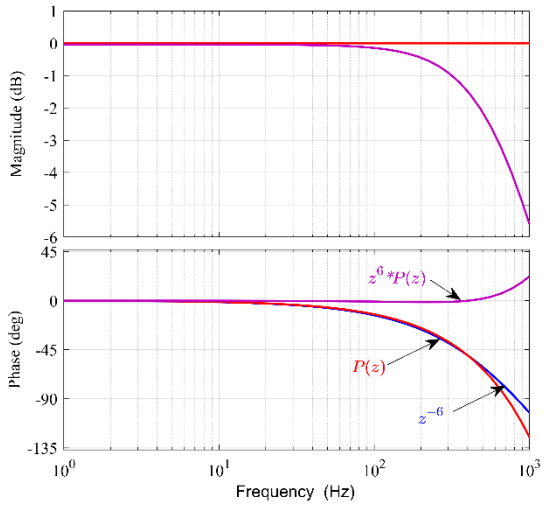


Fig. 21 Bode plot of $P(z)$, z^{-6} and $z^6P(z)$.

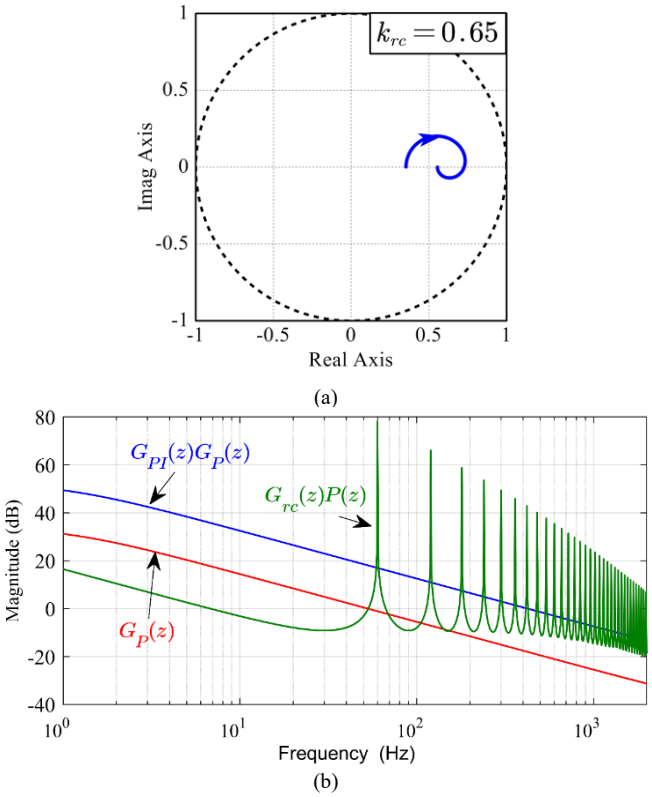
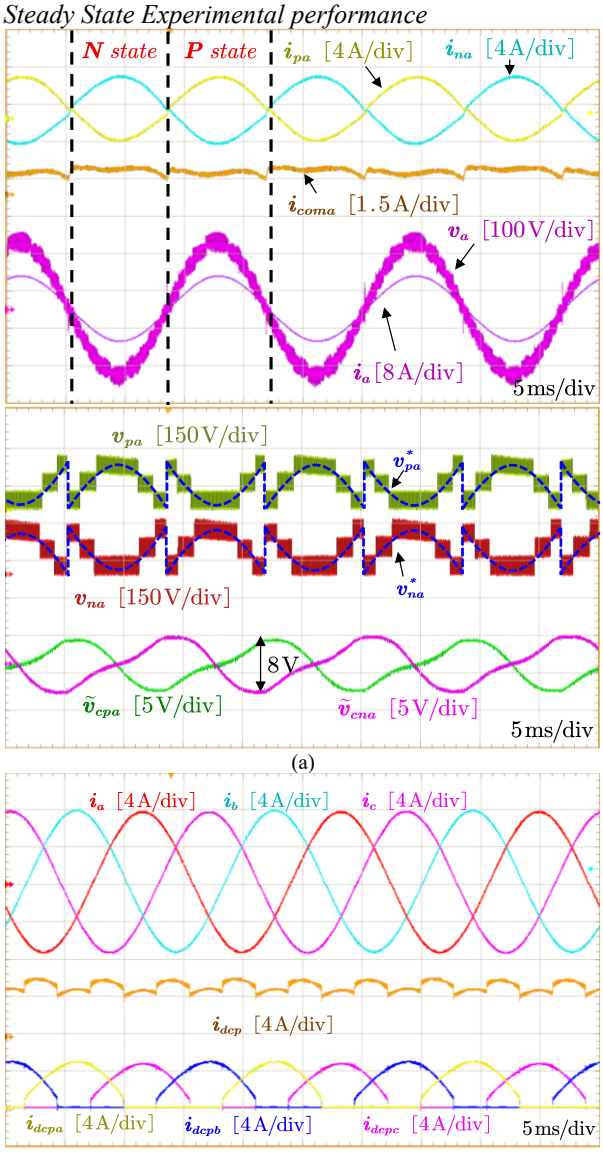
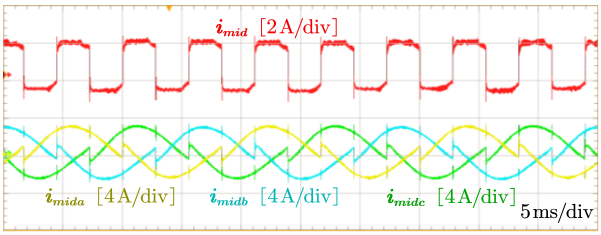


Fig. 22 (a) Nyquist plot of $H(z)$ with k_{rc} = 0.65, (b) Bode plot of open-loop transfer function.

The left repetitive gain k_{rc} greatly influences the controller performance. Lager gain can bring a faster error convergence speed but smaller stability margin. Then the Nyquist plot of $H(z)$ with k_{rc}=0.65 is shown in Fig. 22 (a), which is inside the unit cycle. The corresponding Bode plot of open-loop transfer function of plant model $G_p(z)$, PI system $G_{pi}(z)G_p(z)$ and RC system $G_{rc}(z)P(z)$ are presented in Fig. 22 (b). It should be noted that RC can adaptively tune the gain characteristics to obtain a better performance without being affected by the variation in the fundamental ac line frequency.

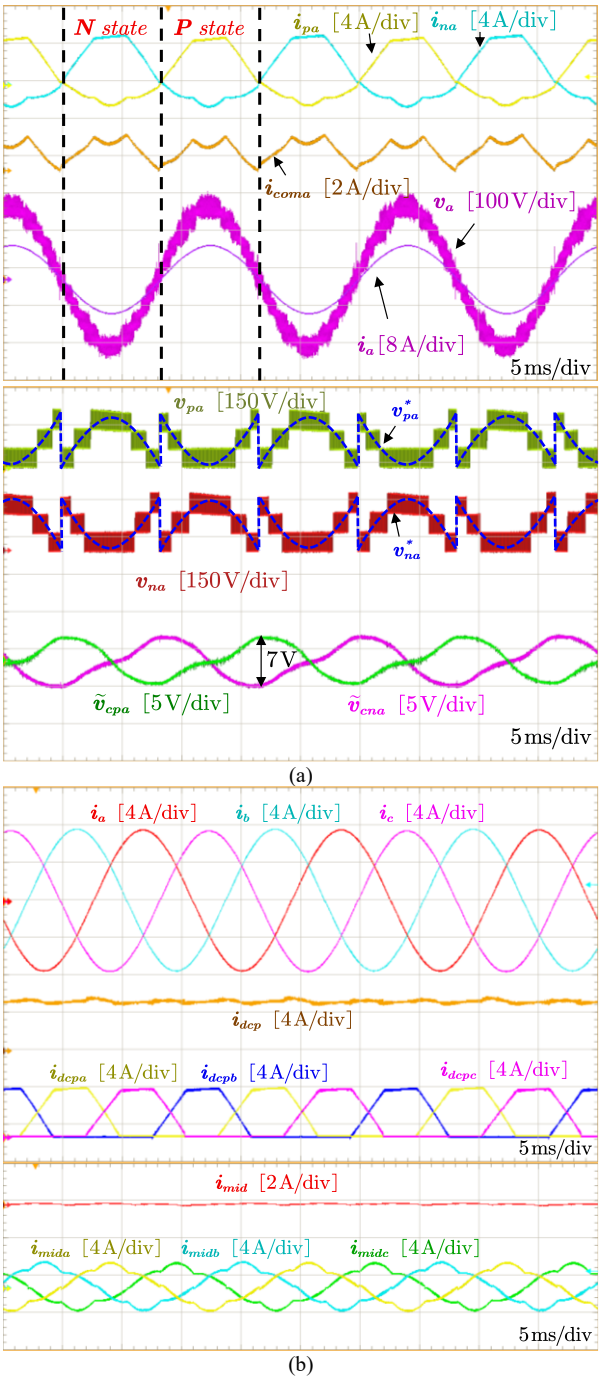
B. *Steady State Experimental performance*





(b)

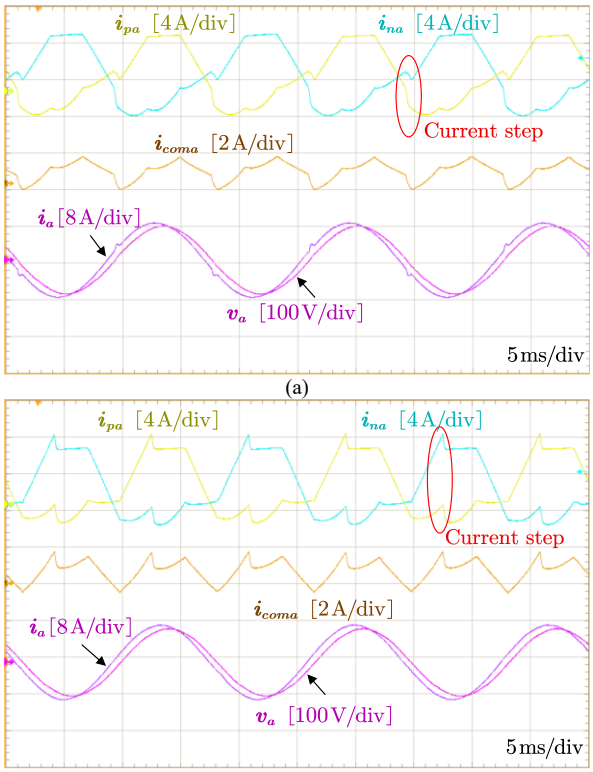
Fig. 23 Waveforms of pure dc common mode current scheme, (a) arm voltages and currents of phase *a*, (b) three-phase ac side, dc side and midpoint currents.



(a)

(b)

Fig. 24 Waveforms of trapezoidal current scheme, (a) arm voltages and currents of phase *a*, (b) three-phase ac side, dc side and midpoint currents.



(a)

(b)

Fig. 25 Phase *a* waveforms with a load of 24 Ω paralleled with 30 μF, (a) using original trapezoidal current scheme, (b) using improved current allocation.

Steady-state operation of the experimental platform at the fixed output voltage, load and capacitor voltage is implemented as shown in Fig. 23. The first test uses the pure dc common mode current scheme, which has similar arm current waveforms to the conventional MMC. It can be seen that the common mode current is almost stable except some distortion at the working sate changing point. And the average value could match the calculation results 1 A of (24), thus validating the derived average model. Since there are 3 SMs per arm, the arm voltage level is 4, but the ac side voltage level is 13 due to the insertion of square wave. With the help of three-level stack, the maximum arm voltage is only half dc bus voltage. As explained earlier, this kind of current scheme will introduce third order harmonics in the dc bus and midpoint currents as in Fig. 23(b). Therefore, the dc bus capacitor should be large enough to suppress the low frequency voltage ripple.

The second test employs the trapezoidal current scheme as shown in Fig. 24. The common mode current is injected even harmonics, but the dc average value keeps the same 1 A. The dc-link capacitor voltage ripple is also 13% percent lower than the pure dc current scheme. The arm voltage and ac side voltage level is the same. But benefiting from the trapezoidal arm current allocation, the dc bus current is constant and midpoint current is almost zero. So the dc bus capacitor could be very small for only IGBT stack commutation purpose.

According to previous analysis, the CL voltage will be out of range to generate the arm current step at non-unity power factor. It can the seen that the current distortion will occur in ac side as shown in Fig. 25(a). To solve this issue, the current step

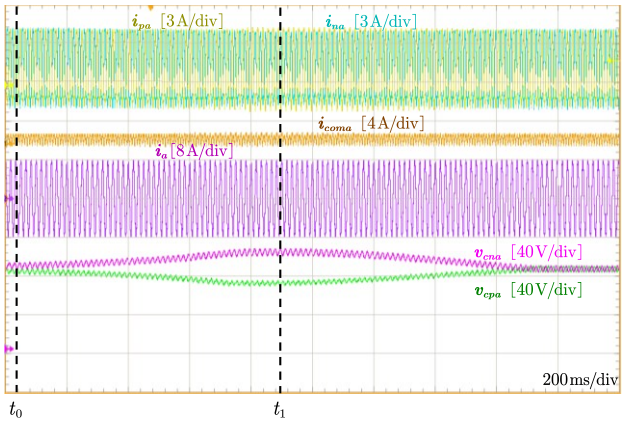


Fig. 26 Illustration of the effectiveness of the CL capacitor voltage balancing scheme.

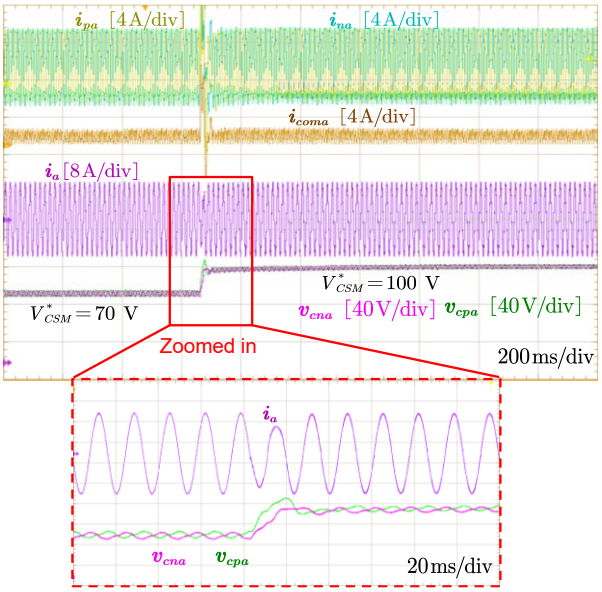


Fig. 27 Waveforms of capacitor voltage reference increase.

point could be moved not overlapping with voltage step point. And it can be seen in Fig. 26(b) that the total harmonic distortion (THD) of ac current becomes much smaller.

In order to verify the effectiveness of CL capacitor voltage balancing, another set of experiment is implemented as shown in Fig. 26. At t_0, this balancing strategy is disabled and it can be observed that upper and lower capacitor voltages start to diverge and the system tends to be unstable. Then at t_1, the balancing strategy is applied again, which makes two capacitor voltages converge quickly.

C. Dynamic Experimental performance

To evaluate the system performance completely, the dynamic response experiments are also implemented. In first experiment, the capacitor voltage reference is changed from 7V to 100V. It can be seen in Fig. 27 that the common mode current changes simultaneously to charge the SM capacitors according to the overall capacitor voltage control, while the output currents keep almost stable. The capacitor voltage increases to the reference value in one fundamental period, indicating the good design of voltage loop.

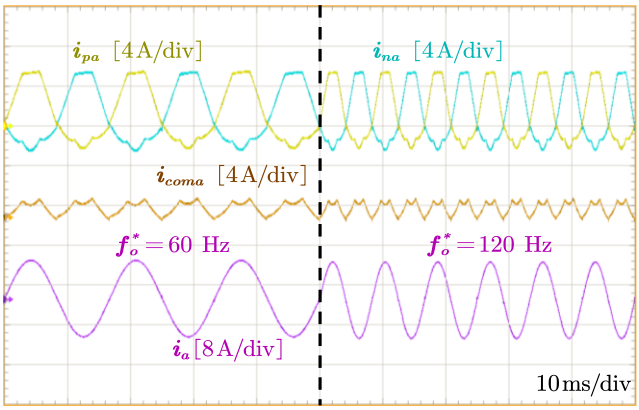


Fig. 28 Waveforms of output frequency increase.

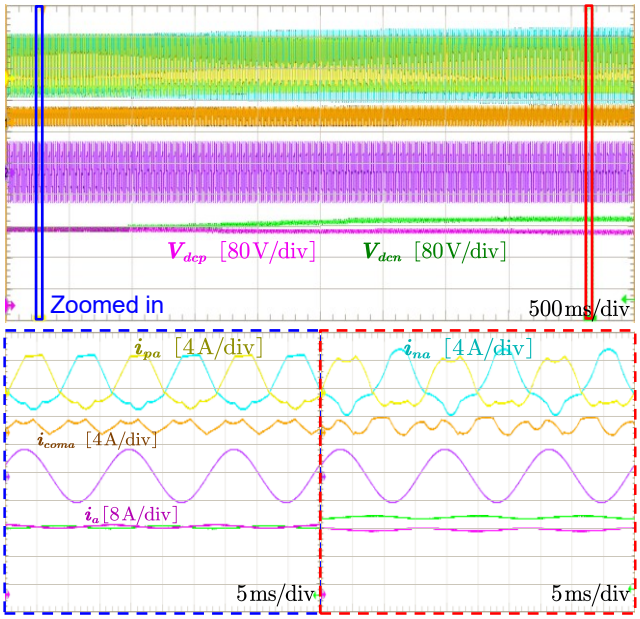


Fig. 29 Waveforms of midpoint voltage reference increase.

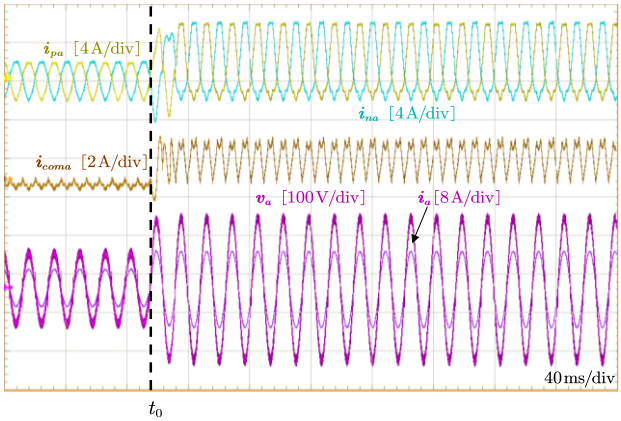


Fig. 30 Waveforms of output ac voltage step.

In another experiment, the load frequency reference has a step change (from 60 Hz to 120 Hz). Due to the variable sampling RP controller, the sampling frequency is also increased from 14.4 kHz (same with SM switching frequency) to 28.8 kHz, and the delay length N_s could keep constant. It can

be seen in Fig. 28 that the ac current transits to the steady state very quickly.

In next experiment, the midpoint voltage reference is changed to verify the effectiveness of third order common mode current injection. In the normal state, the midpoint voltage reference is set as 0, so that v_{dcp} equals v_{dcn}. After changing the reference to -5 V, more harmonics are injected to the upper and lower arms. It can be observed from Fig. 29 that v_{dcp} becomes smaller and v_{dcn} becomes larger. The deviation stables at 5V eventually, and the arm currents are not the trapezoidal shape now, but the ac side current is still sinusoidal.

Finally, an experiment of output ac voltage step at t_0 is conducted as shown in Fig. 30. Since the output load is resistor, the ac current is proportional to the output voltage. When the modulation index is increasing, the average value of common mode current is also increased based on (21).

CONCLUSIONS

This paper gives a detailed average model of 3L-HMMC, which revels the internal relationship between the three-level stacks and the CLs. According to the derived model, one part of power is directly transferred from the dc side to the ac side through the IGBT stack, so that the energy variation of CL becomes smaller. And benefiting from the insertion of square waveform in ac side, the ac voltage level is $4N$+1 instead of $2N$+1 in MMC. The pure dc and trapezoidal current allocation scheme are compared and it shows that the later has better performance in terms of dc side current as well as SM capacitor voltage ripple. Furthermore, a new trapezoidal current scheme is proposed to improve the ac current distortion at non-unity power factor. A variable sampling RC is adopted for the current loop and the control parameter design method are provided for system stability. Finally, the effectiveness of this control structure is verified on a 3L-HMMC prototype in the laboratory. The steady-state and dynamic operation experimental results confirm the good performance of the system and feasibility of proposed control strategy.

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