The effect of bias stress on the performance of amorphous InAlZnO-based thin film transistors

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Abstract

In amorphous InAlZnO (a-IAZO), the addition of the third cation of Al further slows the crystallization kinetics of In_2O_3 and enhances amorphous phase stability, compared to the binary cation system of InZnO. In addition, substantially high carrier mobilities of a-IAZO are obtained, in its un-annealed state: Hall mobility of 30-50 cm^2/Vs at a high carrier density regime ($>\sim10^{18}$ $/cm^3$) and thin film transistor (TFT) field effect mobility of ~8-15 cm^2/Vs at a low carrier density regime ($<\sim10^{16}$ $/cm^3$). Gate bias stress stability of IAZO TFTs is investigated with positive and negative gate biases over time. Due to the channel depletion of n-type IAZO when negative gate biases applied, no performance instabilities were identified. However, with positive gate bias stress (PBS) conditions (30 V), the threshold voltage (V_T) shifts towards higher voltages during the initial 100 s and then no significant changes in V_T are observed during the remaining time, over 10^5 s of the dependent measurements. The TFT field effect mobility shows a similar trend: increases from 7.64 to 11.74 cm^2/Vs within the first 100 s and then is saturated. It is identified that the PBS-induced device parameter variations are attributed to an increase and saturation of trap density at the channel/dielectric interface.

1. Introduction

Over the past two decades, amorphous oxide semiconductors (AOSs) have earned huge attention for their use in various electronic and optoelectronic devices such as thin film transistors (TFTs)[1-3], photovoltaic cells[4], oxide-based p-n heterojuntions[5], and memristors[6-8]. High carrier mobilities, excellent visible regime optical transparency, and low-temperature processing capability lead to tremendous attention and implementation of AOSs into these devices[9]. In particular, ultra-high definition and curved/flexible displays have exploited these attractive properties of AOS materials for a backplane technology used in liquid crystal displays and organic light-emitting diodes[10, 11]. A backplane is an assembly responsible for driving a display where TFTs as pixel driving elements are a key component which determines the refresh rate, power efficiency, and resolution of a display. Compared to the conventional amorphous Si (<1 cm^2/Vs), the mobility of AOSs is much higher (typically 5-30 cm^2/Vs, depending on the number of cation species and compositions), which, therefore, enables faster switching/refresh rate of next generation displays[12].

Indium oxide-based multi-cation AOSs, such as InZnO (IZO) and InGaZnO (IGZO), have been leading AOS electronics. A binary cation AOS of IZO demonstrated advantages of higher TFT field effect mobility of ~15-20 cm^2/Vs in the as-fabricated (or room-temperature processed) state[2, 13] and ~20-40 cm^2/Vs after annealing at ~200 °C[2, 13]. In the binary cation AOS of IZO, the addition of ZnO (10 wt%) to In_2O_3 substantially enhances amorphous phase stability of IZO by reducing the crystallization kinetics since the solubility of divalent tetrahedrally coordinated Zn-O is limited in the octahedrally coordinated In-O bixbyite structure and the excess ZnO impedes the crystallization of In_2O_3 (or enhances the amorphous stability)[14-16]. However, it has been

known that the addition of ZnO does not play any role in carrier generation or annihilation in IZO. Therefore, the carrier density of IZO is similar to that of In_2O_3 that ranges from 10^{17} to 10^{20} /cm^3, depending on O_2 content during processing. A representative ternary cation AOS, IGZO, is able to effectively suppress the carrier generation and limit the carrier density to the range of 10^{15}-10^{19} /cm^3, which is more favorable for TFT applications to achieve low off-state currents. However, the third cation, Ga significantly disrupts the carrier transport in IGZO since the added third cations work as ionized impurity scattering sites. The resulting carrier mobility of IGZO, particularly in the unannealed state, is as low as <0.5-2 cm^2/Vs [17-19], which is much lower than those of room-temperature processed binary cation AOS (IZO; 15-20 cm^2/Vs). To enhance the carrier mobility of IGZO, annealing at temperatures higher than 400 °C is often employed; however, the necessary annealing compromises the low temperature processing capability and, hence, limits potential low temperature applications such as flexible electronics. Therefore, it is needed to develop AOS materials that effectively suppress carrier generation and can be manufactured with low thermal budget processes while maintaining high carrier mobility. We recently reported on a room-temperature processed ternary cation AOS of InAlZnO (IAZO), of which the carrier suppression capability and high carrier mobility of ~8-15 cm^2/Vs without annealing were exhibited[20, 21].

In practical applications for display backplane TFT devices, stable characteristics, such as field effect mobility, threshold voltage (V_T), on-state current, and drain current on/off ratio, need to be maintained during device operations when required bias is applied. Reports are available in the literature on the mechanisms for threshold voltage stability and other characteristics including field effect mobility of AOS-based TFTs under gate bias (V_G) stress[22, 23]. In general, longer stress

times and larger V_G lead to larger V_T shifts[24]. These shifts could be related to the creation of defect states near the channel/dielectric interface or the trapping of charges in the dielectric layer[24, 25].

The mechanisms of bias stability issues were initially proposed based on the amorphous Si framework [26]. Cross *et al*. [27] reported that low field bias stress ($V_G \leq 30$ V) produces a parallel V_T shift in the transfer characteristics with minor changes in the subthreshold slope (S.S), where the primary mechanism was believed to be the charge trapping at the channel/dielectric interface[28]. It is also reported that trapped charges in the dielectric also shift V_T since the channel carrier density changes due to the charge traps in the dielectric, where the required energy to release the trapped charges in the dielectric is higher than those trapped at the channel/dielectric interface[27]. Therefore, the recovery of V_T shifts due to the charge traps in the dielectric needs post-treatments such as thermal annealing, while V_T shifts due to the channel/dielectric interfacial charge traps are recovered over time without any treatments[27]. The instability under high gate bias ($V_G \geq 30$ V) and after long stress times is attributed to a defect generation/annihilation process within the oxide semiconductor channel, in which the defects work as charge trapping centers. For the defects or impurities-dependent V_T shift mechanisms, Jeong *et al*.[26] investigated the effect of dynamic interaction between the exposed backchannel and the ambient atmosphere, from which it was claimed that adsorbed oxygen can capture electrons from the conduction band, leading to a huge positive ΔV_T due to the reduction in channel carrier density. Positively charged water molecules (after donating electrons to the channel) on the IGZO surface can also result in a positive V_T shift since during desorption of the water molecules, electrons are recaptured by the molecules[26]. These bias stabilities of AOS TFTs can vary from AOS materials, depending on their compositions as well the performance and quality of the dielectric material[24, 29].

In addition to our recent reports on a ternary cation AOS of IAZO and its implementation in TFT devices[20, 21], this study further advances the mechanisms for carrier generation/annihilation in IAZO and gate bias stress stability/instability in IAZO-based TFTs. Characteristics of room-temperature processed IAZO films are investigated and the carrier transport behaviors are discussed. In order to investigate the effect of negative/positive gate bias stress over time on the device performance, the V_T, field effect mobility, sub-threshold slope, and trap density are compared as a function of bias stress time.

2. Experimental

Thin films of IAZO were deposited on Si and glass substrates at room temperature using co-sputtering of a sintered InZnO target and an aluminum (Al) metal target. As previously reported by our group, mixed sputter powers were used for the film preparation, where a dc power of 20 W was used to process IZO and an rf power of 15 W was applied for Al incorporation into the IZO matrix. The rf sputtering of Al was intended to limit the Al content in the resulting IAZO films since a large amount of the third cation species is known to be segregated or works as impurity scattering centers that impede the free carrier transport. Prior to depositions, the sputter chamber was pumped down to a base pressure of 5-7 $\times 10^{-8}$ kPa or below, and sputter targets were pre-sputtered for five min to remove any surface contaminants on the targets and to ensure a uniform sputter gas flow in the chamber. IAZO films were processed in pure Ar or mixed sputter gas conditions and the chamber working pressure was maintained at 2.0×10^{-4} kPa during depositions. After completion of the sputter depositions, samples were rested in the ambient

conditions of the chamber for more than five min to cool down any generated heat during the process.

Characterizations of the resulting IAZO films were thoroughly evaluated. The amorphous/crystalline structure of IAZO films was investigated through x-ray diffraction (XRD) analysis in a Malvern Panalytical Empyrean X-ray Diffractometer with a theta-two theta coupled scan mode. XRD investigations were made through Cu Kα radiation (λ=1.54 Å) at a generator voltage of 45 kV and a tube current of 40 mA. Microstructure morphology of IAZO films was imaged through scanning electron microscopy (SEM) with a ThermoFisher Scientific Teneo SEM, featuring a Trinity Detection System. Surface topographic images were obtained by atomic force microscopy (AFM) in a Veeco Dimension 3100 microscope via non-contact tapping mode through a Si tip with a frequency of 330 kHz. Energy dispersive x-ray spectroscopy (EDS), which is attached to the Thermofisher Teneo SEM, was used to determine the elemental composition of the resulting IAZO films, from which the elemental ratio of In, Zn, and Al was found to be In:Zn:Al=1:0.4:0.2 in atomic%. Optoelectronic properties of IAZO films were evaluated through UV-Vis measurements with a Varian Cary 50 spectrometer in the visible regime of wavelengths (300-900 nm). A blank glass substrate was used for a baseline scan to exclude the substrate glass information in the resulting UV-Vis spectra. Film thickness was measured with a multiwavelength ellipsometer (FilmSense FS-1) using an incident and detection angle of 65°. The electrical properties (e.g., carrier concentration, mobility and resistivity) of IAZO films were evaluated through a custom-built Hall Effect system in the van der Pauw configuration where Hall measurements were conducted with a small specimen current (~1 nA),

a magnetic-field variable electromagnet (0-2 Tesla, GMW Associates) and a bipolar power supply (KEPCO Inc.).

Amorphous IAZO-based TFTs were fabricated in a bottom-gated device structure on SiO_2/Si substrates where thermally grown SiO_2 (50 nm) was used as the gate dielectric and heavily-doped Si (0.003-0.005 Ωcm) was employed as the gate electrode. Channel IAZO was co-sputtered from IZO and Al targets with the sputter conditions described above except for the sputter gas composition of Ar/O_2= 80/20 in volume ratio. For the source and drain metallization, Al (100 nm) was sputter-deposited on the channel IAZO with pure Ar as the sputter gas. These channel and metallization layers were deposited at room temperature. To define channel and metallization patterns, in-situ shadow masks were used. A semiconductor parameter analyzer (Agilent 4155B) was used to evaluate fabricated amorphous IAZO-based TFTs in a light-tight probe station under ambient conditions. More than 15 devices were fabricated and tested to collect reliable data and provide evidence of consistency.

3. Results and discussion

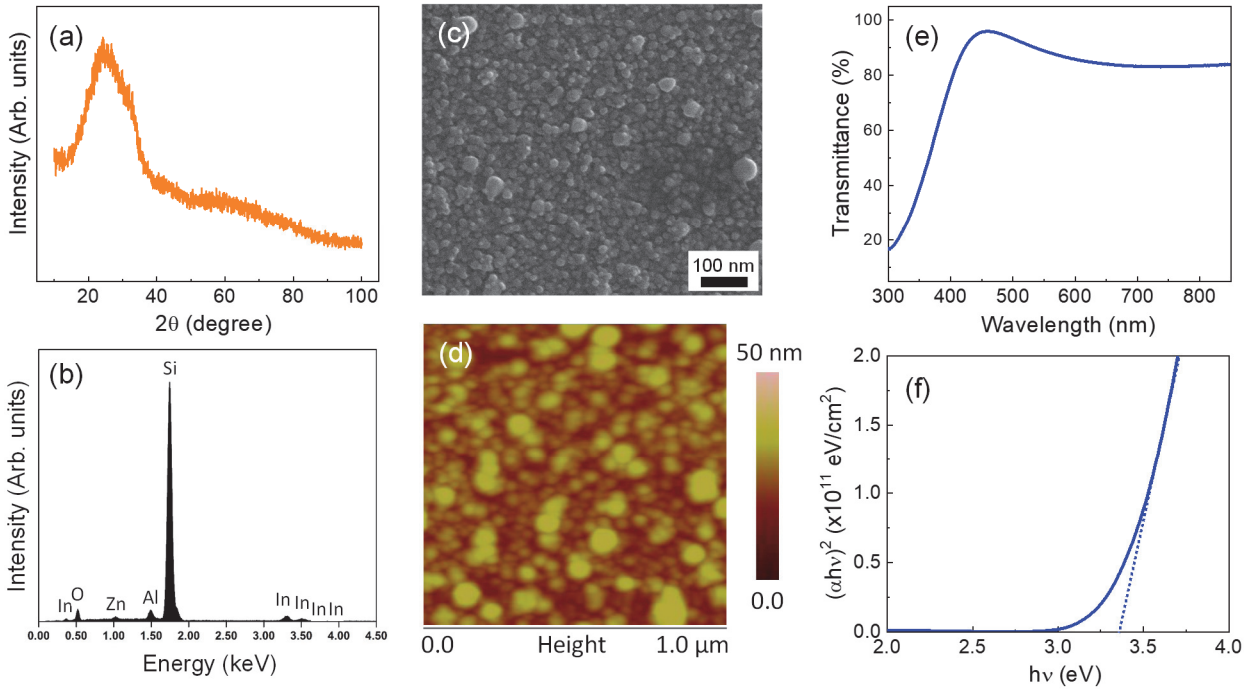

Figure 1. Characterizations of amorphous IAZO films. (a) XRD diffractogram, (b) EDS composition analysis, (c) plan-view SEM image, (d) AFM surface topographic image, (e) UV-Vis optical transmittance in the visible regime, and (f) its associated Tauc plot of $(\alpha h\nu)^2$ vs hν for the direct transition.

The amorphous/crystalline structure of the resulting IAZO was evaluated through XRD analysis and a typical XRD diffractogram is shown in **Figure 1**a. No crystalline peaks are observed in the diffraction pattern where the glass substrate appears as the broad peak at diffraction angles of 15°<2θ<35° and the amorphous IAZO is seen as a shoulder on the side of the amorphous glass peak at about 2θ=~32° [20]. The elemental composition of IAZO films was identified using EDX as shown in Figure 1b, by which the cation atomic ratio of IAZO is determined to be In:Al:Zn= 1:0.4:0.2. An SEM plan-view image in Figure 1c displays the surface microstructure of the IAZO films. It should be noted that the circular-shape features of which the size is approximately 20-50 nm are not attributed to crystalline domains since the XRD diffractogram presented in Figure 1a identified the resulting IAZO films are in the amorphous state. An AFM surface topograph in Figure 1d concurs with the SEM image, exhibiting similar microstructures. The surface roughness

of the IAZO films is measured from the AFM image to be ~ 4.16 nm. UV-Vis optoelectronic properties were investigated on IAZO films (100 nm thickness) in the visible regime (300-900 nm) and the results are shown in Figure 1e-f. The visible range transparency is as high as 93% (at 500 nm) in Figure 1e and its associated Tauc plot for the direct bandgap transition is displayed in Figure 1f. The optical bandgap of IAZO films is determined to be ~3.4±0.13 eV by an extrapolation of the linear portion of the Tauc plot to the zero absorption (i.e., x-axis).

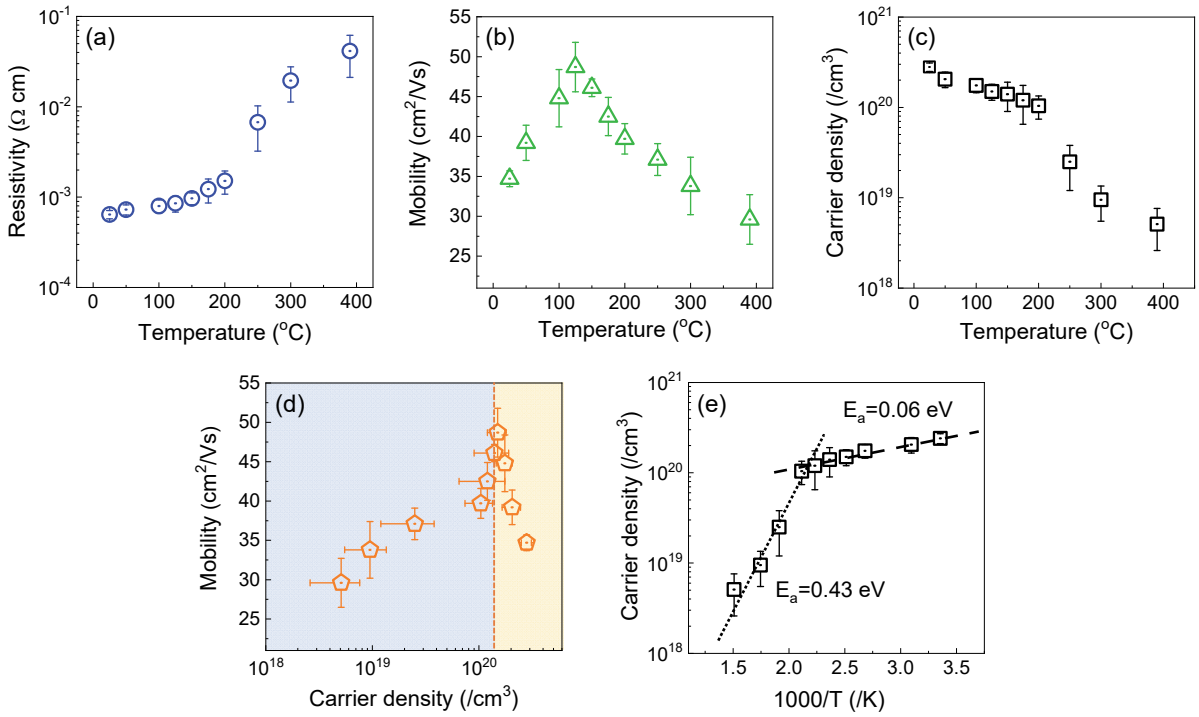

Figure 2. Electrical properties of IAZO as a function of annealing temperature. (a) resistivity, (b) carrier mobility, (c) carrier density, (d) plot of carrier mobility vs carrier density for carrier transport analysis, and (e) Arrhenius plot for carrier annihilation (generation) with extracted activation energies for two different mechanisms.

The electrical properties of the IAZO films were evaluated using Hall Effect measurements. As a figure of merit, the lowest resistivity of 6.46×10^{-4} Ωcm is obtained at the pure Ar sputter gas condition, which is slightly higher than that of approximately 5.5×10^{-4} Ωcm for amorphous

InZnO[30] and 2-3×10^{-4} Ωcm of crystalline InSnO (known as ITO)[31]. The effect of air annealing on the resistivity was monitored as a function of annealing temperature. In **Figure 2**a, the resistivity gently increases with increasing temperature from 6.4×10^{-4} Ωcm at room temperature (or unannealed) to 1.5×10^{-3} Ωcm at 200 °C. However, a substantial increase in resistivity is observed in annealing at temperatures higher than 200 °C. In order to identify the mechanism of the conductivity change in response to annealing, the carrier mobility and carrier density were also investigated as a function of annealing temperature. It should be noted that at a lower temperature regime below 125 °C, the carrier mobility, exhibited in Figure 2b, increases from 34.7 to 48.7 cm^2/Vs while the resistivity increases. Then, at annealing temperatures higher than 125 °C, the carrier mobility monotonically decreases to 29.6 cm^2/Vs at an annealing temperature of 400 °C. Associated changes in carrier density in response to annealing are plotted with temperature in Figure 2c. The carrier density decreases in a mild manner initially from 2.8×10^{20} /cm^3 to 1.1×10^{20} /cm^3 at 200 °C and then starts decreasing fast at temperatures higher than 200 °C. A relationship between carrier mobility and carrier density of IAZO is plotted in Figure 2d where two different carrier scattering mechanisms are related to the carrier density-dependent charge transport in IAZO. The carrier mobility increases with carrier density at the carrier density regime below ~10^{20} /cm^3. At a carrier density of approximately 4×10^{18} /cm^3, the carrier mobility is ~29.6 cm^2/Vs and increases up to 49.7 cm^2/Vs at a carrier density of ~1.5×10^{20} /cm^3. However, the trend is reversed when the carrier density of IAZO further increases. Lower mobility of ~34.7 cm^2/Vs is measured at the maximum carrier density, obtained from this study, of ~2.6×10^{20} /cm^3. The overall relationship between carrier mobility and carrier density shown in IAZO is in good agreement with our previous reports and those available in the literature on IAZO and other In_2O_3-based AOSs such as InGaZnO and InZnO[20, 32, 33]. The charge carrier transport in In_2O_3-based AOSs is governed

by two competing mechanisms of charge screening and ionized impurity scattering, of which the dominance of the two mechanisms is determined by the carrier density. At a lower carrier density regime (<~10^{20} /cm^3), the charge screening mechanisms dominates the carrier transport that is facilitated by screening charged dopant counterparts (i.e., oxygen vacancies) that may work as scattering sites. Therefore, the carrier mobility increases with increasing carrier density until a carrier density of ~10^{20} /cm^3 is reached. However, a further increase in carrier density, which also implies an increase in the density of charged oxygen vacancies, diminishes the effect of charge screening, and increases scattering events between free carriers and charged dopant counterparts (as ionized impurities). Since the carrier mobility is correlated with the carrier density rather than the annealing temperature effect, the carrier density was selected to identify the activation energy for the carrier generation/annihilation and its related conduction. An Arrhenius plot of log (carrier density) vs inverse temperature in Kelvin is shown in Figure 2e, where the activation energy (E_a) for the carrier density is found to be approximately 0.06 eV at annealing temperatures below 200 °C and 0.43 eV above 200 °C. It should be noted that the different activation energy indicates that two different mechanisms for carrier generation/annihilation are involved in the carrier density trend. The higher E_a of 0.43 eV is likely related to the oxygen vacancy-based mechanism as similarly observed in other In_2O_3-based AOSs[32, 34]. The low activation energy is likely associated with the shallow level states located near the conduction band, to which charge carriers in the conduction band are trapped during low temperature annealing (<~200 °C)[35].

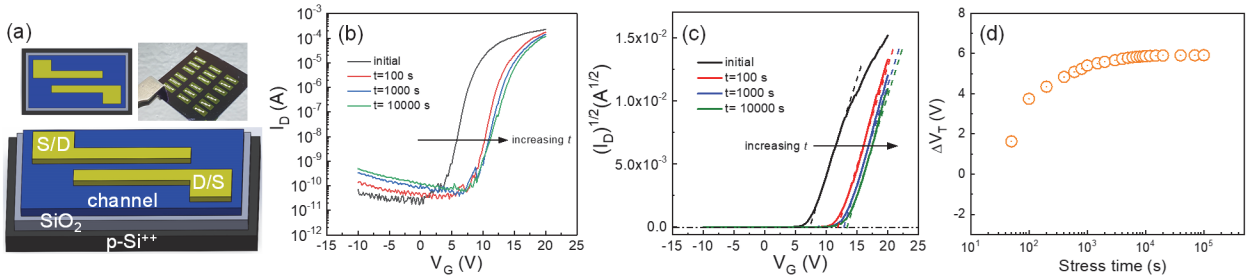

Figure 3. **PBS investigations for IAZO TFTs at a gate bias of 30 V as a function of stress time (*t*).** (a) schematic of bottom-gated TFTs with top and tilted views, and a photograph of IAZO TFTs, (b) TFT I_D-V_G transfer characteristics, (c) $(I_D)^{1/2}$-V_G curves, which show positive shifts of the transfer curves and V_T, and (d) a change in V_T (ΔV_T) with stress time that shows a relatively large change within 100 s PBS, and then the rate of change is saturated to a ΔV_T of approximately 6 V.

Bottom-gated TFT devices were fabricated based upon the knowledge, described above, of the structure, optoelectronic and electrical properties. In order to achieve a low enough carrier density for the channel, oxygen was added to the sputter gas at the O_2/Ar volume ratio of 20/80. A schematic and a photograph of fabricated TFT devices are displayed in Figure 3(a) where the channel IAZO thickness of 20 nm, the channel width and length ratio of W/L=2000 μm/100 μm, and the Al metallization thickness of 100 nm were used. Saturation regime transfer characteristics were investigated by scanning the gate bias at a fixed drain bias of V_D=20 V, where the devices were well into the saturation regime of drain current[21]. In Figure 3(b), initial as-deposited IAZO TFTs exhibit the device drain current on/off ratio of greater than 10^7. The field effect mobility (μ_{FE}) and the threshold voltage are determined from the slope and the x-axis intercept of the linear extrapolation of the $(I_D)^{1/2}$-V_G plots in Figure 3(c). For as-fabricated TFTs (without bias stress applied), the saturation field effect mobility is 7.64 cm^2/Vs and the threshold voltage is found to be approximately 7.49 V.

To investigate the bias stability of IAZO TFTs, the transfer characteristics were measured from as-deposited devices as a function of bias stress time at a negative gate bias of -30 V and a positive

gate bias of 30 V. During the negative bias stress (NBS) tests, no significant changes were observed in transfer characteristics, which is attributed to the depletion of free carriers in the channel due to the application of the negative bias, regardless of stress time[36]. The field effect mobility and threshold voltage extracted from the NBS transfer characteristics shows only minimal variations by ±0.41 cm2/Vs and ±0.33 V, respectively. However, clear positive shifts of the TFT transfer characteristics are detected during the positive bias stress (PBS) measurements as shown in Figure 3(b, c). The ΔV_T trend over time is summarized in Figure 3(d). The positive shift can be explained by trapped electrons during the PBS measurements at the channel and dielectric interface[25, 36, 37], which is supported by the estimated trap density (Q_i) at the channel/dielectric interface with the sub-threshold slope (*S.S*) values using equations:

$$Q_i = \left(\frac{q(S.S)log(e)}{kT} - 1\right)\frac{C_{ox}}{q} \qquad (1)$$

and

$$S.S = \frac{dV_G}{d(logI_D)} \qquad (2)$$

The S.S and trap density increase with increasing PBS stress time as shown in **Table 1** below. A relatively large V_T shift was made within 100 s during the PBS tests, and the rate of V_T shift becomes slow and saturated to ΔV_T of approximately 6 V, as shown in Figure 3(d). The carrier accumulation in the channel due to the positive gate bias (more specifically, the effective region of the active layer near the channel/dielectric interface) is saturated, particularly for the thin channel (~20 nm), and therefore the density of trapped electrons is limited as well. It should be noted that the carrier mobility increases from the initial 7.64 cm^2/Vs to 10.17 cm^2/Vs after 100 s of PBS (Table 1), and then the increase in carrier mobility becomes insignificant with increasing

stress time, compared to that of the increase within 100 s. The initial increase in carrier mobility is attributed to the injection of free carriers into the channel due to the applied positive gate bias since higher carrier density of IAZO, like other In_2O_3-based AOS materials, leads to a greater carrier mobility[32, 38] in the regime of carrier density below approximately 10^{20} /cm^3 as shown in Figure 2(d). In addition, this carrier mobility trend, showing a significant increase within 100 s of PBS then saturated after 100 s, agrees well with the discussion above regarding limited carrier injection with stress time. The off-state drain current behavior, increasing with stress time, is also attributed to the carrier injection to the channel due to the application of positive bias during the PBS investigations. The overall performance parameters of the IAZO TFTs experienced with PBS are summarized in Table 1 below.

Table 1. Properties of amorphous IAZO TFTs during PBS tests.

PBS time [s]	μ_{sat} [cm^2/Vs]	S.S [V/decade]	V_T [V]	Q_i [/cm^2]
Initial – 0 s	7.64	0.73	7.49	4.88 x 10^{12}
100 s	10.17	0.87	11.88	6.34 x 10^{12}
1000 s	10.87	0.99	12.75	7.21 x 10^{12}
10000 s	11.74	1.19	13.30	8.49 x 10^{12}

4. Conclusions

A third cation AOS of InAlZnO, which exhibits enhanced amorphous phase stability and higher carrier mobility, was integrated into TFT devices as a channel. The saturation field effect mobility of IAZO-based TFTs shows as high as 7.64 cm^2/Vs in its annealed state, which is much higher than those of other un-annealed AOS TFTs. Although negative gate bias stress does not affect the threshold voltage of IAZO TFTs, positive gate bias stress leads to threshold voltage shifts towards

the higher bias direction. The trap density calculation suggests that the observed V_T shift is attributed to the increased charge trap density at the channel/dielectric interface. In addition, the V_T shift is prominent for the first 100 s and then no significant changes are observed in the remaining time-dependent analysis, up to 10^5 s, which is possibly related to the saturation of trap density at the channel/metallization interface within the first 100 s. The bias stress analysis and the findings of gate bias-induced trap-related V_T shifts are of importance to understand and enhance the performance stability of IAZO other AOS TFTs.

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Notes

The authors declare that they have no conflict of interest.

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