ScienceAdvances
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FRONT MATTER

Title

- **Full title:** Layer-resolved release of epitaxial layers in III-V heterostructure via a buffer-free mechanical separation technique
- **Short title:** Buffer-free mechanical release of III-V epi-layers

Authors

Honghwi Park,[1]† Heungsup Won,[1]† Changhee Lim,[1,6] Yuxuan Zhang,[3] Won Seok Han,[4] Sung-Bum Bae,[4] Chang-Ju Lee,[1] Yeho Noh,[1] Junyeong Lee,[1] Jonghyung Lee,[1] Sunghwan Jung,[5] Muhan Choi,[1,2] Sunghwan Lee,[3] and Hongsik Park[1,2]*

Affiliations

[1]School of Electronic and Electrical Engineering, Kyungpook National University, Daegu 41566, South Korea
[2]School of Electronics Engineering, Kyungpook National University, Daegu 41566, South Korea
[3]School of Engineering Technology, Purdue University, West Lafayette, IN 47907, USA
[4]Electronics and Telecommunications Research Institute, Daejeon 34129, South Korea
[5]Department of Mechanical Engineering, Dankook University, Yongin-si, Gyenggi-do 16890, South Korea
[6]Applied Materials Korea, Ltd., Cheongju-si, Chungcheongbuk-do 28378, South Korea

†These authors contributed equally to this work.
*Correspondence to H.P. (email: hpark@ee.knu.ac.kr).

Abstract

Layer-release techniques for producing freestanding III-V epitaxial layers have been actively developed for heterointegration of single-crystalline compound semiconductors with Si platforms. However, for the release of target epitaxial layers from III-V heterostructures, it is required to embed a mechanically- or chemically-weak sacrificial buffer beneath the target layers. This requirement severely limits the scope of processable materials and their epi-structures and makes the growth and layer-release process complicated. Here, we report that epitaxial layers in commonly used III-V heterostructures can be precisely released with an atomic-scale surface flatness via a buffer-free separation technique. This result, for the first time, shows that heteroepitaxial interfaces of a normal lattice-matched III-V heterostructure can be mechanically separated without a sacrificial buffer and the target interface for separation can be selectively determined by adjusting process conditions. This technique of selective release of epitaxial layers in III-V heterostructures will provide high fabrication flexibility in compound semiconductor technology.

Teaser

We show that epitaxial layers of III-V compound semiconductor heterostructures can be selectively released at target interfaces.

MAIN TEXT

Introduction

Heterogeneous integration of materials is one of the important processing technologies for emerging electronic and optoelectronic applications such as monolithic 3D-integrated circuit chips and high-performance flexible devices based on single-crystalline inorganic semiconductors. The co-integration of heterogeneous materials with dissimilar electrical and optical properties enables novel technologies with a broad spectrum of functionalities beyond the limitations of a single-material nature. In particular, the co-integration of compound semiconductor devices and Si-based integrated circuits (ICs) can offer an effective pathway for overcoming Si's poor light-emitting properties and ultimately realizing the monolithic integration of photonic circuits with complementary metal-oxide-semiconductor (CMOS) ICs on a single chip (*1*–*3*). The simplest approach to such co-integration is to directly grow epitaxial layers of compound semiconductors on desired regions of a Si substrate. The compound semiconductors required for the co-integration with Si are typically GaAs- or InP-based III-V alloys such as InGaAs and InGaAsP, which are used for the fabrication of light sources and photodetectors in Si photonics (*4*). However, it is extremely difficult to epitaxially grow high-quality heterostructures composed of these compound semiconductors on a Si substrate because of a large lattice and thermal expansion coefficient (TEC) mismatch with Si(100) (*5*, *6*). For instance, the lattice/TEC mismatch of GaAs and InP with Si is approximately 3.9/128.1% and 8.0/73.1%, respectively, which induces a large density of dislocations and excessive strain upon the heterostructures (*6*, *7*).

As an approach without direct heteroepitaxy, layer release/transfer techniques for separating a thin layer of single-crystalline compound semiconductors and subsequently bonding it to arbitrary substrates have been actively developed at the industrial scale because this approach can enable a versatile combination of various semiconductors for heterointegration without the limitations of lattice and TEC mismatch. One of the commonly used processes is epitaxial lift-off (ELO) and its variant techniques. The most typically used ELO process is a chemical lift-off technique. For this process, a chemically weak layer is first grown as a sacrificial buffer during a heterostructure epitaxy step and the weak layer is then selectively etched away for the release of the epitaxial layers on top of the buffer (*8*–*10*). Although this process has been widely used to fabricate thin, flexible, and 3D-integrated structures, it can be applied only to epitaxial heterostructures with extremely high etching selectivity between the sacrificial buffer and other layers and has limitations in high-throughput wafer-scale processes because of the slow lateral etching rate of the sacrificial buffer. Another type of the ELO process is a mechanical lift-off technique. For this process, a mechanically-weak defective or porous sacrificial buffer is first formed within a heterostructure and the sacrificial buffer is then physically broken for the layer release (*11*, *12*). This is much faster process than the chemical lift-off technique. However, the formation of the mechanically-weak buffer in the heterostructure makes the growth process very complicated and limits the crystal quality of single-crystalline epitaxial layers grown on the buffer. In addition, this process is also allowed only for the limited scope of III-V materials and epitaxial structures. Recently, a graphene-assisted layer release/transfer technique has been suggested (*13*–*15*). This technique is based on remote epitaxy allowing the growth of single-crystalline compound semiconductor layers on a graphene buffer, which thereby enables facile layer release from the graphene surface due to its weak van der Waals bonding. Although this technique has been widely applied for the co-integration of various heterogeneous materials, for industrial adoption, it is still necessary to improve the processes for the growth and transfer of large-scale defect-free graphene layers because the process yield depends on the quality of transferred one- or few-monolayer graphene (*15*).

As an alternative approach without using a sacrificial buffer, a mechanical separation technique called thickness-controlled spalling has been actively studied because it enables the fast and kerf-less release of wafer-scale semiconductor layers through a relatively simple and low-temperature process (*16–31*). In this process, a thin single-crystalline semiconductor layer is mechanically released by the stress induced from a stressor film (typically, Ni) deposited on the substrate. Since the spalling process of semiconductors relies on the mechanical separation of crystal planes in the single-crystalline substrates, a thin-layer release is possible without a sacrificial buffer. Moreover, the thickness of the released layer can be controlled from hundreds of nanometers to tens of micrometers by adjusting the thickness and stress of the Ni film. Based on these advantages, the thickness-controlled spalling technique has been applied to a wide range of materials from elemental semiconductors (*16–23*, *29–31*) to compound semiconductors (*20*, *24–28*). In particular, this technique has been effectively used in device fabrication with a thin layer of elemental semiconductors (Si and Ge). For instance, flexible logic and memory ICs based on sub-30 nm CMOS technology (*16–19*), wearable/stretchable sensors (*29*, *30*), and thin-film photovoltaic cells (*20–23*) for flexible applications have been demonstrated using Si or Ge spalling processes. In practice, the greater potential of this buffer-free mechanical separation technique is derived from the layer release of compound semiconductors which enables the versatile heterointegration of III-Vs and Si. However, it is known that this technique has a critical issue for applying to III-V semiconductors. In contrast to elemental semiconductors, the spalling process for zinc-blende (100) compound semiconductors such as GaAs- or InP-based III-Vs leaves zig-zag corrugations on the surface of the released III-V layers and substrates because of the undulating crack propagation along the {110} planes (*20*, *24–27*). It has been reported that the height and pitch of the corrugations can be as large as several to tens of micrometers (*20*, *26*). This is a significant problem that limits practical applications of this buffer-free mechanical separation technique to co-integration of III-V and Si devices because the non-flat surface impedes the subsequent transfer of the released layer and the continuous reuse of the substrate.

In this study, we propose a layer-resolved mechanical separation technique that can precisely release target III-V epitaxial layers from a single-crystalline heterostructure without a sacrificial buffer. This technique is based on mechanical exfoliation at the epitaxial interface of a heterostructure and allows the release of single-crystalline III-V layers with an atomically flat surface. To demonstrate this technique, we epitaxially grow a lattice-matched heterostructure with multiple InP/InGaAs junctions on an InP(100) wafer and show that the epitaxial layers can be released at a specific junction of the heterostructure. Furthermore, we demonstrate that the target junction for separation can be selectively determined by controlling the strain energy induced by the Ni stressor film. Structural characterizations based on energy-dispersive x-ray spectroscopy (EDS), Raman spectroscopy, and atomic force microscopy (AFM) measurements prove that layer release occurs precisely at junctions between the InGaAs and InP epitaxial layers and the surface of the released layers is atomically flat. Additionally, we confirm the effect of the proposed layer-release process on crystal and material quality by measuring high-resolution x-ray diffraction (XRD) and photoluminescence (PL) characteristics after the transfer of the released InP/InGaAs epitaxial layers onto a Si substrate.

Results

Layer release of III-V compound semiconductors

Thickness-controlled spalling technique and its mechanism for layer release of single-crystalline semiconductors is summarized in the Supplementary Materials (fig. S1 and note S1). As reported in the literature, it can be observed that the spalling process for zinc-blende III-V(100) compound semiconductors such as GaAs(100) and InP(100) leaves zig-zag corrugations on the surface of the released layers, unlike the spalling process for elemental semiconductors. The origin of the formation of the corrugations in III-V(100) spalling could be explained by undulating crack propagation along the {110} planes (*24*, *26*, *27*), as shown in Fig. 1A. In the spalling of (100) semiconductors, the (100) plane is oriented parallel with the "local symmetry plane" where the mode-II stress intensity factor (K_{II}, in-plane shear mode) is zero (*i.e.*, $K_{II} = 0$). However, in the case of III-V(100), the crack is inclined to deviate from the local symmetry plane to grow on the (110) plane because the surface energy of the (100) plane is considerably higher than that of the (110) cleavage plane (*32*, *33*). As the crack grows off from the local symmetry plane, the magnitude of K_{II} grows from 0 and K_{II} at the crack tip evolves to act in a way of stabilizing the crack path (*i.e.*, inducing the crack to grow back toward the local symmetry plane with a decrease of its magnitude). When K_{II} decreases back to 0, the crack deviates from the local symmetry plane again to grow on the $(\bar{1}10)$ plane. Such directional change of the crack is repeated alternatively with respect to the local symmetry (100) plane. Thus, after successive directional changes of the crack, the periodic zig-zag corrugation is formed at the released surface. To investigate the surface structure of the released III-V(100) layers, we fabricated thin GaAs and InP layers with various layer thicknesses. First, as expected from the suggested theory, there was correlation between the peak-to-peak height and pitch of the zig-zag corrugations on the released layers. Half of the zig-zag pitch was directly proportional to the zig-zag height over the entire released region, as shown in Fig. 1B; this indicates that the facet of the corrugation is composed of {110} cleavage planes. This result supports the idea that the corrugations originate from the surface-energy contrast between the (100) and (110) crystal planes. Second, we observed that the height of the zig-zag corrugations was dependent on the released-layer thickness. In our study, the zig-zag height was approximately 1.2 times larger than the released-layer thickness in its range from 2 to 13 μm (Fig. 1C). This result suggests one simple approach to minimizing zig-zag corrugations; that is releasing the III-V(100) layer as thin as possible. However, the practical problem is that the minimum spalling depth (released-layer thickness) guaranteeing the reliability of this process is typically limited to 1–2 μm (*19*, *31*). When the Ni film is too thin, it is difficult to initiate a crack. Additionally, the local non-uniformity of the film stress and undesirable external force can cause non-uniform crack propagation. Thus, it may be difficult to remove the surface corrugation by engineering the process conditions and this issue limits practical applications of the spalling process because of difficulty with the transfer of the released III-V layers and the continuous reuse of substrates (fig. S2 and note S2).

Layer-resolved mechanical separation technique for III-V heterostructures

As an alternative approach, based on the results and mechanism of the III-V(100) spalling, we designed a layer-resolved mechanical separation process for III-V heterostructures. The zig-zag corrugations originate from the fact that the surface energy of the local symmetry (100) plane is significantly higher than that of another crystal plane, *i.e.*, the (110) plane. This means that the spalling of III-V compound semiconductor layers with a flat surface and a uniform thickness may become possible if we can find a condition in which the surface energy of the local symmetry plane is less than that of the (110) plane. To achieve this condition, our approach is to match the location of the local symmetry plane (*i.e.*, spalling depth) to a covalent-bonded epitaxial interface in a III-V heterostructure composed of multiple epitaxial layers. The reason is that the surface energy (*i.e.*, crystal binding energy) of an epitaxial interface in III-V heterostructures can be reduced by the misfit-induced strain energy. In cases of lattice-mismatched heterostructures, a strong misfit strain

is induced between the heteroepitaxial layers, and further, localized dislocations and defects are often introduced into the crystals near the epitaxial interface (*5–7*, *15*). Even in lattice-matched heterostructures, it is known that an abruptly inverted heteroepitaxial interface contains at least one or few monolayers of undesirable lattice-mismatched III-V alloy, which is induced by phase intermixing due to interdiffusion of atoms or memory effects of precursors (*34–41*). For instance, compressive-strained InAs and InAsP or tensile-strained InGaP layers are formed at the heteroepitaxial interface of the lattice-matched InP/$In_{0.53}Ga_{0.47}As$ heterostructure (*38–41*). Thus, as the localized misfit strain energy is introduced at the epitaxial interface, the surface energy of the (100) plane aligned with the strained interface layers can be reduced to less than that of the (110) plane, and thereby, the (100) interface plane becomes preferable to the (110) plane for the layer release in spalling processes. The reduction of crystal binding energy at a heteroepitaxial interface of lattice-matched heterostructures can also be predicted from a simple binding-energy calculation based on density functional theory (see fig. S3 and note S3 for calculation results of the representative lattice-matched III-V heterostructures, InP/InGaAs and GaAs/InGaP).

Since III-V semiconductors are typically grown as an epitaxial heterostructure rather than as a bulk for device applications, if this process is viable, it would enable a versatile III-V spalling technique capable of selectively releasing single-crystalline III-V layers of interest from a heterostructure. The concept of this process is illustrated in Fig. 1D. Crack propagation is not straight when the local symmetry plane is located in the bulk substrate; however, if the location of the local symmetry plane is matched to one of the heterointerfaces (*i.e.*, junctions between heteroepitaxial layers) which are covalently bonded, layer release can occur at a specific junction via a straight crack propagation along the relatively weak local symmetry plane. Furthermore, the target interface to be separated in the multiple epitaxial layers can be selectively determined by controlling the strain energy from the stressor film.

To demonstrate the proposed layer-resolved mechanical separation technique, we first grew a III-V heterostructure composed of lattice-matched multiple InP/$In_{0.53}Ga_{0.47}As$ epitaxial layers on an InP(100) wafer using a metal-organic chemical-vapor-deposition (MOCVD) system. This structure is one of the commonly-used heterostructures for fabricating a near-infrared (NIR)-sensitive *p–i–n* photodiode (*42*, *43*). The epitaxial-layer structure is shown in Fig. 2A. To verify the layer-selection capability of the proposed technique, we designed process conditions to set the local symmetry plane at three different locations in the heterostructure. The first process condition corresponds to that in which layer release occurs in the bulk substrate (process I). The other process conditions are designed to match the location of the local symmetry plane to one of the interfaces between the heteroepitaxial layers (process II and III). The locations of the local symmetry planes in process I, II, III are denoted in Fig. 2A. In process II, the local symmetry plane is set to the junction between the n-InGaAs and n-InP layers. In process III, the local symmetry plane is set to another junction, the epitaxial interface between the n-InP and i-InGaAs layers. To establish detailed experimental conditions for the three layer-release processes, it is essential to estimate the correlation between the spalling depth and the strain energy determined by the thickness and stress of the Ni stressor film. Thus, we first measured the internal stress of the Ni film with varying Ni thicknesses using a multi-beam optical-sensor system (*44*) and calculated the strain energy accumulated in the substrate as a function of the Ni thickness (Fig. 2B). This result shows that the strain energy can be controlled by adjusting the Ni thickness. Then, the estimated spalling depth was calculated as a function of the Ni thickness using an analytical model based on delamination theory (*31*, *45–47*). In this model, the spalling depth is determined from the thermodynamic equilibrium condition in which the total strain energy accumulated in the Ni film and the released layer is balanced with the crystal binding energy of a (100) plane (see fig. S4 and note S4 for details of the analytical model and calculation procedure).

The calculated spalling depth is shown by the solid line in the plot of Fig. 2C. From this analytical calculation, we estimated the Ni thickness for process II and III to be ~3.5 and 3 μm to match the

spalling depth to two different junction depths. For process I, we set a thicker Ni thickness (7 μm) to guarantee that the layer release occurs in the InP bulk. Based on these estimates, we released the III-V epitaxial layers using the Ni stressor films with various Ni thicknesses and found out that release of the layers with a flat and uniform surface at specific junctions was possible when the Ni thickness was 3.2 μm for process II and 2.8 μm for process III. When we deposited 7-μm-thick Ni, the spalling occurred in the bulk with a released-layer thickness of 28 μm, as expected. The released-layer thicknesses (spalling depths) in process I, II, and III are shown by the dots in Fig. 2C. The empirical results showed good agreement with the estimates by the analytic model. The cross-sectional scanning electron microscopy (SEM) images of the released layers and the remaining substrate after the three processes are shown in Fig. 2D. (The SEM images obtained with different magnifications are shown in fig. S5). Process I with thick Ni film left zig-zag corrugation on the surface of the released layer and the substrate because the layer release occurred in the bulk. On the other hand, the SEM images show that the surfaces of the released layers after process II and III were flat and the images indicate that the layer release was occurred respectively at the target InP/InGaAs junctions because the thicknesses of the epitaxial layers in the released layers and remaining structures were the same as the junction depths of the heterostructure. In the SEM images, the color and brightness of the relatively thin epitaxial layers have been adjusted to make them more visible (see fig. S6 for the original SEM images). From the surface images taken after the spalling, we could also estimate the yield of the layer release at the heteroepitaxial interface. The estimated yield was about 78% (see fig. S7 and note S5 for details of the yield estimation). In addition, we could evaluate the thickness uniformity by measuring the released surface morphology after process II and III over the entire region of the spalled sample (sample size of 15 × 15 mm^2). The results indicate that both process II and III enabled uniform layer release at the target heteroepitaxial interfaces (*i.e.*, local symmetry planes we designed) in the large area of the sample (> 12 × 12 mm^2) except for the sample edge regions (fig. S8 and S9).

Characterizations of the layer-resolved mechanical separation technique

We investigated the elemental compositions and structural information of the layers to confirm that layer release occurred at the target junctions between the InGaAs and InP epitaxial layers (Fig. 3). Cross-sectional SEM images and EDS elemental-mapping images (P, In, Ga, As) of the released epitaxial layers and the remaining substrates are shown in Fig. 3A and 3B for process II and III, respectively. Since process II was designed to separate the interface between n-InP and n-InGaAs, the released structure was composed of three epitaxial layers (InP/InGaAs/InP), as could be observed from the SEM image. The elemental-mapping image of the released layer is clearly divided into three different regions. As shown in Fig. 3A, the Ga and As composition signals are depleted in the top and bottom regions and the P signal is depleted in the middle region of the released layer while the P composition signal is depleted in the thin top region of the remaining substrate. In the case of process III, the released layer is composed of two epitaxial layers (InP/InGaAs) and the remaining substrate has two epitaxial layers on the InP bulk. This compositional structure can be also confirmed by elemental-mapping images for process III (Fig. 3B). The P signal is depleted in the bottom region of the released layer while the Ga and As signals are depleted in the top of the remaining substrate. For more rigorous confirmation, we analyzed the III-V structure of the released layers and the remaining substrates by measuring Raman spectroscopy on their surfaces after layer release by process II and III. Fig. 3C shows the Raman spectra for process II. The two primary peaks of the Raman spectrum measured on the surface of the released layer correspond to the InP-like longitudinal optical (LO) mode and transverse optical (TO) mode (*48*). The main peaks observed on the surface of the remaining substrate correspond to the InAs-like LO mode and the GaAs-like LO mode (*49*, *50*). On the other hand, the Raman spectra for process III indicate that the main peaks on the released layer correspond to the InAs-like LO mode and the GaAs-like LO mode and those on the substrate correspond to the InP-like LO and TO

modes (Fig. 3D). These results clearly confirm that spalling process II released the InP/InGaAs/InP epitaxial layer and process III released the InP/InGaAs epitaxial layer. The important aspect of these results is that the proposed process can enable a III-V spalling technique that can selectively release single-crystalline epitaxial layers of interest from a III-V heterostructure wafer by controlling the strain energy induced by the Ni film. Additionally, to confirm the presence of an intermixing layer which plays a dominant role in enabling the flat and uniform layer release at the target epitaxial interfaces, we performed transmission electron microscopy (TEM) and additional Raman analysis on the interface between InP and InGaAs layers. High-resolution TEM images and the additional Raman investigation showed the lattice-matched InP/InGaAs heterostructure contains an intermixing layer with a two- or three-monolayer thickness at the epitaxial interface between InP and InGaAs layers (fig. S10).

To confirm whether the proposed layer-release technique can be applied to practical applications, we transferred the released layer onto a Si(100) substrate and investigated the crystal and material qualities of the transferred epitaxial layers (Fig. 4). The transfer process was performed by a spin-on-glass process with a tetraethyl orthosilicate (TEOS)-based SiO_x-bonding layer (*51*, *52*). Because the surface of the layer released by the proposed technique was flat, we could reliably transfer the epitaxial layer (InP/InGaAs) onto the Si substrate without any air voids at the interface between the epitaxial layer and bonding layer (Fig. 4A). We characterized the surface morphology of the released layers by using AFM measurement. As shown in Fig. 4B, the surface of the released layer was atomically flat with a root-mean-squared surface roughness of ~3.7 Å. This flatness is comparable with the spalling result of elemental semiconductors (*31*). Fig. 4C shows the characterization on the crystallinity of the transferred epitaxial layer based on the high-resolution XRD measurement. The slight shift in XRD peaks towards higher diffraction angles (~0.005°) indicates that there was a weak remaining compressive stress after the transfer, and the full-width at half-maximum values less than 0.01° (< 40 arcsec) of the XRD peaks corresponding to the (004) lattice of transferred InGaAs and InP indicate that there was no noticeable degradation in crystal quality of the single-crystalline epitaxial layer after the processes. In addition, we confirmed the material quality of the transferred epitaxial layer by measuring the steady-state PL characteristics at room temperature. There was no noticeable difference between the spectrum of the epitaxial layer as-grown on InP and that of the released/transferred layer (Fig. 4D). No peak shift induced by the optical-bandgap change nor peaks activated by defects were observed after the processes. Consequently, these structural and optical characterization results indicate that the proposed layer-resolved mechanical separation process enables atomically flat release and transfer of a III-V(100) epitaxial layer without noticeable degradation in both crystal and material quality.

Discussion

In summary, we proposed a layer-resolved mechanical separation technique that can selectively release III-V(100) epitaxial layers of interest from a normal lattice-matched heterostructure without an embedded sacrificial buffer. Because the layer release precisely occurs at a heteroepitaxial interface with a relatively weak surface energy, this technique can enable atomically flat and uniform release of single-crystalline III-V epitaxial layers without degradation in crystal and material quality. Furthermore, we demonstrated that the target heteroepitaxial interface for layer release can be selectively determined by controlling the strain energy induced by the Ni stressor film. This technique will offer an effective processing technique required for heterogeneous integration of III-V compound semiconductors with Si or other substrates and provide high fabrication flexibility in compound semiconductor technology.

Materials and Methods

Epitaxial growth

The InP/InGaAs heterostructure was epitaxially grown on a 2-inch on-axis n-InP(100) wafer by a MOCVD reactor (D180 LDM, Veeco Inc.). After growing a 0.3-μm-thick buffer layer (Si-doped n-InP) on the InP substrate, a lattice-matched 0.2-μm-thick n-$In_{0.53}Ga_{0.47}As$ layer (Si-doped with a doping concentration of 5×10^{16} cm^{-3}) was grown as an etch-stop layer for n-type contact formation. For a *p–i–n* structure, a 1-μm-thick n-type contact layer (Si doped InP), 2.8-μm-thick active layer (undoped $In_{0.53}Ga_{0.47}As$), and 0.5-μm-thick p-type contact layer (Zn doped InP) were sequentially grown. The doping concentrations of the n-InP and p-InP contact layers were 3×10^{18} and 5×10^{17} cm^{-3}, respectively. In this growth process, the InP/InGaAs epitaxial layers were grown at 650 °C under N_2 ambience, and phosphine, trimethylindium, trimethylgallium, and arsine were used as P, In, Ga, and As precursors, respectively.

Mechanical release of thin semiconductor layers

The Si, GaAs, InP, and InP/InGaAs heteroepitaxial layers were mechanically released by the Ni stressor film with a handling layer. Prior to the deposition of the Ni film, a 20-nm-thick Ti film was deposited by DC magnetron sputtering with a system power of 600 W and a working pressure of 3 mT to promote adhesion between the Ni film and substrate. Subsequently, in the same chamber, a Ni film with a high internal tensile stress was deposited with a system power of 300 W and a working pressure of 3 mT. After unloading the Ni-deposited samples and cooling them to room temperature, the semiconductor layers were released from their substrates by using a thermal-release tape (Revalpha, Nitto Denko Inc.) as a handling layer for the layer release/transfer process. In this step, we attached the thermal-release tape on top of the Ni film and manually applied an external lifting force to the sample using the handling tape to initiate the crack at the sample edge. After the crack initiation, due to the high stress induced by the Ni film, the crack propagated almost spontaneously until the semiconductor layer was completely released from the substrate.

Transfer of released semiconductor layers

The released semiconductor layers were transferred onto a Si substrate by using the spin-on-glass process (*51*, *52*). First, TEOS-based solution-processable SiO_x was spin-coated on the Si substrate as a bonding layer; then, a released semiconductor layer was placed onto the SiO_x-coated Si substrate. Subsequently, to cure the SiO_x layer and bond the semiconductor layer with the Si substrate, we baked the sample at 120 °C for 2 hours with applying a pressure of 55 g/cm^2. In this step, the thermal release tape was detached from the surface of the sample due to the baking temperature being higher than the release temperature of the tape (90–120 °C). The thickness of the SiO_x layer was about 500 nm after the baking step. Finally, the stressor film was completely removed by wet etching. The Ni film was etched in a 0.1 M ferric chloride ($FeCl_3$) solution and the thin Ti layer was etched in a diluted (1%) hydrogen fluoride (HF) solution.

Stress measurement

The internal stress of the Ni film was measured with a multi-beam optical sensor system (*44*). In this measurement, the internal stress was estimated based on Stoney's method (*53*) which is a standard method for measuring film stress. The internal stress was deduced from the curvature change in the film/substrate which was estimated from the change in the measured spacing between multiple beams. The relation between the internal stress of the film and the measured beam spacing is given by:

$$\sigma_f = \left(\frac{\Delta d}{d_0}\right) \frac{Y_s t_s^2 cos\alpha}{12(1-v_s)t_f L}$$

where σ_f, Δd, d_0, Y_s, ν_s, t_s, t_f, α, and L are the internal stress of film, the difference in beam spacing due to stress-induced curvature, the initial beam spacing before film deposition, the Young's modulus of the substrate, the Poisson ratio of the substrate, the thickness of the substrate, the thickness of the film, the detection angle, and the detection length, respectively. To calculate the estimated spalling depth as a function of Ni thickness, we deposited Ni films with various thicknesses on InP(100) substrates and measured the internal stresses depending on their thicknesses.

Characterizations

The cross-sectional images of the released layers and the remaining substrates and the mapping images of their elemental compositions were obtained by using field-emission SEM (SU8220, Hitachi Inc.) combining with EDS (MX80, Oxford Instruments Inc.). The III-V structures on the surfaces of the released layers and the remaining substrates were evaluated via Raman spectroscopic measurement (inVia reflex, Renishaw Inc.) with a laser wavelength of 532 nm. The AFM image was obtained by the tapping-mode operation of a scanning probe microscope (NX20, Park Systems Inc.). An AC-mode Si probe with a resonance frequency of 300 kHz was used for imaging. The crystal quality of the epitaxial layers was characterized by an XRD measurement system (Empyrean, Malvern PANalytical Inc.) with Cu *Kα* radiation operated at 40 kV and 25 mA. The material quality was characterized by a PL measurement system (LabRAM HR-800, Horiba Jobin Yvon Inc.) with a 514-nm line laser and a Ge photodetector. The cross-sectional images of the heteroepitaxial interface between the InP and InGaAs layers were obtained by using field-emission TEM (Titan G2 ChemiSTEM Cs Probe, FEI Company Inc.).

References and Notes (references 54–64 appear only in the Supplementary Materials)

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Acknowledgments

Funding: This work was supported by the National Research Foundation of Korea (NRF) grant funded by the Korea government (MSIT) (2020R1A4A1019518), the NRF grant funded by the Korea government (MSIT) (2019R1A2C1088324), and the Bio & Medical Technology Development Program of the NRF funded by the Ministry of Science & ICT (2017M3A9G8083382). This work was also supported by Electronics and Telecommunications Research Institute (ETRI) grant funded by the Korean government (21ZB1100, Development of Creative Technology for ICT).

Author contributions: H.P. (Hongsik Park) conceived the idea and designed the experiments. H.P. (Honghwi Park), H.W., C.L. and Y.N. performed layer release and transfer processes for the Si, III-Vs, and InP/InGaAs heterostructures. W.S.H. and S.-B.B. performed epitaxial growth of the heterostructures. H.P. (Honghwi Park), H.W. and J.L. (Junyeong Lee) characterized all samples. H.P. (Hongsik Park), C.-J.L, J.L. (Jonghyung Lee), Y.Z., S.J., M.C. and S.L. participated in data analysis. H.P. (Hongsik Park), H.P. (Honghwi Park), H.W. and S.J. wrote the manuscript. All authors discussed and contributed to the discussion and analysis of the results regarding the manuscript at all stages.

Competing interests: The authors declare that they have no competing interests.

Data and materials availability: All data needed to evaluate the conclusions in the paper are available in the main text and/or the Supplementary Materials.

Figures (Fig. 1 to Fig. 4)

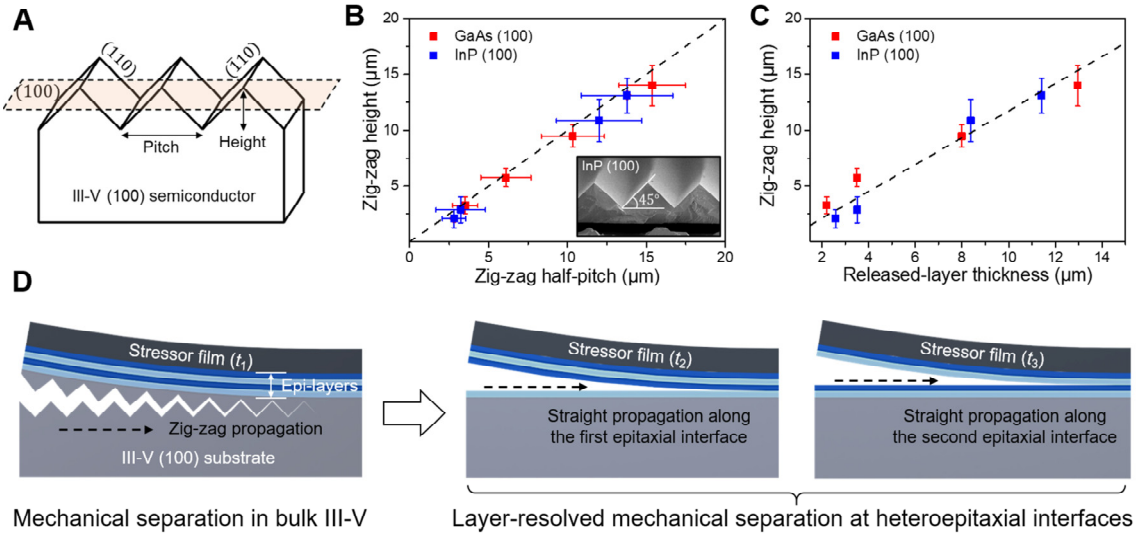

Fig. 1. Formation of zig-zag corrugations in a bulk III-V(100) and layer-resolved mechanical separation for III-V heterostructures. (**A**) Crystallographic planes of zig-zag corrugation formed in the spalling of a bulk III-V(100) semiconductor. The corrugation originates from undulating crack propagation along the {110} planes due to the surface-energy contrast between the (100) and (110) crystal planes. (**B**) Correlation between the height and half-pitch of the zig-zag corrugations on the released GaAs(100) and InP(100) layers, confirming that the facets of the corrugations is composed of {110} cleavage planes. (**C**) Peak-to-peak height of the zig-zag corrugations increases along with the thickness for both the released GaAs(100) and InP(100) layers. (**D**) A schematic of the proposed layer-resolved mechanical separation technique. By matching the location of the local symmetry plane (where $K_{II} = 0$) with a specific interface of an epitaxial heterostructure, a crack can propagate straightly along the junction between heteroepitaxial layers because of the relatively weak surface energy at the interface. The target junction for layer release in the heterostructure can be selectively determined by controlling the strain energy induced by the stressor film.

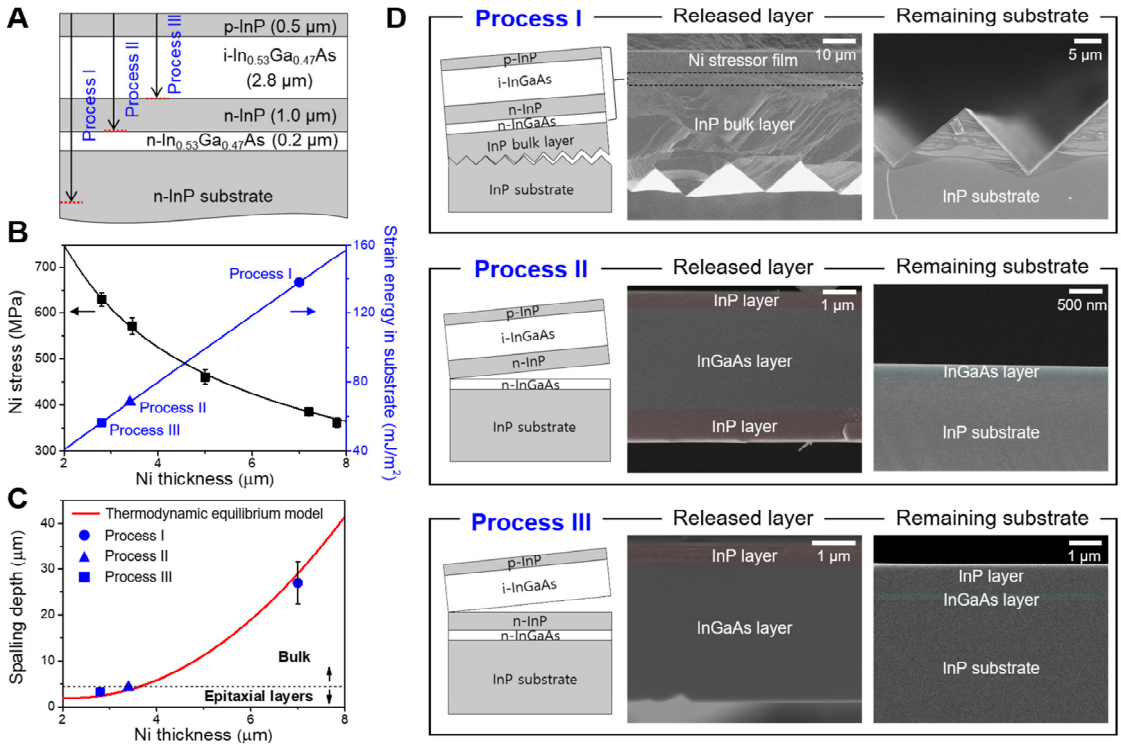

Fig. 2. Selection of target junctions for layer release in an InP/InGaAs heterostructure by controlling the strain energy induced by the Ni stressor film. (**A**) A schematic of the epitaxial heterostructure with multiple InP/InGaAs junctions used in this study. Process I, II, and III denoted in the schematic indicate layer-release processes with three different locations of local symmetry planes (dashed red lines). Process I corresponds to a process condition for layer release in the bulk substrate. Process II and III correspond to process conditions which are designed for the release of the epitaxial layers at different InP/InGaAs junctions. (**B**) Internal stress of the Ni film and the strain energy accumulated in the substrate as a function of the Ni thickness, showing that strain energy can be controlled by adjusting the Ni thickness and stress. (**C**) The estimated spalling depths of the layers as a function of the Ni thickness (red solid line) calculated from an analytical model based on the thermodynamic equilibrium condition between the stress-induced strain energy and the crystal binding energy. Dots in the plot indicate the empirical results for process I, II, and III, showing good agreement with the estimates obtained by the analytic model. (**D**) Cross-sectional SEM images of the released layers and the remaining substrates after process I, II, and III. These show that the epitaxial layers released at the InP/InGaAs junctions are flat and the target junction for layer release can be controlled by the strain energy induced by the Ni stressor film, whereas the surface of the layer released in the InP bulk exhibits the zig-zag corrugation.

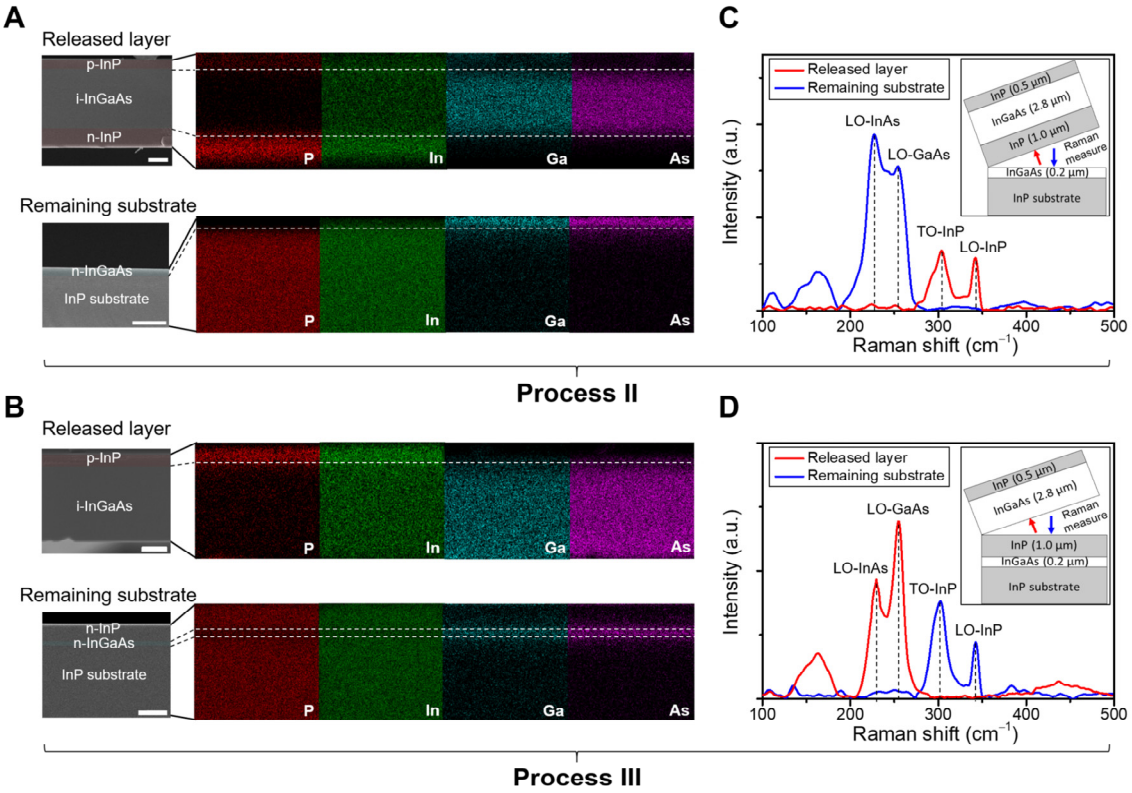

Fig. 3. Confirmation of layer-resolved release of epitaxial layers at different InP/InGaAs junctions. (**A**, **B**) Cross-sectional SEM images and EDS elemental-mapping images of the released layer and the remaining substrate after (A) process II and (B) process III. The scale bar is 1 μm. The spatial distributions of the P, In, Ga, and As signals of EDS agree well with the elements of each epitaxial layer. The dashed lines indicate the interfaces between the heteroepitaxial layers determined from the SEM images. (**C**, **D**) The Raman spectra measured from the surface of the released layer (red arrows in the insets) and the remaining substrate (blue arrows in the insets) after (C) process II and (D) process III. The spectra with the InP-like LO and TO mode peaks indicate InP surfaces and those with the InAs-like LO mode and GaAs-like LO mode peaks correspond to InGaAs surfaces. This result shows that the epitaxial layers are precisely released at the different target InP/InGaAs junctions of the heterostructure via process II and III.

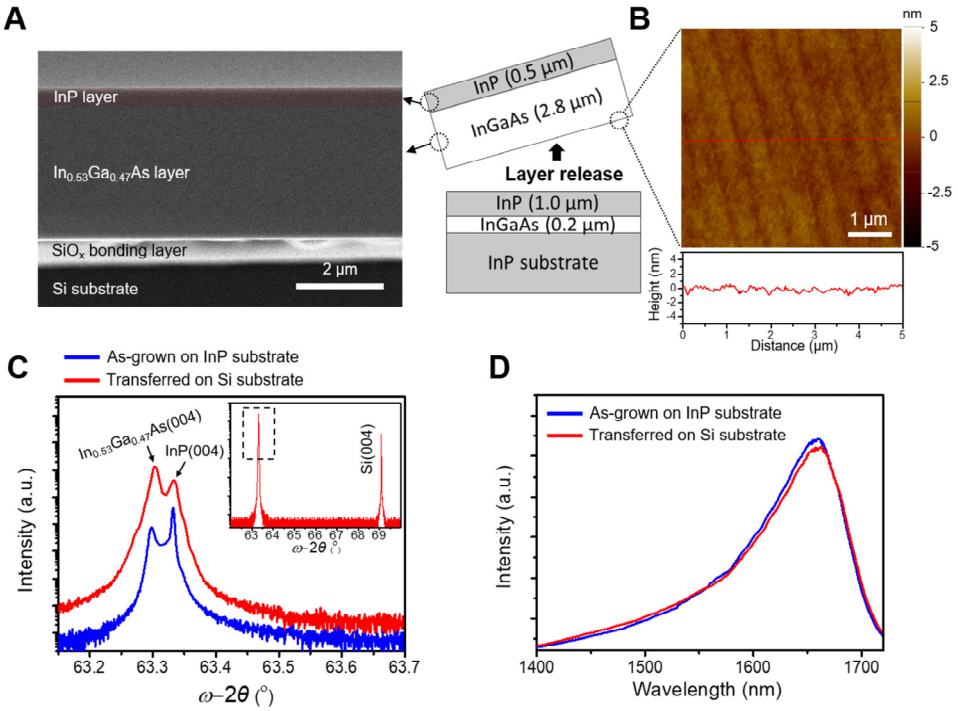

Fig. 4. Characterization of InP/InGaAs epitaxial layer transferred onto a Si substrate. (**A**) Cross-sectional SEM image of the transferred InP/InGaAs epitaxial layer on a Si(100) substrate after process III and (**B**) an AFM image of the surface of the released epitaxial layer (root-mean-squared surface roughness of 3.7 Å), showing that the surface of the released layer is atomically flat and the layer can be transferred without air voids. (**C**) High-resolution XRD ω–2θ scans of the InP/InGaAs epitaxial layer grown on the InP substrate and transferred onto the Si substrate, showing XRD peaks corresponding to the (004) lattice of InGaAs and InP (Inset, wide-range XRD ω–2θ scan including the Si lattice). (**D**) Steady-state room temperature PL spectra of the InP/InGaAs epitaxial layer grown on the InP substrate and transferred onto the Si substrate. These results indicate that the layer-resolved mechanical separation process enables atomically flat release and transfer of a III-V epitaxial layer without degradation in both crystal and material quality.

Supplementary Materials

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Supplementary Materials for

Layer-resolved release of epitaxial layers in III-V heterostructure via a buffer-free mechanical separation technique

Honghwi Park, Heungsup Won, Changhee Lim, Yuxuan Zhang, Won Seok Han, Sung-Bum Bae, Chang-Ju Lee, Yeho Noh, Junyeong Lee, Jonghyung Lee, Sunghwan Jung, Muhan Choi, Sunghwan Lee and Hongsik Park*

*Corresponding author. Email: hpark@ee.knu.ac.kr (H.P.)

This PDF file includes:

Supplementary Text

[Note S1] Controlled spalling technique for layer release of single-crystalline semiconductors

Fig. S1 shows the thickness-controlled spalling technique for layer release of single-crystalline elemental semiconductors (Si) and zinc-blende compound semiconductors (GaAs and InP). In this process, a thin semiconductor layer can be mechanically released by depositing a stressor film such as Ni which has a high tensile stress (*28*), as shown in Fig. S1A and S1B. The crack initiation and propagation for layer release are facilitated by the strong misfit stress induced in the Ni film and substrate. The crack trajectory and mechanism of the spalling process have been explained by a fracture model developed by Suo and Hutchinson (*54, 55*); this model defines two major stress intensity factors: K_I (mode I, opening mode) for the vertical direction and K_{II} (mode II, in-plane shear mode) for the lateral direction. First, the crack is initiated near the substrate edge by an external force and propagates to the inclined direction due to the mixed-mode stresses of K_I and K_{II}. Then, the crack seeks a specific depth at which $K_{II} = 0$ and propagates straight along the main crystal plane parallel to the film/substrate interface. In accordance with the Suo and Hutchinson model, a thin layer of Si(100) could be released with a flat surface and uniform layer thickness, as observed in the SEM images of Fig. S1A. Previous studies have shown that the spalling process enables layer release of Si and Ge with an atomically flat surface (root-mean-squared surface roughness < 5 Å) (*31*, *56*). However, it has been reported that the spalling of zinc-blende III-V(100) compound semiconductors such as GaAs and InP cannot offer a flat surface because cracks do not straightly propagate along the (100) crystal plane (*20*, *24–27*). Fig. S1C shows a schematic of the III-V(100) spalling process and cross-sectional SEM images of the released GaAs(100) layer and the remaining substrate. The thickness of the released layer is not uniform and periodic zig-zag corrugations are observed, unlike the result of Si spalling. To investigate the dependence of the thickness of the released layers upon Ni thickness, we released the Si(100) and III-V(100) layers using Ni films with varying thicknesses and measured the thickness of the released layers (*i.e.*, spalling depth) from cross-sectional SEM images of these layers. In the case of the III-V(100) layers, we estimated the spalling depth from the average thickness of the released layers because layer thickness was non-uniform because of zig-zag corrugations (Fig. S1C). Fig. S1D shows the thickness of the released Si(100), GaAs(100), and InP(100) layers as a function of the Ni thickness. The released-layer thickness was controlled in the range from 2 to 15 μm for Ni thicknesses from 2.5 to 6.5 μm. This result shows that the layer thickness can be controlled by adjusting the Ni thickness, and the non-linear relationship between the Ni thickness and the released-layer thickness agrees well with the previously reported empirical model for spalling depth (*31*).

In this result, the large thickness deviations observed in the relatively thick layers were possibly attributed to the locally non-uniform Ni thickness and film stress resulted from the harsh sputtering environment required for the thick Ni deposition because the local variation of Ni thickness and stress causes the variation of spalling depth where $K_{II} = 0$. This indicates that the thickness uniformity of the Ni stressor film is a critical factor for layer separation with uniform thickness from a semiconductor bulk. Thus, the development of a sputtering or electroplating process that guarantees the thickness and stress uniformity of thick Ni films is essential for reliable spalling process of bulk semiconductors.

[Note S2] Characterizations of GaAs(100) layer transferred onto a Si substrate

To investigate the effects of surface corrugation on a subsequent transfer process, we released the 3-μm-thick GaAs layer from bulk GaAs(100) using the spalling process and transferred the layer onto a Si substrate. Then, we characterized the quality of the transferred GaAs layer based on SEM, XRD, and PL measurements. Fig. S2A shows the cross-sectional SEM images of the GaAs layer transferred onto the Si substrate. Because of the zig-zag corrugations on the surface of the released layer, undesirable air voids were formed along the interface between the GaAs layer and the SiO_x bonding layer. These voids hinder the reliable transfer process because adhesion between bonded layers is not uniform and air voids can expand or contract under temperature variation. Moreover, air voids can degrade the heat-dissipation capability and local-temperature uniformity of the transferred layer due to the low thermal conductivity of air. Although zig-zag corrugations impede the transfer process, the XRD and PL measurement results show that the crystal and material quality of the GaAs layer were maintained during the layer release/transfer processes [Fig. S2B and S2C].

[Note S3] Estimation of the crystal binding energy based on density functional theory (DFT)

To investigate the difference in binding energy of a heteroepitaxial interface and bulk crystal planes, we conducted DFT calculations to estimate the crystal binding energy of a heteroepitaxial interface and compared the result with those of main crystal planes in the III-V bulk. The DFT calculations were performed using the plane-wave pseudopotential code as implemented in Quantum Espresso (*57*), and the pseudopotential was described by the projector augmented wave (PAW) method (*58*) and Generalized Gradient Approximation (GGA) function (*59*). The kinetic-energy cutoff of plane waves was set to 450 eV and Γ-centered Monkhorst−Pack grids of 1 × 1 × 1 k-points were utilized for the Brillouin-zone integration. The force and energy convergence criterion were set to 0.02 eV $Å^{-1}$ and 10^{-5} eV, respectively.

In these calculations, we built three different atomic structures to estimate the crystal binding energy of the epitaxial interface between $In_{0.53}Ga_{0.47}As$(100) and InP(100) layers and those of (100) and (110) planes in the InP bulk. The atomic structures used for the calculation are illustrated in Fig. S3A. The binding energy was calculated by $E_b = E_{tot} - E_{slab1} - E_{slab2}$ (*60*), where E_{tot} is the total energy of the atomic structure system, and E_{slab1} and E_{slab2} are the total energy of one half of the structure without considering the other half. For instance, as shown in the atomic structure of InP(100)/$In_{0.53}Ga_{0.47}As$(100) in Fig. S3A, E_{slab1} and E_{slab2} represent the total energy of $In_{0.53}Ga_{0.47}As$(100) slab and InP(100) slab, respectively. The estimated binding energy of the (100) interface between InGaAs and InP was –44.78 eV, and those of the (100) and (110) planes in the InP bulk were –472.05 and –165.94 eV, respectively. The DFT calculation results indicate that (i) the crystal binding energy of the bulk (100) plane is larger than that of the bulk (110) plane, as expected and (ii) the interfacial bonding between the InP(100)/InGaAs(100) layers is weaker than the crystal bonding of the (100) and (110) planes in the InP bulk. This result implies that a heteroepitaxial interface between InP and InGaAs layers can become more preferable to the bulk crystal planes for the layer release in spalling processes. In addition, it is notable that the typical formation of lattice-mismatched one or few monolayers at an epitaxial interface were not

accounted for in this calculation. If the effect of the lattice-mismatched monolayers at the interface are introduced, we think that the difference in binding energies of a heteroepitaxial interface and bulk crystal planes can be even larger because of the localized misfit strain energy induced by the lattice-mismatched intermixing layers.

Furthermore, to estimate whether the layer-release process at an epitaxial interface can also be applied to other III-V heterostructures, we investigated the binding-energy contrast in GaAs/$In_{0.49}Ga_{0.51}P$ heterostructure (one of the representative lattice-matched systems) based on the additional DFT calculation. The atomic structures used for the calculation are illustrated in Fig. S3B. The crystal binding energy was calculated by the same method (*i.e.*, $E_{tot} - E_{slab1} - E_{slab2}$) used for the InP/InGaAs heterostructure. The estimated binding energy of the (100) interface between $In_{0.49}Ga_{0.51}P$ and GaAs was –51.61 eV, and those of the (100) and (110) planes in the GaAs bulk were –419.88 and –130.43 eV, respectively. This DFT calculation results also indicate that (i) the crystal binding energy of the bulk (100) plane is larger than that of the bulk (110) plane, and (ii) the interfacial bonding between the GaAs(100)/InGaP(100) layers is weaker than the crystal bonding of the (100) and (110) planes in the GaAs bulk. As with the result in the InP/InGaAs heterostructure (Fig. S3A), this result implies that a heteroepitaxial interface between GaAs and InGaP layers can become more preferable to the bulk crystal planes for the layer release in spalling processes. In addition to this binding energy contrast, it is also known an abruptly inverted heteroepitaxial interface between GaAs and InGaP layers can contain one or few monolayers of an undesirable lattice-mismatched III-V alloy which is induced by As–P phase intermixing (*61*, *62*). Considering that two contributing factors (binding-energy contrast and intermixing layer) for layer separation at an epitaxial interface are also valid in the lattice-matched GaAs/$In_{0.49}Ga_{0.51}P$ heterostructure, we think that the proposed technique can be extended to GaAs/InGaP heterostructures and probably generalized to a wide range of III-V heterostructures.

[Note S4] Estimation of the spalling depth using an analytical model

In this study, the spalling depth was calculated by an analytical model based on delamination theory (*31*, *45*, *46*). In this model, the spalling depth can be calculated based on the thermodynamic equilibrium condition of the film/substrate structure in which the total strain energy accumulated in the Ni film and the released layer is balanced with the crystal binding energy (*31*, *46*, *47*, *63*). A detailed calculation procedure is described with the schematic in Fig. S4 indicating the magnitude and direction of the stresses induced in the film/substrate structure.

To calculate this analytical model, we first need to know the elastic strain of the film and the substrate, which can be calculated from the measured film stress. The relationship between elastic strain and stress is expressed as follows (*45*):

$$\varepsilon = \frac{(1-\nu)}{Y}\sigma \quad (1)$$

where ε, σ, Y, and ν are the elastic strain, biaxial stress, Young's modulus, and Poisson ratio of a material, respectively. Then, the elastic strain energy accumulated in the stressor film (U_F) can be calculated as follows:

$$U_F = \frac{1}{2}\int_{\frac{t_S}{2}}^{\frac{t_S}{2}+t_f} \varepsilon_f \sigma_f dy = \frac{(1-\nu_f)}{2Y_f} t_f \sigma_f^2 \quad (2)$$

Because of the strong tensile stress of the stressor film, the compressive stress ($\sigma_{compression}$) and bending stress ($\sigma_{bending}$) are induced in the substrate (*45*). The total stress induced in the substrate can be estimated based on the film stress (σ_f) as follows:

$$\sigma_s = \sigma_{compression} + \sigma_{bending} = -\left(\frac{t_f}{t_s}\sigma_f + \frac{6t_f\sigma_f}{t_s^2}y\right) \quad (3)$$

The elastic strain energy in the substrate (U_S) accumulated from the substrate surface ($y = t_s/2$) to a specific release point ($y = y_s$) can be calculated as follows:

$$U_S = \frac{1}{2}\int_{y_s}^{\frac{t_S}{2}} \varepsilon_s \sigma_s dy = \frac{1}{2}\int_{y_s}^{\frac{t_S}{2}} \varepsilon_s(\sigma_{compression} + \sigma_{bending})dy = \frac{(1-\nu_s)}{2Y_s}\int_{y_s}^{\frac{t_S}{2}}\left(\frac{t_f}{t_s}\sigma_f + \frac{6t_f\sigma_f}{t_s^2}y\right)^2 dy$$
$$= \frac{(1-\nu_s)}{2Y_s}\frac{t_f^2}{t_s}\sigma_f^2\left[\frac{7}{2} - 12\left(\frac{y_s}{t_s}\right)^3 - 6\left(\frac{y_s}{t_s}\right)^2 - \left(\frac{y_s}{t_s}\right)\right] \quad (4)$$

In this model based on the thermodynamic equilibrium condition, the layer is released at the point where the strain energy accumulated in the film/substrate ($U_F + U_S$) is equal to the crystal binding energy of the substrate (γ_S) (*31*). Thus, we could calculate the spalling depth that satisfies the thermodynamic equilibrium condition ($\gamma_S = U_F + U_S$) for the layer release at y_s:

$$\gamma_S = \frac{(1-\nu_f)}{2Y_f} t_f \sigma_f^2 + \frac{(1-\nu_s)}{2Y_s}\frac{t_f^2}{t_s}\sigma_f^2\left[\frac{7}{2} - 12\left(\frac{y_s}{t_s}\right)^3 - 6\left(\frac{y_s}{t_s}\right)^2 - \left(\frac{y_s}{t_s}\right)\right]. \quad (5)$$

The positive real solution of this cubic equation corresponds to the release point (y_s). Therefore, if we know the physical parameters of materials (Y_f, ν_f, Y_s, ν_s, and γ_S), the film stress (σ_f), and the thickness of the film and the substrate (t_f and t_s), the spalling depth can be simply calculated from y_s (*i.e.*, $d_{spall} = t_s/2 - y_s$).

[Note S5] Estimation of the layer-release yield of InP/InGaAs heterostructures

As shown in Fig. S7A, the zig-zag corrugations on the surface of the remaining substrate after the spalling process in the III-V(100) bulk can be observed in the optical microscopy (OM) image. In case the periodic stripes corresponding to the corrugations were not observed in the OM image of a spalled sample, that sample's surface was flat when imaged by SEM; this indicates that layer release occurred at an epitaxial interface. Thus, we could estimate the layer-release yield of the InP/InGaAs heterostructure using OM images taken from the entire region of the remaining substrate after the layer-resolved mechanical separation process. The estimated yield is shown in Figs. S7B and S7C. After spalling process III, we took 441 OM images from the entire spalled region (sample size of 15 × 15 mm^2). To evaluate the yield, we divided each OM image into 50 areas of 100 × 100 μm^2, counted the number of flat and defect-free areas and defined the yield of one region covered by the OM image by the percentage of counted areas. We repeated this process

for all OM images. The yield-mapping images of all regions corresponding to the 441 OM images are shown in Fig. S7B. Here, the color of each pixel indicates the yield of each region. Figure 'a' shows a representative OM and top-view SEM images for a high yield (> 95%) and Figure 'b' shows ones for a relatively low yield due to zig-zag corrugations or cracks. The histogram of the yield distribution is plotted in Fig. S7C. The overall layer-release yield estimated from this method was about 78%. To compare the quality of the layer-resolved III-V mechanical separation with that of conventional Si(100) spalling, we released a thin Si layer through the same process and evaluated the yield of Si spalling using the same method. The sample size of the Si layer was 22 × 22 mm^2. Fig. S7D shows the mapping image of the spalling yields estimated from 961 OM images and Fig. S7E shows the histogram plot of the yield distribution. The overall process yield for the entire region was about 80%, which is comparable with that of the III-V result. This implies that the process yield in this study was limited by the non-ideal manual process in a laboratory environment rather than by the process scheme of the proposed layer-resolved mechanical technique for III-V heterostructures. As suggested in several previous reports, we expect that the process yield can be further increased if the mechanical separation process is performed by using force-controlled spalling equipment. After crack initiation by an external force, the layer-release process relies on a quasi-spontaneous exfoliation (*i.e.*, quasi-self-propagation), by which the crack propagates with a uniform layer thickness under the accumulated strain energy balanced with the crystal binding energy. Thus, after the crack initiation, an external force should be maintained with a uniform magnitude and sustained direction and an excess external force should be minimized. Furthermore, it is known that the layer-release yield can be further increased in a wafer-scale process because large-scale mechanical separation process requires a smaller external force for quasi-spontaneous exfoliation (*16*, *18*, *20–22*).

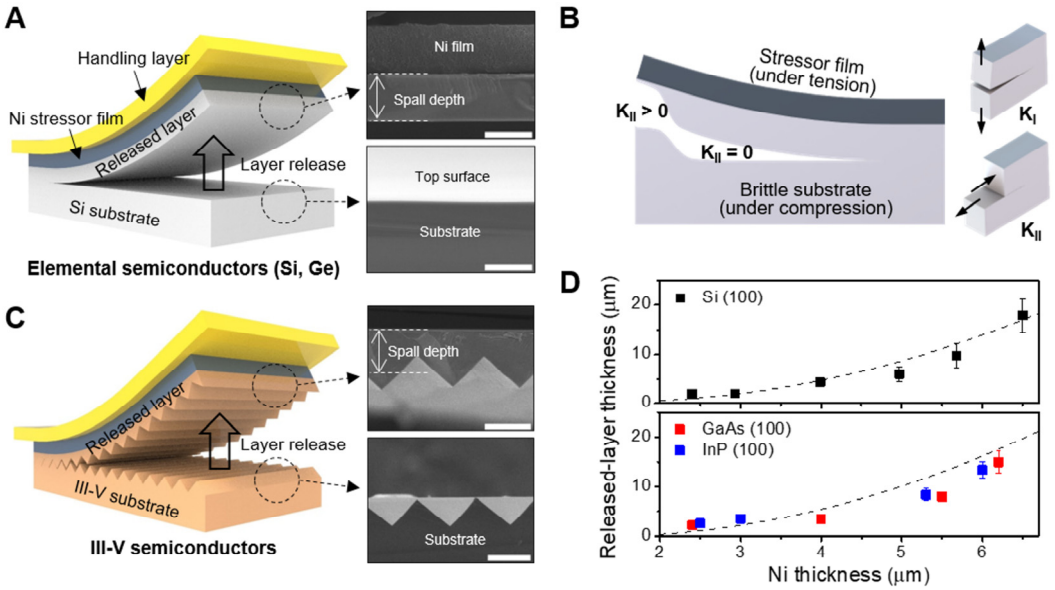

Fig. S1.

Thickness-controlled spalling process for the layer release of single-crystalline elemental and zinc-blende III-V compound semiconductors. (**A**) A schematic of the spalling process for Si(100) and cross-sectional SEM images of the released layer and remaining substrate, showing that the surfaces of the released Si layers are flat and uniform. The scale bar is 3 μm. (**B**) A schematic of the crack trajectory and the mechanism of the spalling process. Under strong misfit stress in the stressor film and substrate, a crack is initiated near the substrate edge with two major stress intensity factors (K_I and K_{II}); it propagates straightly parallel to the film/substrate interface at a specific depth at which $K_{II} = 0$. (**C**) A schematic of the spalling process for III-V(100) semiconductors with a zinc-blende structure and cross-sectional SEM images of the released GaAs(100) layer and the remaining substrate. In contrast to Si, the surface of the released III-V layers is not flat; periodic zig-zag corrugations are observed. The scale bar is 5 μm. (**D**) The thickness of the released Si(100), GaAs(100), and InP(100) layers depends on the thickness of the Ni stressor film.

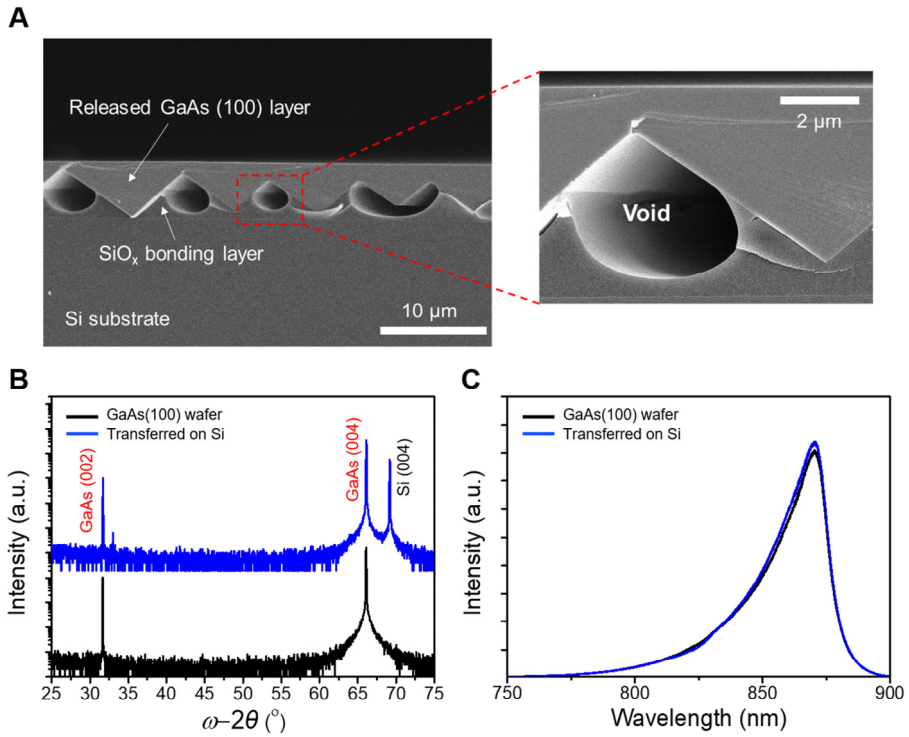

Fig. S2.

Characterizations of a GaAs layer released from bulk GaAs(100) and transferred onto a Si substrate. (**A**) Cross-sectional SEM image of the transferred GaAs(100) layer on a Si substrate after the spalling process. (**B**) Wide-range XRD ω–2θ scans and (**C**) steady-state room temperature PL spectra of the bulk GaAs(100) wafer and the GaAs(100) layer after the layer release/transfer processes.

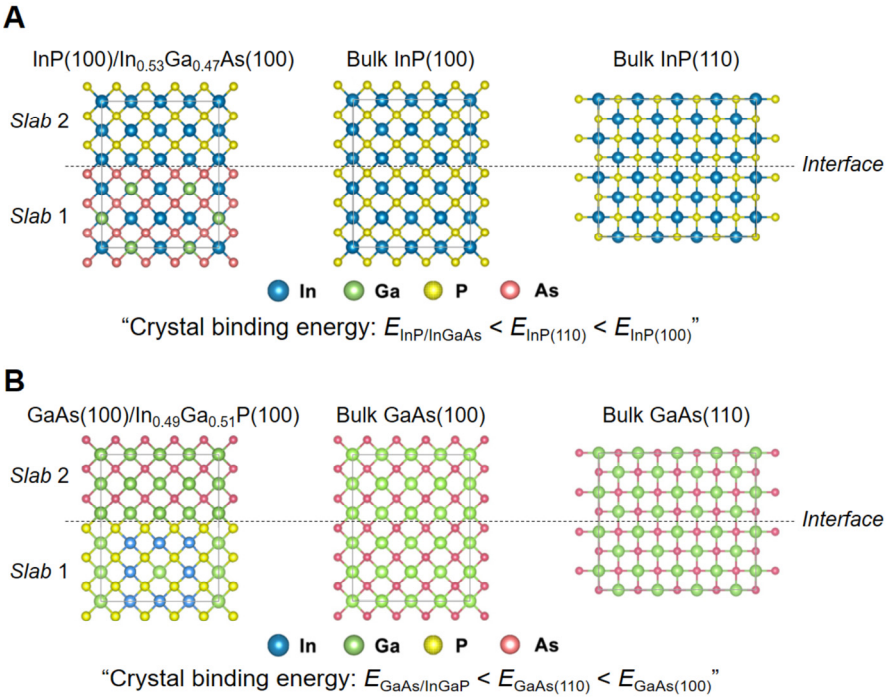

Fig. S3.

DFT calculation for estimation of crystal binding energies. (**A**) The atomic structures of InP(100)/$In_{0.53}Ga_{0.47}As$(100), bulk InP(100), bulk InP(110) and (**B**) those of GaAs(100)/$In_{0.49}Ga_{0.51}P$(100), bulk GaAs(100), bulk GaAs(110), which were used for the DFT calculations. The calculation results showed that the interfacial bonding between the heteroepitaxial layers is weaker than the crystal bonding of the (100) and (110) planes in the bulk.

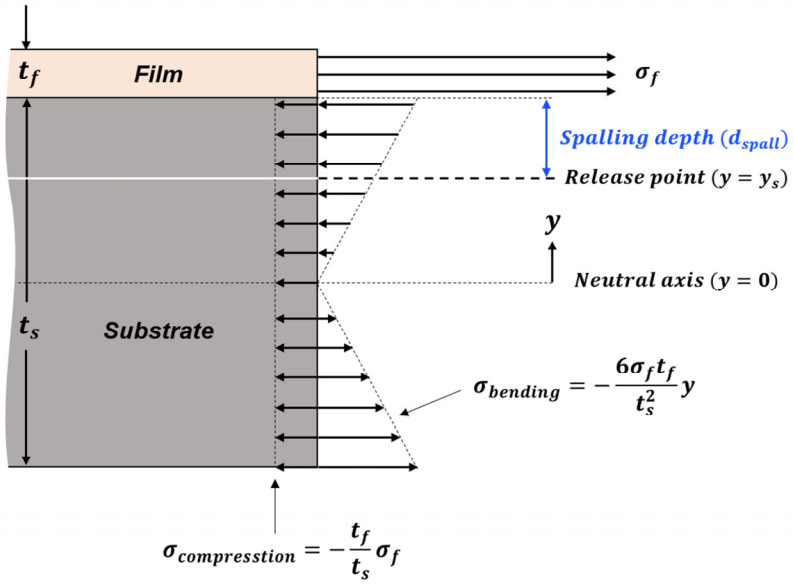

Fig. S4.

Schematic of the magnitude and direction of stresses induced in the film/substrate structure. Assuming that the stressor film is under tension, the film-induced stresses in the substrate are composed of the compressive stress and the bending stress (*31*, *45*). The black-dashed line indicates a specific release point ($y = y_s$).

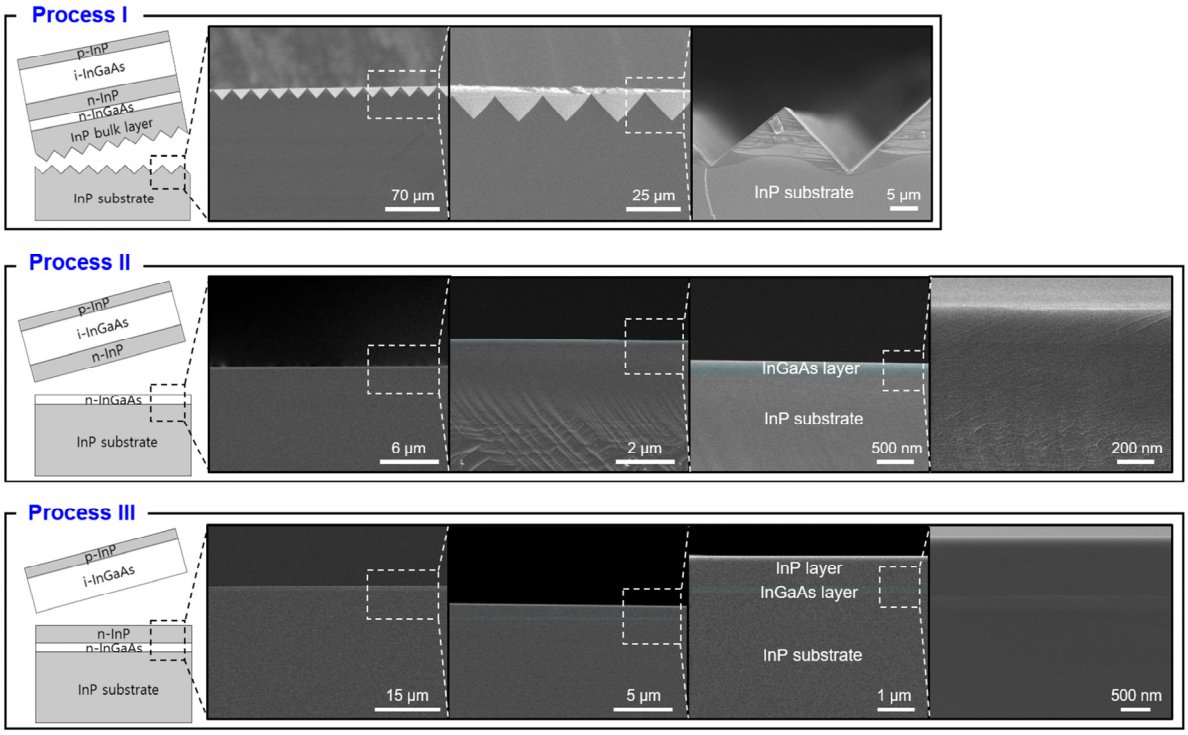

Fig. S5.

Cross-sectional SEM images of the remaining substrates with various magnifications after process I, II, and III. The third SEM image for each process is identical to the image shown in Fig. 2D of the main text. The color and brightness of the 200-nm-thick InGaAs layers in the images, except for the fourth images in process II and III, have been adjusted to make them more visible.

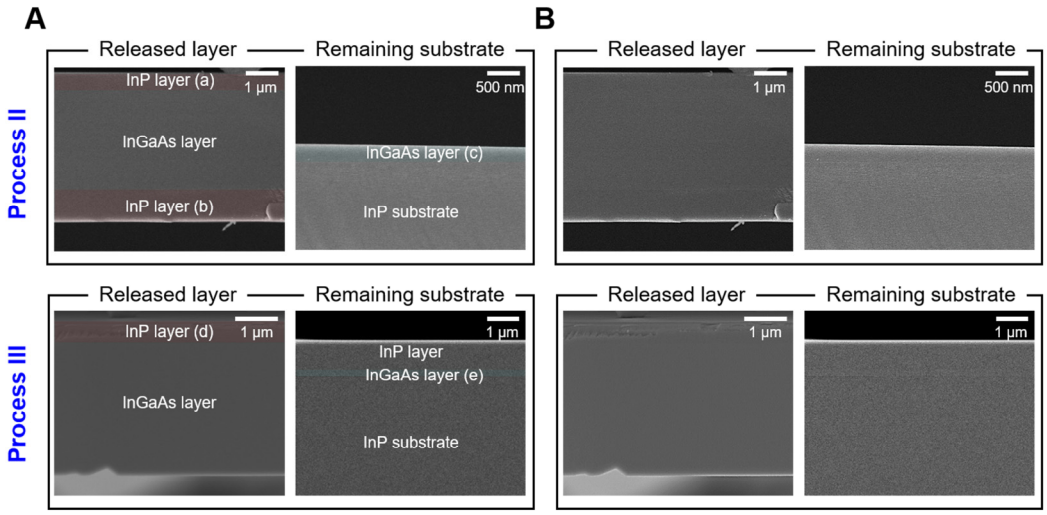

Fig. S6.

Original versions of the false-colored SEM images. (**A**) False-colored cross-sectional SEM images of the released layers and the remaining substrate after process II and III (shown in Fig. 2D) and (**B**) their original SEM images. The color and brightness of the relatively thin epitaxial layers (denoted as *a*, *b*, *c*, *d*, and *e* regions) have been adjusted to make them more visible.

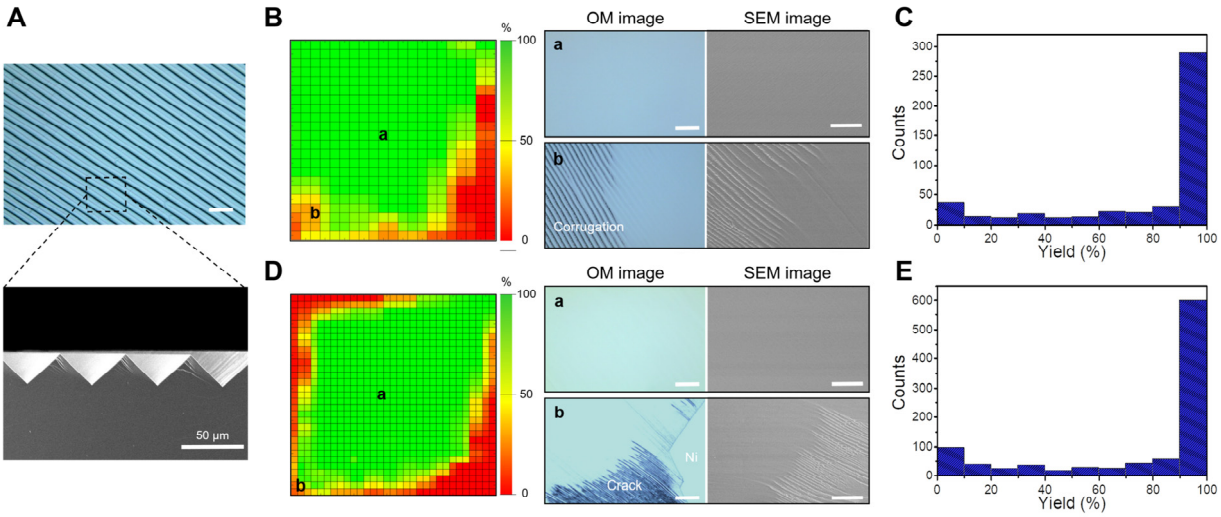

Fig. S7.

Estimation of the layer-release yield at the InP/$In_{0.53}Ga_{0.47}As$ interface. (**A**) OM image of the surface of the remaining substrate after the layer release in the InP bulk and the cross-sectional SEM image of the substrate defined by the dashed box in the OM image. It can be confirmed that the periodic stripes in the OM image correspond to zig-zag corrugations. (**B**) The yield-mapping image for the layer-resolved mechanical separation (process III) and representative OM and top-view SEM images for a high yield (denoted by 'a', yield ~98%) and a relatively low yield (denoted by 'b', yield = ~40%). The InP/InGaAs epitaxial layer was released from 'b' to 'a'. (**C**) Histogram of the yield distribution for the layer-resolved mechanical separation. (**D**) The yield-mapping image for the conventional Si(100) spalling and representative OM and top-view SEM images for a high yield (denoted by 'a', yield ~98%) and a relatively low yield (denoted by 'b', yield ~40%). The Si layer was released from 'b' to 'a'. (**E**) Histogram of the yield distribution for Si spalling. Scale bars in all OM and top-view SEM images are 100 μm.

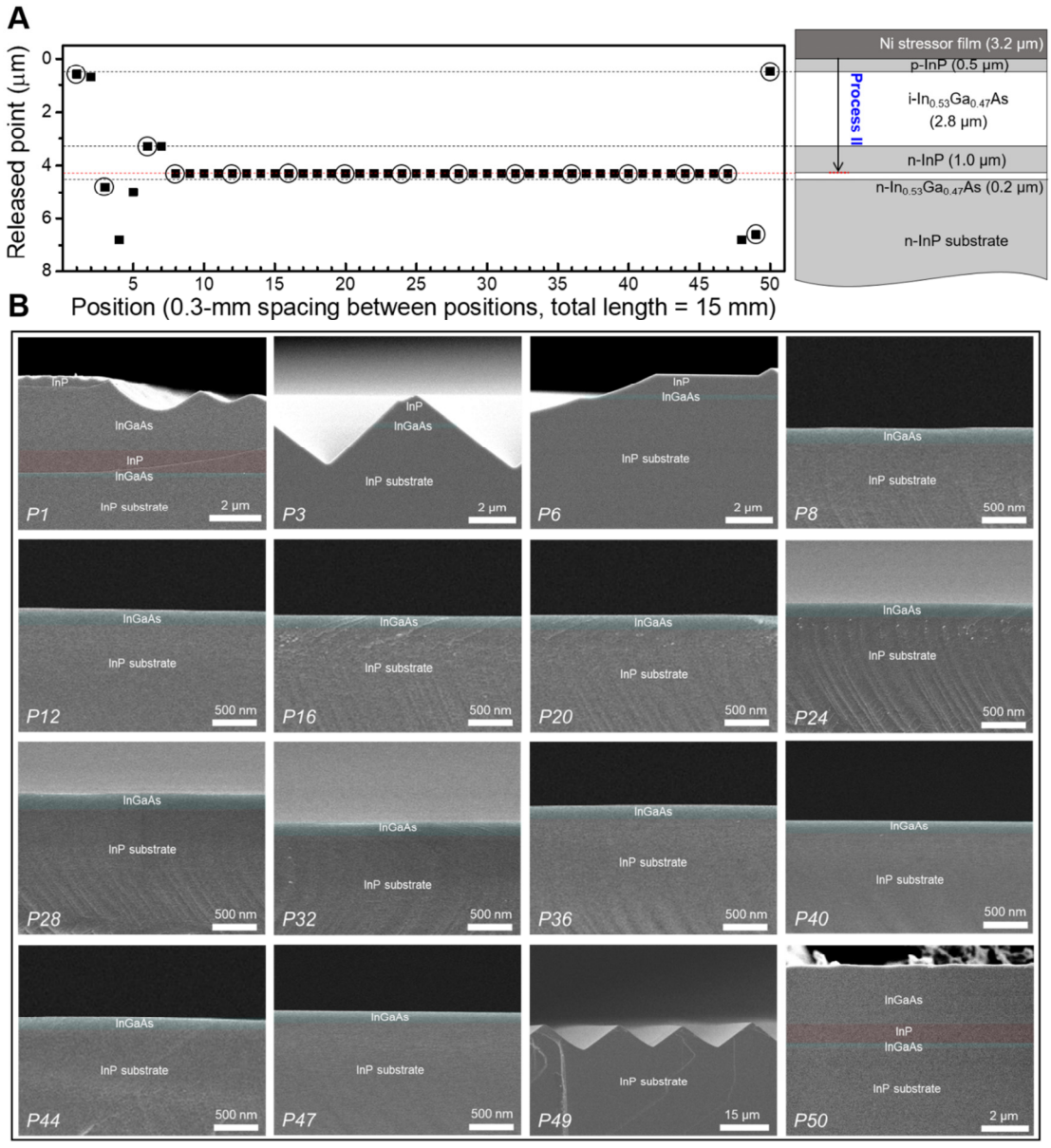

Fig. S8.

Uniformity evaluation of the released points after process II. (**A**) The plot for the released points at 50 positions covering the entire region of the spalled sample. The released points were evaluated by measuring the thickness of the top epitaxial layer in the remaining substrate after obtaining the cross-sectional SEM images from the 50 positions. The released point means the thickness of the released layer estimated from the thickness of the top epitaxial layer in the remaining substrate. The sample size was 15 × 15 mm^2 and the spacing between the measured positions was approximately 0.3 mm. The release points corresponding to the heteroepitaxial interfaces are denoted by dashed lines among which the designed local symmetry plane for process II is highlighted by the red dashed line. (**B**) Representative cross-sectional SEM images of the remaining substrate at the positions denoted by circles in the plot (A).

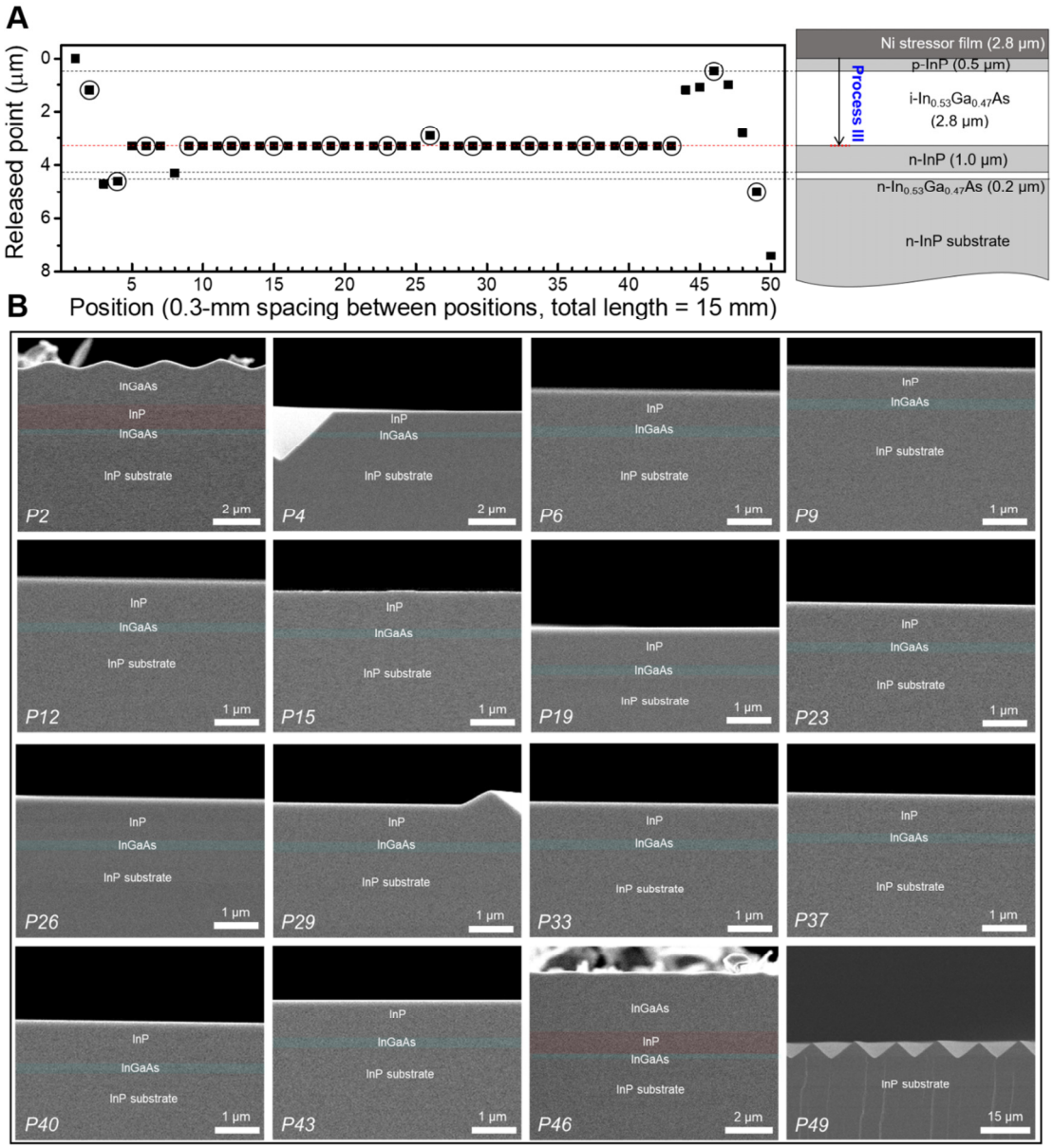

Fig. S9.

Uniformity evaluation of the released points after process III. (**A**) The plot for the released points at 50 positions covering the entire region of the spalled sample. The released points were evaluated by measuring the thickness of the top epitaxial layer in the remaining substrate after obtaining the cross-sectional SEM images from the 50 positions. The released point means the thickness of the released layer estimated from the thickness of the top epitaxial layer in the remaining substrate. The sample size was 15 × 15 mm^2 and the spacing between the measured positions was approximately 0.3 mm. The release points corresponding to the heteroepitaxial interfaces are denoted by dashed lines among which the designed local symmetry plane for process III is highlighted by the red dashed line. (**B**) Representative cross-sectional SEM images of the remaining substrate at the positions denoted by circles in the plot (A).

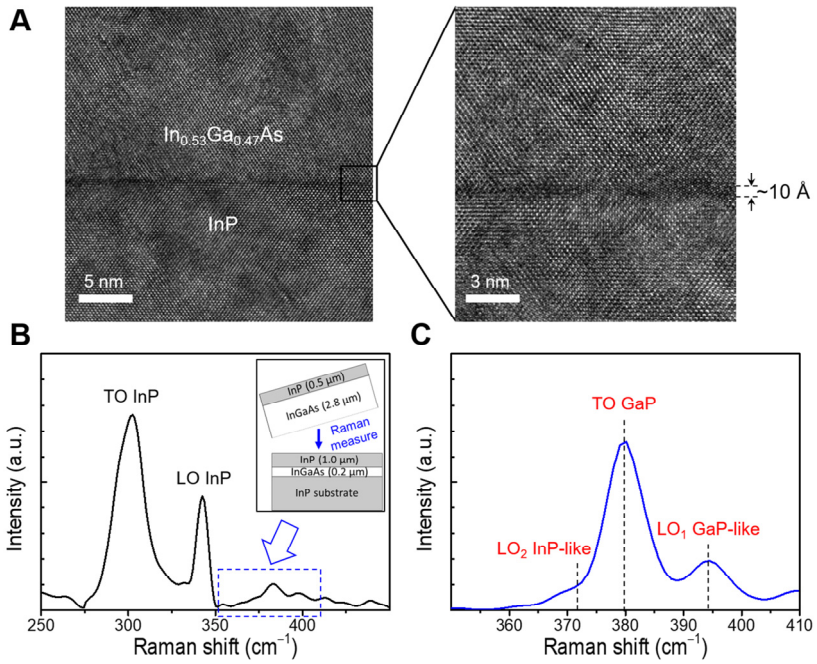

Fig. S10.

Confirmation of undesirable intermixing layers formed at the epitaxial interface of the lattice-matched InP/$In_{0.53}Ga_{0.47}As$ heterostructure. (**A**) High-resolution TEM images at the heteroepitaxial interface between InP and $In_{0.53}Ga_{0.47}As$ layers, showing the presence of an intermixing layer with a two- or three-monolayer thickness. (**B**) The Raman spectrum measured on the surface of the remaining substrate after process III (adopted from Fig. 3D of the main text), where non-negligible sub-peaks are observed in the range of 350–410 cm^{-1}. (**C**) The Raman spectrum measured in the sub-peak region (350–410 cm^{-1}) denoted by the blue dashed box in (B). The spectrum with the GaP-like LO- and TO-mode peaks (*64*) indicates that the epitaxial interface contains an InGaP-like undesirable intermixing layer induced by phase intermixing of As–P atoms. In the proposed layer separation technique, this intermixing layer can facilitate the layer release at the epitaxial interfaces, and further, the few-monolayer thickness of the intermixing layer can suppress the probability of the crack propagation taking the detour path to the bulk crystal planes, leading to make the straight crack propagation at the epitaxial interface more stable in the layer-release process.

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