A Jitter-Robust 40Gb/s ADC-Based Multicarrier Receiver Front End in 22nm FinFET

Yuanming Zhu*, Julian Camilo Gomez Diaz*, Srujan Kumar Kaile, Il-Min Yi, Tong Liu, Sebastian Hoyos, and Samuel Palermo

Texas A&M University, College Station, TX, USA
*Equally Credited Authors (ECAs)

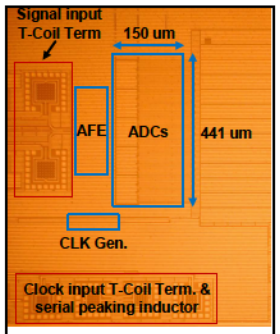
Demand for increased data-rates in serial link transceivers calls for innovative architectures capable of overcoming communications impairments such as limited channel bandwidth and stringent jitter specifications. While mixed-signal and ADC-based receiver architectures that utilize simple pulse amplitude modulation (PAM) can take advantage of technology scaling, it is becoming increasingly difficult to deal with the extremely short baseband pulse widths. This paper presents a wireline receiver front-end (RXFE) architecture that supports multicarrier signaling to provide a ~3X relaxation in clock jitter requirements.

Figure 1 shows the implemented RXFE architecture and the multicarrier signal power spectral density, where orthogonality is leveraged to allow for band overlapping and improved spectral efficiency. The multicarrier signal is formed by three bands to support a total 40Gb/s data rate. This includes baseband (BB) PAM4 operating at 4GS/s and mid-band (MB) and high-band (HB) that both carry 4GS/s QAM16 on 4GHz and 8GHz orthogonal carriers, respectively. This 4GS/s rate has a symbol duration that is 5X longer than a conventional 20GS/s baseband PAM4 signal. Thus, the proposed architecture offers jitter robustness that has been evaluated through system-level simulations with different clock jitter amounts on both the receiver LO down-conversion and sampling clocks when operating over a channel with 20dB loss at 10GHz. The results show that the proposed multicarrier system which can tolerate up to $1.6ps_{rms}$ jitter, whereas a BB PAM4 system cannot tolerate more than $600fs_{rms}$ at a BER=10^{-4}.

As shown in Fig. 2, after the input T-coil termination the multiband signal passes through three parallel continuous-time linear equalizers (CTLEs) designed to optimally equalize each of the bands and relax RXFE linearity requirements. The BB CTLE drives a single segment consisting of a dummy mixer, integrating sinc filters, and 4-way time-interleaved ADC, while the MB and HB CTLE both drive two I/Q segments with the mixers switched with the 4GHz and 8GHz LO signals, respectively. Inverter-based CTLE structures with two signal paths are utilized [1], with the top branch low-pass response subtracted from the bottom path all-pass response to form a high-pass characteristic. The advantage of using this architecture lies on the ability to set equal transconductances for the top and bottom branches to significantly attenuate the low-frequency component of the multiband signal. This results in a more optimal AC response, improved linearity, and lower output-referred noise for the MB and HB segments. The RXFE sinc filters are implemented with resettable integrators built with dynamic amplifiers with common-restoration and programmable source degeneration resistances for gain control.

The Fig. 2 timing diagram shows the integrator operation and interface with the 4-way time-interleaved ADC. The integrator in each segment operates in a 2-way time-interleaved manner to allow for an integrator reset cycle. In this case, ϕ_{ini} going high marks the start of the integration period. The clock ϕ_{A1} will go high right after this to start tracking the output and then perform sampling after ϕ_{ini} goes low. The 25% percent duty cycle ϕ_{rst} creates an integrator hold phase that relaxes the timing requirement for this ADC sample clock. The integrator capacitor is then reset when ϕ_{rst1} goes high. Each 7-bit 1GS/s unit ADC is formed by a pipelined-SAR structure with an output level shifting (OLS) settling technique [2] for low power and high-speed operation. 4-bits are converted in both pipeline stages, with 1-bit redundancy between the two stages to relax the gain, offset, and reference settling requirements. Both stages employ parallel comparators that are asynchronously activated sequentially for each conversion step, eliminating the comparator reset delay and offering significant speed-up.

Fig. 3 shows the RXFE clock generation circuitry that generates the HB and MB LOs and the 10 input clocks for the integrators and ADC local clock generation blocks in each segment. A 16GHz differential clock input passes through a CML divider and CML-to-CMOS converters to generate 4-phase 8GHz clock signals for the HB LO signals. A subsequent CMOS divider generates 8-phase 4GHz clock signals, with four of these phases used for the MB LO signals. Additionally, these eight 4GHz clocks signals are provided to 10 6b phase interpolators to generate the clocks for the integrators and ADCs with independent sampling phase control. Phase mismatches between I and Q LO signals are compensated with skew calibration blocks consisting of distribution buffers that have digitally-controlled capacitive loading.



Die micrograph.

To verify the proposed RXFE jitter robustness, the distribution buffers of the LO and integrator/ADC clocks operate on a power domain with programmable noise injection. Large shunting NMOS transistors are driven by either an internal PRBS generator or an external signal to provide jitter with varying frequency content.

As shown in the 22nm FinFET die micrograph, the entire RXFE occupies $0.84mm^2$ when the input T-coil and clock buffer inductors are included. The CTLE, mixers, and integrators occupy 102um X 225um of this area, while the ADCs consume 150um X 441um. Fig. 4 shows the DFT from one of the decimated (621x) 4-way time interleaved ADC outputs when sampling a low-frequency input at 4GS/s, with an achieved SNDR and SFDR of 33.7dB and 42 dB, respectively. The ADC Nyquist rate ENOB through the entire RXFE is 4.2b and 4.53b when the RXFE is de-embedded. The frequency response of the CTLEs are measured from the ADC output using single-tone inputs, with the BB, MB, and HB CTLEs achieving a highest normalized peaking of 8dB, 7dB, and 3dB, respectively. Fig. 5 show RXFE measurement results with a 40Gb/s multiband input signal with independent PRBS15 patterns in the bands generated with a Keysight M8195A AWG with an $800mV_{ppd}$ total swing. This is passed through a channel with 20dB insertion loss at 10GHz (conventional baseband PAM4 Nyquist) and data is collected with and without jitter added. For the maximum $1.6ps_{rms}$ jitter injection, the BB channel has an average voltage margin of 24 ADC codes at a BER=10^{-5} and the MB and HB constellations have a respective EVM of 20.4dB and 18.8dB that translates to BERs of 10^{-6} and $3.5x10^{-5}$. These constellations suffered a respective EVM degradation of 0.5dB and 0.8dB with respect to the no jitter added case. Fig. 6 compares this RXFE with other ADC-based wireline RXFE that utilize conventional PAM4 and multi-tone signaling. The proposed multicarrier RXFE can operate with the highest $1.6ps_{rms}$ jitter and achieves 3.05pJ/bit power efficiency.

Acknowledgment:

This work was supported in part by SRC TxACE Grant 2810.013 and NSF Grant 1930828. Chip fabrication services were provided through the Intel University Shuttle Program.

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2022 IEEE Custom Integrated Circuits Conference (CICC) | 978-1-6654-0756-4/22/$31.00 ©2022 IEEE | DOI: 10.1109/CICC53496.2022.9772868

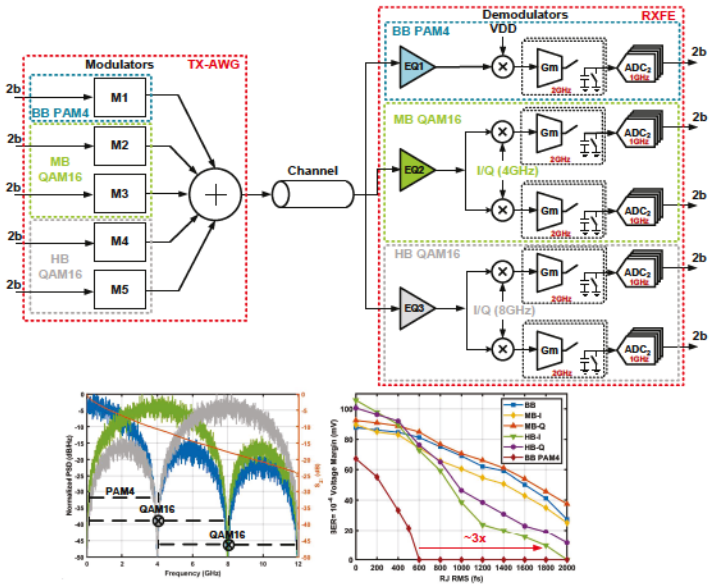

Fig. 1. Multicarrier RXFE architecture and modeling results.

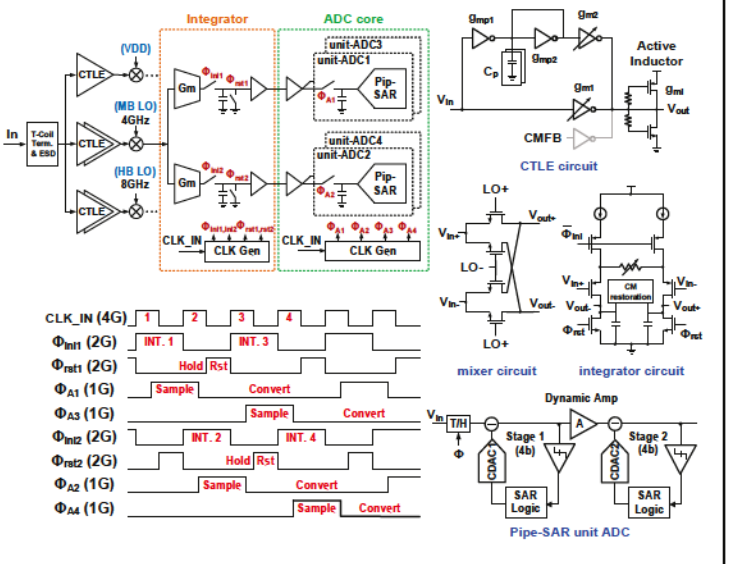

Fig. 2. RXFE schematic and timing diagram.

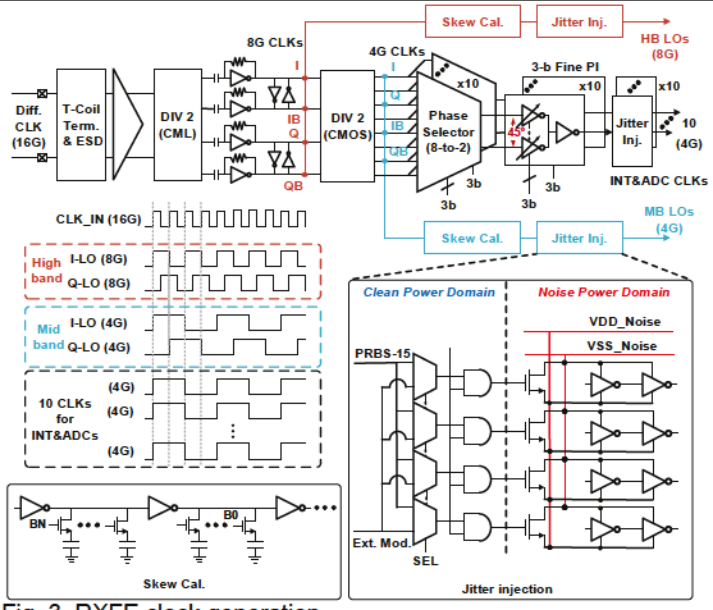

Fig. 3. RXFE clock generation.

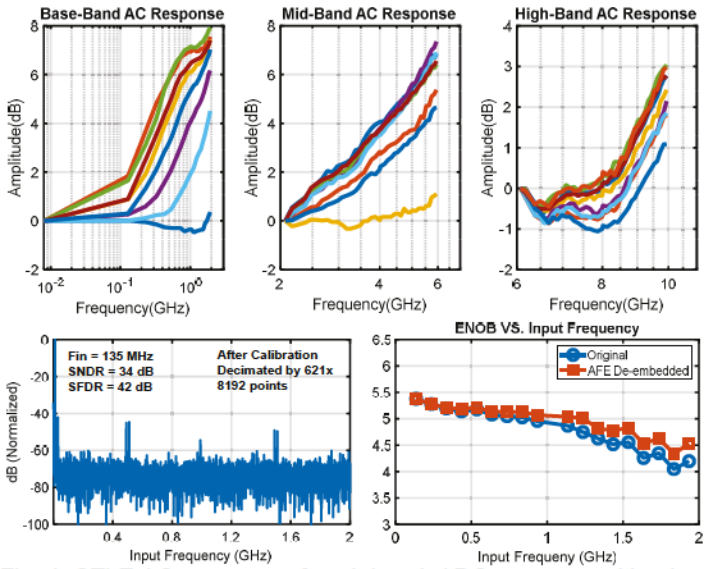

Fig. 4. CTLE AC response of each band, ADC spectrum with a low frequency input, and ENOB vs input frequency.

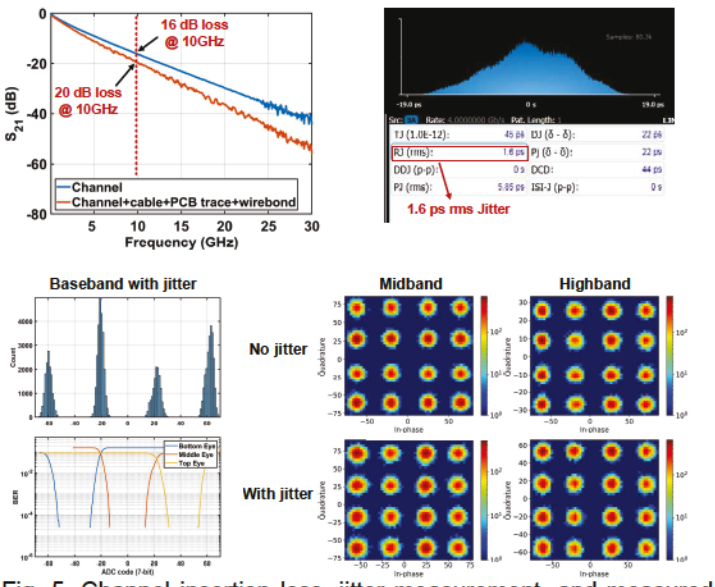

Fig. 5. Channel insertion loss, jitter measurement, and measured PAM4 and QAM16 constellations.

Specification	LaCroix ISSCC 2019	All ISSCC 2019	Kim ISSCC 2019	Upadhaya ISSCC 2018	Wang ISSCC 2018	This Work
Technology	7 nm FinFET	7 nm FinFET	14 nm FinFET	16 nm FinFET	16 nm FinFET	22 nm FinFET
Modulation	PAM-4	PAM-4	64-QAM DMT	PAM-4	PAM-4	Multicarrier
Power Supply (V)	0.75, 0.8, 1.2	0.8, 1	0.7, 0.75, 0.8	0.85, 0.9, 1.2, and 1.8	0.9, 1.2	0.85, 0.95, 1.2
Data Rate	60 Gb/s	56 Gb/s	56 Gb/s	56 Gb/s	64.375 Gb/s	40 Gb/s
Fs (GS/s)	30	28	22.4	28	32	5 x 4
ADC Structure	TI-SAR	TI-SAR	TI-Pipe-SAR	TI-SAR	TI-Folding Flash	TI- Pipe-SAR
Pre-Equalization	CTLE	CTLE	No	CTLE	CTLE	CTLE
ENOB @ Nyquist	N/A	4.74 bits	N/A	4.43 bits	4.33 bits	4.5 bits
Area	0.84 mm²	0.32 mm²	0.26 mm²	N/A	0.16 mm²	0.84 mm²
Max. Compensated Channel Loss	32 dB @ 14 GHz	40 dB @ 14 GHz	28 dB @ 14 GHz	32 dB @ 14 GHz	30 dB @ 16 GHz	20 dB @ 10 GHz
RMS Jitter	160 fs	225 fs	N/A	180 fs	162 fs	1.6 ps
BER	< 1e-6	< 1e-5	< 2e-4	< 1e-12	< 1e-4	< 1e-4
AFE + ADC Power	303 mW	180 mW	93.2 mW	N/A	283.9 mW	122 mW
Power Efficiency (pJ/bit) AFE + ADC	5.05	3.2	1.6	5.8	4.44	3.05

Fig. 6. Performance summary and comparison table.