A 38GS/s 7b Time-Interleaved Pipelined-SAR ADC with Speed-Enhanced Bootstrapped Switch in 22nm FinFET

Yuanming Zhu, Tong Liu, Srujan Kumar Kaile, Shiva Kiran, Il-Min Yi, Ruida Liu, Julian Camilo Gomez Diaz, Sebastian Hoyos, and Samuel Palermo

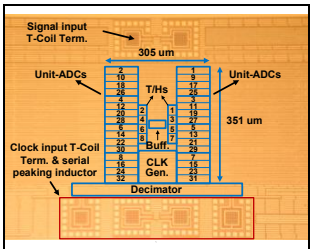
Texas A&M University, College Station, TX, USA

High-speed time-interleaved ADCs are becoming more common in wireline receiver front-ends due to the enabling of subsequent digital processing for equalization and easier support of higher-order modulation schemes [1]. As technology nodes scale, ADCs based on the digital-intensive SAR architecture are more pervasive. However, implementations with the most common SAR algorithm that has sequential single-bit conversion cycles can result in large time-interleaving factors. Also, the sampling of wideband analog signals associated with higher data rates is difficult for conventional bootstrapped switch (BS) T/H circuits that have not adequately scaled in performance. One reason for this is that the low-duty-cycle sampling clocks, which are utilized for avoiding sampling crosstalk between time-interleaved sub-ADCs, shorten the tracking time and requires improvements in T/H circuit startup time. This motivates the use of simple NMOS switches in high-speed ADCs [2], [3]. However, this can negatively impact the high-speed linearity and ADC front-end bandwidth and also require higher supply voltages. This paper presents an ADC that utilizes both a high-bandwidth interleaver architecture based on a speed-enhanced bootstrapped switch and a pipelined-SAR unit ADC with output level shifting (OLS) settling [4] to enable low-power high-speed operation. At 38GS/s, the 7b ADC achieves 41.9fJ/conv.-step at low input frequencies, 64.1fJ/conv.-step at Nyquist, and has 20GHz 3dB bandwidth.

An overview of the ADC is shown in Fig. 1. The ADC core consists of an 8-way first-rank interleaver that samples and buffers the input signal, 32-way interleaved unit-ADCs, and a multi-phase clock generation block. High input bandwidth is achieved with differential T-coil structures that distribute the input pad, ESD diode, 100Ω termination, and input buffer capacitances. Clock generation is performed with a differential external $f_s/2$ clock connected to an on-chip CML buffer that drives a CML divider to generate 4 phases spaced at 90°. These 4 phases are then fed into the ADC core multi-phase generation block that outputs the 8 first-rank T/H phases and the 32 unit ADC clock phases. The digital output data bits and clock signals from each unit ADC are captured by a synchronization block connected to a decimator that down samples the output data rate to the MHz-range for measurement purposes.

Figure 2 shows the two-stage interleaver architecture and ADC clocks timing diagram. Parallel even and odd input buffers drive half of the first-rank 8-way T/Hs where the input is sampled and held utilizing 25% duty-cycle $f_s/8$ pulses to avoid sampling crosstalk. These critical input T/H pulses are generated utilizing $f_s/4$ differential CML-level clocks that are passed through a CML-to-CMOS converter and then enabled with an $f_s/8$ signal that is produced by dividing the CMOS-level $f_s/4$ clocks. Skew calibration is then performed with distribution buffers that have digitally-controlled capacitive loading. The second-rank consists of a buffer that drives 4 parallel T/Hs clocked at $f_s/32$ with 90° phase offsets, such that only one unit-ADC sampling switch is on at a time and overlaps the corresponding first-rank hold phase.

A detailed interleaver schematic and the proposed speed-enhanced bootstrapped switch is shown in Fig. 3. While the 25% duty cycle first-rank T/H signals reduce the input buffer loading and sampling crosstalk, it does necessitate that the T/H have a fast start-up time. This is difficult because the T/H is loaded by the second-rank buffer that has to be sized sufficiently to drive long routing parasitics to the second-rank switches. The proposed BS topology modifies the M_{N1} gate connection to come directly from Φ. As soon as the clock is enabled, M_{N1} turns on to transfer the boosted voltage to the M_{NSW} gate to reduce start-up time and offer better tracking of the high-speed input. M_{N5} is also added to rapidly pull up the M_{NSW} gate signal upon entering track mode to further improve the start-up time. Post-layout transient simulation waveforms show that the proposed topology has a wider switch on pulse, faster start-up, and better tracking relative to a conventional bootstrapped switch. At the effective $f_s/8$ T/H frequency of 4.75GHz for 38GS/s operation, this results in 0.75b and 1.1b improvement in ENOB with 20GHz and 30GHz input signals, respectively. Projecting this bootstrapped switch operation in ADCs with higher-speed 16GHz clocks shows further improvement of 1.8b with both 20GHz and 30GHz input signals.



Die micrograph.

Figure 4 shows the 7b unit pipelined-SAR ADC. Both pipeline stages convert 4-bits, with 1-bit redundancy between the stages to relax the first stage gain, offset, and reference settling requirements. The second-rank switch is the same proposed bootstrapped topology to reduce the input sampling time constant and improve linearity. kT/C noise requirements are satisfied with CDAC1 and CDAC2 set at 32fF and 16fF, respectively. Both stages employ parallel comparators that are asynchronously activated sequentially for each conversion step, eliminating the comparator reset delay and offering significant speed-up. A clocked inverter-based buffer that achieves a gain of ~4 serves as the residue amplifier stage. An OLS technique [4] allows the residue amplifier output to only settle to 50% of the steady state value, which results in a 1.15τ settling time that is roughly 3X faster than a conventional CML amplifier's settling for 4-bit resolution. This allows for lower average power due to the dynamic amplifier's reduced activation time. Both the first and second pipeline stages have independent reference DACs and buffers, which avoids crosstalk and allows for inter-channel gain mismatch and inter-stage gain error calibration.

As shown in the 22nm FinFET die micrograph, one unit pipelined-SAR ADC occupies 20um X 90um and the entire core 32-way time-interleaved ADC has an active area of 0.107mm^2. Measurements are performed with comparator offset, channel gain mismatch, and timing-skew errors foreground calibrated based on sine-fitting and statistical averaging. Fig. 5 shows the DFT of the decimated (1089X) ADC output when sampling an 18.9GHz sinusoidal input at 38GS/s, with an achieved SNDR and SFDR of 35.6 dB and 43.7dB, respectively. The proposed speed-enhanced bootstrapped switch allows for a measured 20GHz input bandwidth with the wirebonded chip-on-board test setup, while de-embedding the wirebond parasitics show that 28GHz bandwidth is possible. Fig. 6 compares this work against previous 7-8b ADCs operating at ≥28GS/s. Total ADC power consumption is 119.7mW, with 82.65mW dissipated in the pipelined-SAR unit ADCs and clock generation circuitry operating on a 0.85V supply and 37.05mW from the 0.9V proposed interleaver. Overall, the high input bandwidth and SNDR enabled by the proposed interleaver and pipelined-SAR unit ADC with OLS settling allows for significant improvement in the Nyquist rate FoM.

Acknowledgment:

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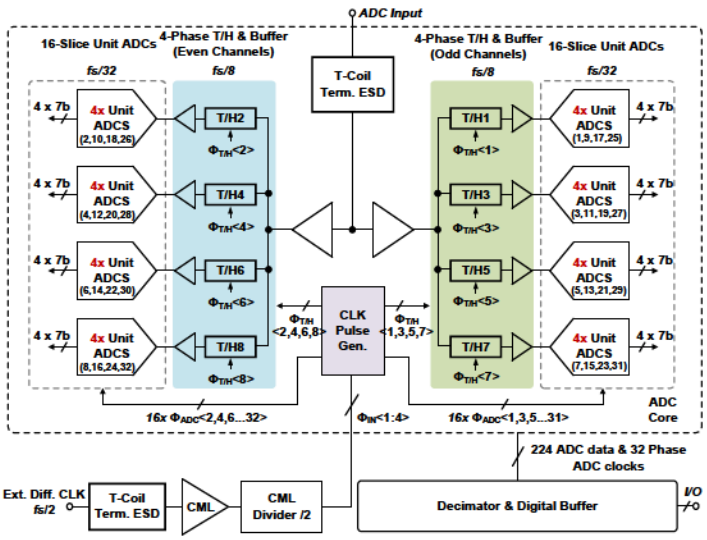

Fig. 1. 38GS/s 7-bit 32-way time-interleaved ADC architecture.

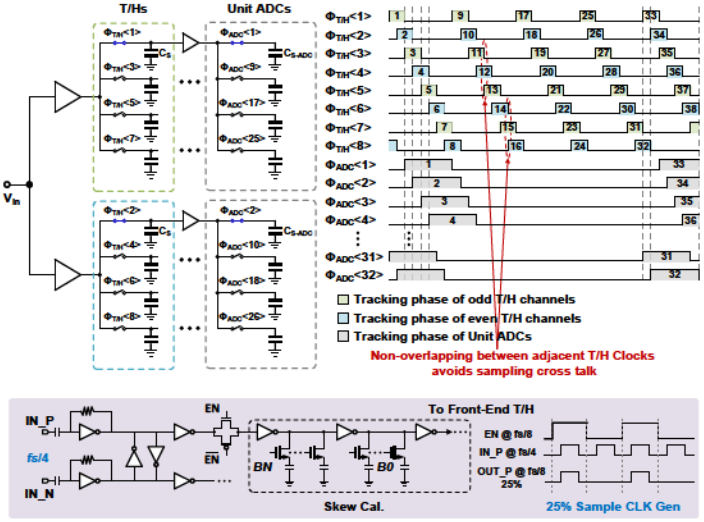

Fig. 2. Interleaver timing diagram and 25% duty cycle T/H clock generation circuit with skew calibration.

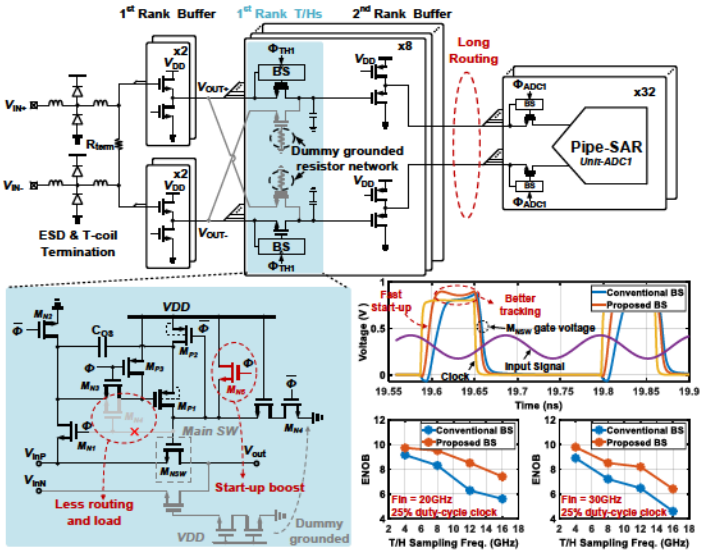

Fig. 3. Interleaver schematic, proposed speed enhanced bootstrapped switch, and post-layout simulation results.

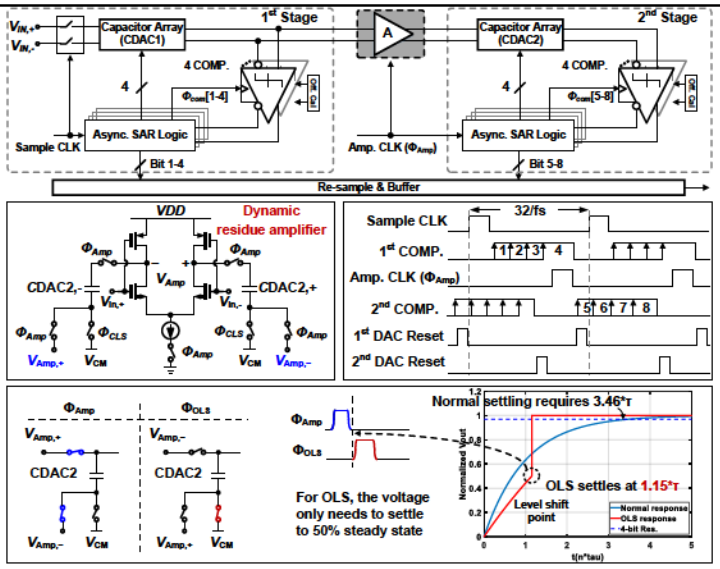

Fig. 4. Unit pipelined-SAR ADC block diagram, dynamic residue amplifier schematic, timing diagram, and OLS settling technique.

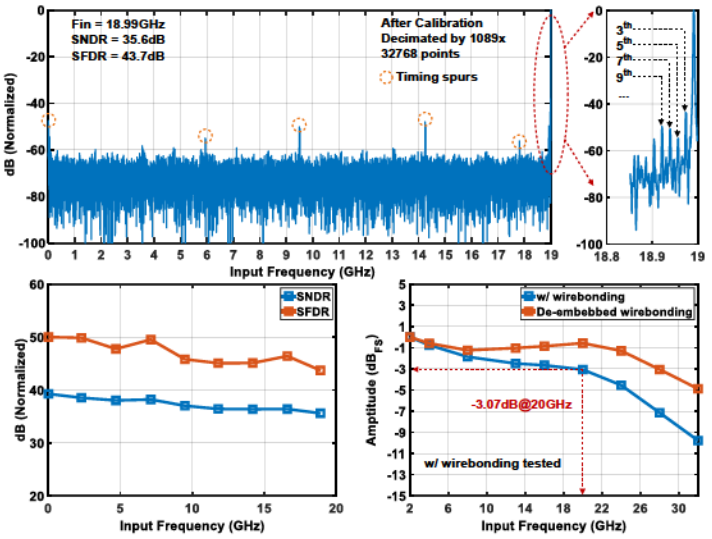

Fig. 5. ADC output DFT for Nyquist rate input, SNDR and SFDR vs input frequency, and input frequency response.

References	ISSCC'18 [2]	CICC'18 [3]	CICC'17 [5]	ISSCC'19 [6]	VLSI'16 [7]	This Work
Technology (nm)	14	28	28	7	16	**22**
ADCs/Interleaver Supply (V)	0.8/0.9	0.95/±0.9	0.95/0.95	0.9/0.9	0.9/0.9	**0.85/0.9**
Sampling Rate (GS/s)	72	56	28	30	28	**38**
Architecture	8b -TI-SAR	8b -TI-SAR	8b -TI-SAR	7b-TI-SAR	8b-TI-SAR	**7b -TI-Pipe-SAR**
3 dB Bandwidth (GHz)	21	31.5	NA	NA	NA	**20**
SNDR@$f_{in,low}$ (dB)	39.3	40.5	37	33	40.9	**39.26**
SNDR@$f_{in,Nyquist}$ (dB)	32.7 @27G	33	34	32 @14G	31.5	**35.6**
Total/Interleaver Power (mW)	235/77	702/291	165/NA	79.65/NA	280/NA	**119.7/37.05**
FoM@$f_{in,low}$ (fj/conv-step)	43	145	102	81.6	110.4	**41.9**
FoM@$f_{in,Nyquist}$ (fj/conv-step)	121	344	140	83.6	325.7	**64.05**
Area (mm^2)	0.15	0.878	0.24	0.078	NA	**0.107**

Fig. 6. Performance summary and comparison table.