Study of Nanowire-based Integrated Via Technology for CMOS Application in Millimeter-Wave Frequencies

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***Abstract*— This work shows a novel integrated via structure based on 1.2 µm thick copper nanowires for use in CMOS applications at millimeter-wave frequencies. Coplanar waveguide (CPW) lines are fabricated on a 5000 Ω-cm high resistivity silicon wafer and connected by nanowire vias that are grown in integrated anodized alumina oxide (AAO). The AAO layer is fabricated by anodizing an evaporated aluminum layer onto the silicon wafer. This co-integrated technology has 0.095 dB insertion loss for 0.3 mm long circuits with 2 vias at 40 GHz. The results are promising with estimated loss per via of approximately 0.0275 dB. The fabricated structure shows great performance agreement with its reference test circuits of similar length. The design comparisons of circuits with different via dimensions and positions show that the shorter via length, wider via width and placing the via on the CPW ground plane closer to the signal line provide better performance.**

***Index Terms*—CMOS, integrated circuit, millimeter-wave technology, nanowires.**

I. Introduction

FUTURE millimeter and submillimeter wave communication systems are the key enablers to internet of things technology, autonomous vehicles, and low-power cube-satellites. In these areas, the devices using 3D integrated circuits (ICs) can be a game changer. By using a 3D IC structure, the low cost and volume can be provided due to its compact feature. High speed signal and low power consumption can be achieved.

In IC circuits and systems, vias play a significant role providing high-density interconnections between active devices as well as being used in grounding, signal routing, and transitions from microstrip to coplanar waveguide (CPW). They provide less metal interconnection paths and therefore lower parasitic resistance and inductance [1], compared to conventional interconnect technology such as wire bonds.

However, as the communication frequency band expands progressively into millimeter and even submillimeter wave frequencies, higher skin depth loss and parasitic inductance for vias become prohibitive. To resolve these issues, different substrate materials are used to reduce the high frequency loss, such as high resistivity silicon (Si) wafers [2]-[3], glass [4] and commercial anodized alumina oxide (AAO) [5]. However, due to substrate thickness limitations, the via thickness for these technologies ranges from 50-250 µm. This range does not satisfy the need of small package size for a 3D IC/Si integration process [6] in CMOS applications, such as the CMOS imager sensor [7]. The required via thickness is in the range of 1-30 µm. Thus, a technique for fabricating and characterizing ultra-thin vias that are required by 3D CMOS applications is lacking.

Herein, we propose a novel integrated via structure in integrated AAO with copper (Cu) nanowires (NWs) onto a high resistivity Si wafer. CPW lines on high resistivity are used to evaluate the via loss and to minimize Si substrate loss from the via assessment. The proposed integrated structure provides low power loss due to the benefit of the substrate material and NW properties. NWs are easily penetrated by high frequency fields due to their nanometer size and therefore show less skin depth effect. By using bundles of NWs, total power loss can be decreased [5]. Also, by using integrated AAO, ultrathin via thickness can be provided and improved integration can be achieved. The following sections will present the NW via design, fabricated structure, measurement results and via loss analysis.

II. Via Design and Measurement

The via design is shown in Fig. 1. The NW vias are tested through CPW lines, shown in Fig. 1a. Two types of vias are designed. Type 1 has a via length (VL) of 90 µm and via widths (VW) on the signal line (S) and ground plane (G) of 80 µm and 390 µm, respectively. Type 2 designs have the same VW on S and G. The designed VL × VW dimensions have values of 30 µm × 70 µm, 90 µm × 30 µm, 90 µm × 70 µm and 150 µm × 30 µm, as summarized in Table I. The optimized via location on G is studied by comparing an offset value, Δx, of 0 and 130 µm,

This work was supported in part by Semiconductor Research Corporation (SRC) and the National Science Foundation (NSF) Award (01762884) with portions conducted in the Minnesota Nano Center, which is supported by the National Science Foundation through the National Nanotechnology Coordinated Infrastructure (NNCI) under Award Number ECCS-2025124.

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where 0 µm is located at the midpoint of the ground plane (Fig. 1b).

TABLE I
SUMMARY OF VIA DIMENSIONS

Type	VL (µm)	VW (µm)
1	90	S = 80 G = 390
2	30	S = G = 70
	90	S = G = 30
	90	S = G = 70
	150	S = G = 30

In Fig. 1b, a one-unit cell circuit possesses a Via-AAO-CPW section and two CPW feed lines (L2). The Via-AAO-CPW section is defined as two rectangular NW vias, two via to CPW transitions (T1) plus CPW below AAO section (L1). To further enhance the signal level of vias, a five-unit CPW circuit (Fig. 1c) is designed to include 5 Via-AAO-CPW sections for a total of 10 NW vias. The total lengths of the one-unit and five-unit circuits are defined as 2*L2+L1+2*VL+2*T1 and 2*L2+5*L1+4*L3+10*T1+10*VL, respectively. L1, L2, L3 and T1 are 100 µm, 470 µm, 100 µm and 10 µm, respectively.

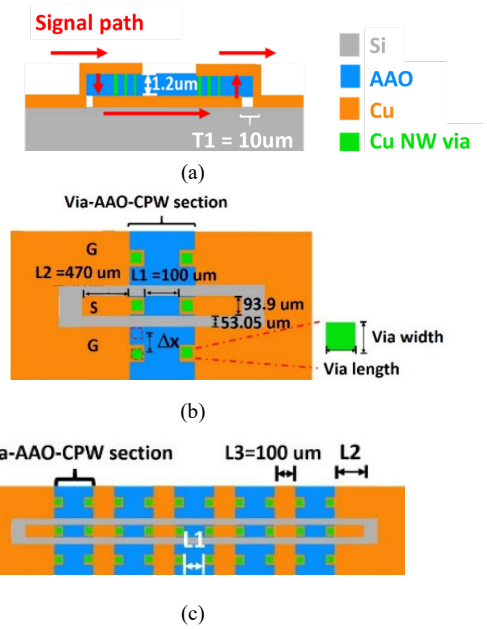

Fig. 1. Top view and cross section of via design in CPW circuit: (a) cross section of one-unit CPW with NW via; b) top view of one-unit CPW with NW via; c) five-unit CPW with NW via.

In this work, a CPW line is fabricated on a 500 µm thick 5000 Ω-cm resistivity Si wafer. The 1.2 µm AAO template is anodized from an evaporated aluminum (Al) layer that is pore widened to an average of 20 nm pore diameter and 9% porosity. Next, the Cu NWs are grown into the AAO template using an electrodeposition process [8]. The fabricated structure in Fig. 2 shows the Cu NWs in the patterned AAO region. The vias are created by connecting the NWs in pores to the top Cu layer.

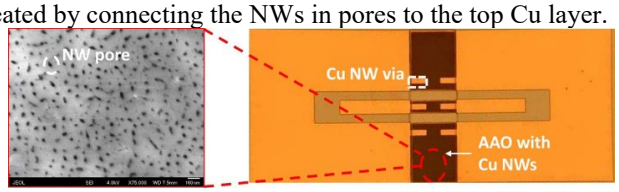

Fig. 2. SEM image of NW pore on AAO surface (left) and fabricated one-unit cell CPW with type 2 NW via (right).

The fabricated structures are characterized using an Anritsu 37369D VNA up to 40 GHz connected to a Cascade probe station RF-1. A 500 µm thick 5000 Ω-cm high resistivity Si wafer was placed between the measured sample and the metallic chuck for isolation. LRRM calibration is performed with Cascade ACP50 probes (pitch of 150 µm) and an ISS 101-190 calibration chip. The reference plane is the probe tip.

III. Results and Analysis

A. One-unit CPW with Cu NW vias

Fig. 3 shows a comparison between a one-unit CPW with type 1 NW via and a 1224 µm CPW line, used as the reference. The data of the CPW with type 1 NW via agrees well with the reference and even shows around 0.05 dB lower insertion loss at 25 GHz. This confirms the benefit of using Cu NW-based vias which provides similar performance to CPW lines.

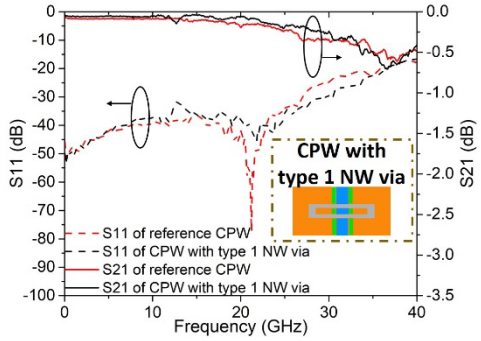

Fig. 3. Comparison of one-unit CPW with type 1 vias and 1224 µm reference line, where, VL= 90 µm, VW = 80 µm and 390 µm on S and G, respectively.

B. Five-unit CPW with Cu NW vias and via loss analysis

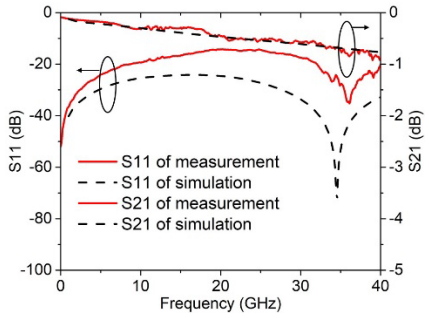

Fig. 4. Comparison of HFSS simulation and measurement results of five-unit CPW with type 2 NW vias. VL=30 µm, VW =70 µm and Δx =0 µm.

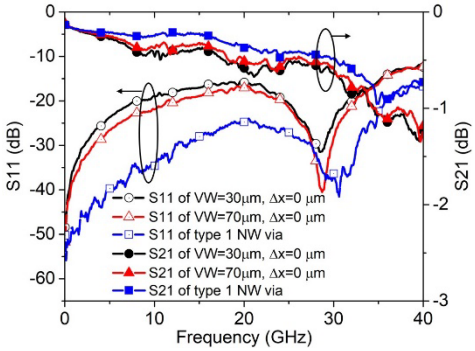

Fig. 5. Measured via width comparison of five-unit CPW with NW vias. For all three circuits, VL =90 µm, VW ranges from 30 µm to 390 µm.

Fig. 4 compares the HFSS simulation and measurement results. In simulation, due to high aspect ratio between the Cu NWs and CPW dimensions, the NW vias are represented by Cu

TABLE II
COMPARISON OF VIA TECHNOLOGIES FOR MILLIMETER-WAVE FREQUENCY RANGE

Ref.	Substrate (Type: Resistivity)	Insertion loss of one G-S-G via (dB)	Insertion loss of test line with two G-S-G vias at 40 GHz (dB)	Via size	Via Thickness (μm)	Line Length (mm)
[2]	Si: 5000 Ω·cm resistivity	0.53 at 75 GHz	0.93	Via diameter =42 μm	252	3.15
[3]	Si: High resistivity	0.03 at 40 GHz	~ 0.3	Via diameter =200 μm	100	2.7
[5]	AAO	0.035 at 40 GHz	~ 0.21	20×30 μm^2	50	0.200
This work	Si: 5000 Ω·cm resistivity (CPW) & AAO (via)	~ 0.0275 at 40 GHz	0.095 (Via-AAO-CPW section)	S: VL x VW = 90 μm×80 μm G: VL x VW = 90 μm×390 μm	1.2	0.300

pillars with 1.2 μm thickness, 5 μm×5 μm area and 9% porosity. The comparison shows that the measurement follows the simulation trend in S21 data. The measured S11 is worse than simulation which might be due to the fabrication defects, such as over etching.

Fig. 5 shows the via width comparison for CPW with vias. With the same VL of 90 μm, larger VW shows better insertion loss and reflection coefficient. CPW with type 1 NW via shows the best performance due to its widest VW on both S and G plane which provides more area for current to flow through.

In Fig. 6, the via length comparison is shown. Both circuits have VW of 30 μm. The circuits with VL of 150 μm show higher insertion loss compared to VL of 90 μm. This is because the longer VL introduces a longer signal path which results in higher insertion loss.

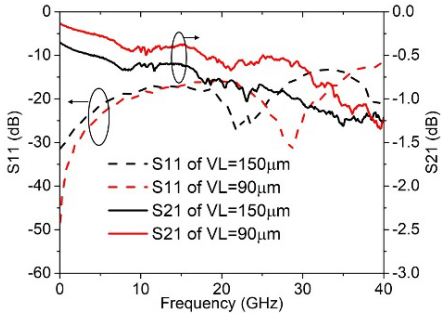

Fig. 6. Via length comparison of five-unit CPW with type 2 vias in measurement results. For both circuits, VW =30 μm, Δx =0 μm, VLs are 90 μm and 150 μm.

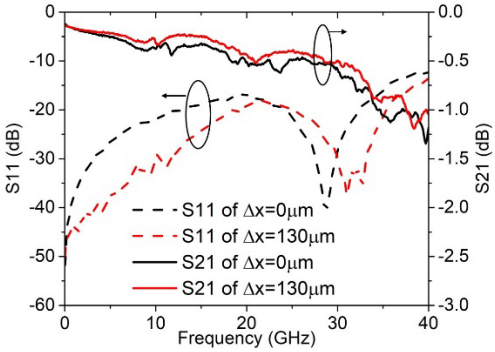

Fig. 7. Δx comparison of five-unit CPW with type 2 vias in measurement results. For both circuits, VW =70 μm, VL=90 μm. Δx is 0 μm and 130 μm.

Fig. 7 shows the comparison of via offset, Δx, relative to the midpoint in the ground plane width. Both circuits possess the same via size dimensions. From the measurement results, higher Δx shows better S21 data. Therefore, putting the via position on G closer to S provides better via performance.

In order to find the loss of Via-AAO-CPW section, the influences from other CPW line in the test circuits need to be removed. The five-unit CPW with vias includes two feed line (L2), four CPW sections (L3) and five Via-AAO-CPW sections. The loss of L2 and L3 sections can be measured and obtained from standard CPW lines. The insertion loss of 0.3 mm long Via-AAO-CPW section with type 1 vias can be calculated with the values of 0.043 at 20 GHz, 0.07 at 30 GHz and 0.095 at 40 GHz (in dB).

$$Loss = -10 * \log_{10}\left(\frac{|S_{21}|*|S_{12}|}{1-|S_{11}|*|S_{22}|}\right) \quad (1)$$

Next, to find the loss of a single G-S-G via, the loss of CPW below AAO section (L1) needs to be removed from the Via-AAO-CPW section. Two methods are available to remove the loss of L1 and approximate each via loss. The first assumes the loss of 100 μm CPW below AAO is equal to the 100 μm standard CPW without AAO and can be obtained from measurement. Using (1) [9], the attenuation loss can be obtained. The loss of a 100 μm standard CPW above Si wafer is 0.011 at 20 GHz, 0.018 at 30 GHz and 0.024 at 40 GHz (in dB). Therefore, each type 1 G-S-G via loss will be 0.016 at 20 GHz, 0.026 at 30 GHz and 0.035 at 40 GHz (in dB). The second method assumes the loss of CPW below AAO is represented by simulation results which is 0.024 at 20 GHz, 0.0379 at 30 GHz and 0.04 at 40 GHz (in dB). Then, each type 1 G-S-G via loss will be 0.0095 at 20 GHz, 0.016 at 30 GHz and 0.0275 at 40 GHz (in dB).

The comparison of type 1 via and other via technologies is shown in Table II. Compared to the other work, the via in this work is extremely thin. Considering the 50 μm via thickness in [5] and the circuit has 2 vias, the total signal path length is 0.3 mm which is very close to this work. The much lower insertion loss of the total signal line with via at 40 GHz ,0.095 dB, shows promise for the proposed via technology in this work.

IV. CONCLUSION

The work shows a novel integrated Cu NW via structure with 5000 Ω-cm resistivity Si wafer as CPW substrate and 1.2 μm AAO template anodized from evaporated Al for NWs growth. One-unit and five-unit circuits are designed, fabricated and tested. The one-unit CPW circuit with type 1 via shows a close S11 and S21 performance compared to its reference line. The measurement and simulation results of the five-unit circuit are compared. The comparison shows agreement for S21 data and worse performance for S11 data in measurement which might be due to fabrication defects. The CPW circuits with different via dimension, positions and types are compared. The via with shorter length, wider width, and larger Δx provides better performance. The type 1 via shows better performance compared to type 2 vias with the same via length. The analysis of via loss shows that the Via-AAO-CPW section with 0.3 mm length has 0.095 dB insertion loss and each type 1 via possesses around 0.0275 dB loss at 40 GHz.

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