An Inductor-First Single-Inductor Multiple-Output Hybrid DC-DC Converter With Integrated Flying Capacitor for SoC Applications

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***Abstract*—With the increasing complexity of highly integrated system on chips (SoCs), the power management system (PMS) is required to provide several power supplies efficiently for individual blocks. This paper presents a single-inductor multiple-output (SIMO) inductor-first hybrid converter that generates three outputs between 0.4V and 1.6V from a 1.8V input. The proposed multiple-output hybrid power stage can improve the conversion efficiency by reducing inductor current while extending the output voltage range compared with the existing hybrid topologies. In addition, the proposed converter employs an on-chip switched-capacitor power stage (SCPS) with a dual-switching frequency technique, resulting in a fast response time, low cross-regulation, and reduced number of on-chip pads. Measurement results show that the converter achieves a peak efficiency of 87.5% with the maximum output current of 450mA. The converter is integrated with a fast voltage regulation loop with 500MHz system clock to achieve a less than 0.01mA/mV cross-regulation and a maximum 20mV overshoot at full-load transient response. The design is fabricated in the standard 180nm CMOS technology.**

***Index Terms*—System-on-Chip, dc-dc converter, fast transient response, single-inductor multiple-output, hybrid buck converter, cross-regulation.**

I. Introduction

To maximize the performance of modern SoCs, it has become indispensable for the power management system (PMS) to provide scalable supply voltages [1], [2]. In a highly-integrated SoC, supply voltages are customized for individual points of load as illustrated in Fig.1(a). The PMS requires voltage regulators (VRs) with high power efficiency, high power density, precise point-of-load regulation, and fast voltage transition [1], [2]. The linear low-dropout regulators (LDOs) have limitation of conversion efficiency for wide output voltage range applications [3]–[6]. In contrast, switching regulators can achieve high power efficiency at the cost of a large passive area [7]–[9]. The switched-capacitor voltage regulators (SCVRs) have discrete numbers of voltage conversion ratios (CRs) and charge redistribution loss. However, high cap density in advanced technology makes it possible to implement converters with enhanced power density [10]–[15]. The switched-inductor voltage regulators (SIVRs) can achieve high efficiency over a wide output voltage range, but it also suffers low power density due to bulky inductor size [7], [8], [16]–[18].

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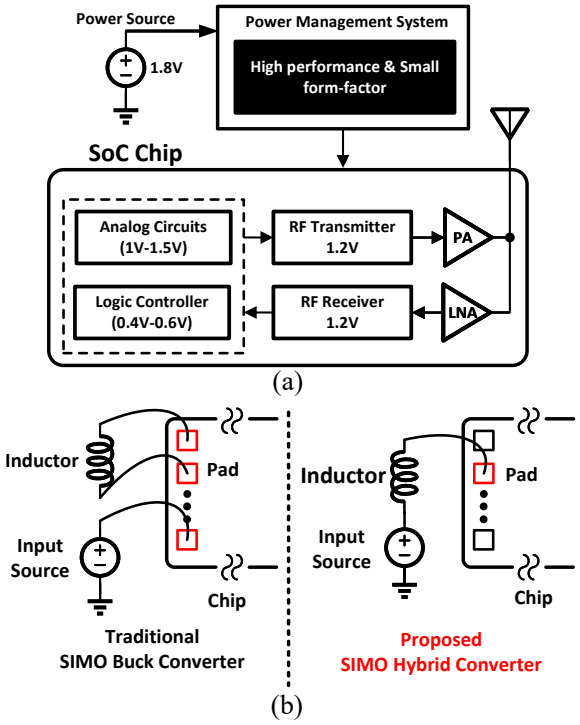


Fig. 1. (a) Block diagram of SoC applications, (b) comparison of chip packaging between conventional buck converter and inductor-first hybrid converter.

Recently, hybrid converters have captured keen attention as they incorporate the advantages of both SIVR and SCVR topologies. For example, 3-level converter [19], input-passive-stacked third-order buck converter [20], double step-down (DSD) converter [21] and flying-inductor hybrid converter [22] have shown the capability to generate a continuous output voltage range with good power efficiency. The 3-level and DSD converter reduce voltage stresses on the power switches and allow a higher switching frequency. However, they both suffer high inductor conduction loss. An inductor-first hybrid converter [23] has shown that by placing the inductor directly to the input power source, as shown in Fig.1(b), the converter offers better efficiency and higher power density due to the reduction of the inductor current. However, this inductor-first hybrid converter produces one output, requiring many individual single output converters for multiple loads.

As a result, single-inductor multiple-output (SIMO) dc–dc converters gain attraction since they are area and cost-effective

to provide multiple power supplies by requiring only one single off-chip inductor [24]–[36]. The conventional SIMO SIVRs suffer from high output voltage ripple and large cross-regulation. The SIMO converter presented in [37] shows the cross-regulation improvement by using a fast-response digital controller in the closed-loop regulation. However, slow switching frequency still requires the converter to use large output capacitors. The dual switching frequency converter presented in [38] improves both output voltage ripples and cross-regulation. Unfortunately, this technique needs additional power switches that switch at a very high frequency, sacrificing conversion efficiency. A SIMO converter with a hybrid power stage has also been extended for three outputs in [22], but only one of the outputs is tunable with the limited output voltage range of 1/3x to 1/2x of input voltages. The rest two outputs are regulated at 2x and 3x of the first output voltage, respectively. In SoCs, it is desired to implement multiple independent outputs. Besides, cross-regulation between outputs is still an issue for the multiple-output converters. Existing cross-regulation reduction techniques were incorporated in conventional buck converters [24]–[27]. However, for hybrid SIMO converters, cross-regulation and large overshoot/undershoot due to the load/line transition are still unsolved.

This paper presents a SIMO inductor-first hybrid voltage regulator to achieve a wide output voltage range, higher efficiency, lower cross regulation, and fast transient response. The proposed hybrid SIMO converter demonstrates following advantages:

1) The proposed SIMO hybrid structure extends output voltage conversion range to the full step-down range of 0x-1x.
2) The inductor-first power stage reduces the inductor conduction loss for better efficiency and minimize the number of on-chip pads for chip packaging.
3) The proposed feedback control methodology enhances the cross-regulation and transient response.

This paper is organized as follows. In the section II, the hybrid power stage and the operation of the SIMO converter are explained with the circuit schematic and timing diagram.

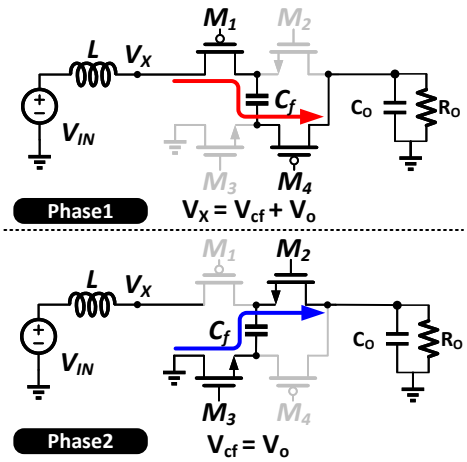


Fig. 2. Operation principle and charge flow of the proposed two-phase sub-SCPS.

Power loss analysis is presented in section III. Section IV presents the regulation methodology and implementation details. Measurement results from the fabricated chip are shown in section V. Finally, section VI concludes the paper.

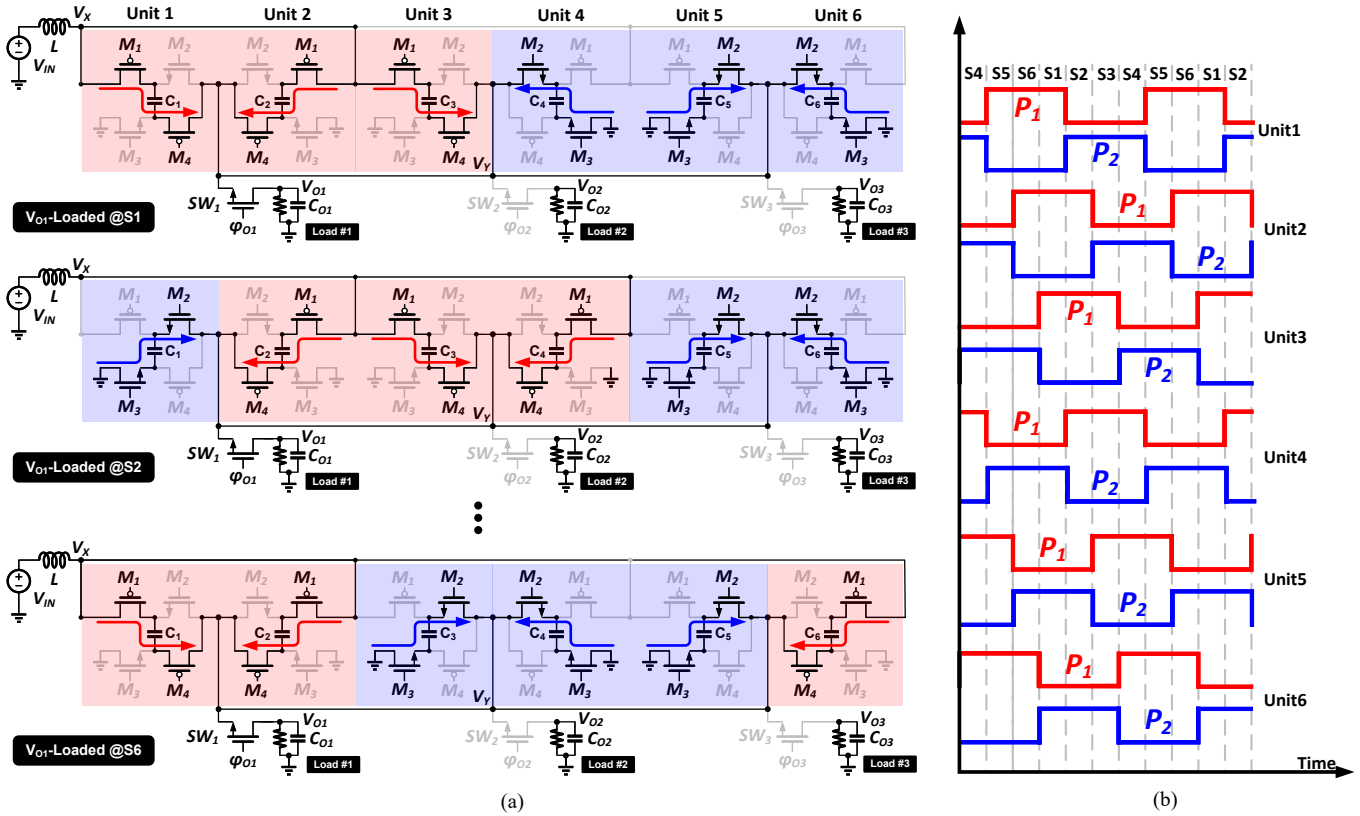
II. Power Stage Topology and Operation

The power stage of the proposed inductor-first hybrid converter consists of one power inductor L and one on-chip switched-capacitor power stage (SCPS). One terminal of the inductor is directly connected to the input power source and the other one is connected to the SCPS. With this inductor-first structure, the hybrid SIMO topology enhances the efficiency by reducing the inductor current [23]. The SCPS consists of six individual sub-SCPSs. Each sub-SCPS operates in a two-phase mode, as shown in Fig. 2. There are total four switches and one flying capacitor in a sub-SCPS. In phase 1, switches M_1 and M_4 are turned on. The flying-capacitor C_f is connected in series with the output capacitor to the inductor. In phase 2, switches M_2 andM_3 are turned on. The flying capacitor C_f is connected in parallel with the output capacitor, between output node V_O and the ground. As a result, the inductor current charges both V_O and C_O in phase 1, and C_f charges C_O in phase 2. The node voltage of V_X is boosted to V_{cf} + V_O in phase 1 and V_{cf} is regulated to V_O in phase 2.

The proposed SIMO hybrid power stage operates in two modes: the inductor current decreasing (ICD) mode and the inductor current increasing (ICI) mode. The inductor current is ramping down during the ICD mode and ramping up during the ICI mode. The power stage is switching between ICD and ICI mode alternately and periodically in the steady state. Fig. 3(a) presents an example of V_{O1}-loaded power stage configuration during the ICD mode. Corresponding timing of clock signals for the six sub-SCPSs is illustrated in Fig. 3(b). There are 6-state interleaved states, S_{1-6}, within a conversion cycle.

During state $S1$, the sub-SCPSs of unit1, 2 and 3 work at phase 1 mode and the sub-SCPSs of unit 4, 5 and 6 work at phase 2 mode. The flying capacitors C_1, C_2 and C_3 are connected in parallel between the node V_X and V_Y. The other flying capacitors, C_4, C_5 and C_6 are connected in parallel with the output capacitor C_{O1}, serving as on-chip output capacitors to reduce the output ripple and noise produced by the switching events and other parasitic. Thus, C_{4-6} are balanced to the output voltage of V_{O1}. The red curves show the current direction from the inductor to the output and the blue curves show the current direction of the on-chip flying capacitors charging the output.

During state S_2, the sub-SCPS of unit 4 is switched to phase 1 mode and the sub-SCPS of unit 1 is switched to phase 2 mode. Current flow is created from V_{IN} to V_{O1} via the flying capacitor C_4, and C_1 charges the output by arranging parallel connection with C_{O1}. For states S_{3-6}, the sub-SCPSs of unit 5,6,1,2 are switched to phase 1 mode and the sub-SCPS of unit 2,3,4,5 are switched to phase 2 mode, respectively.With the six interleaving states S_{1-6}, the node voltage of V_X in the ICD mode is maintained at $2V_{O1}$, allowing the inductor current to ramp down at a rate of:



(a) (b)

Fig. 3. (a) Power stage configuration of the proposed SIMO hybrid converter at inductor current decreasing (ICD) mode, (b) timing of clock signals for the six sub-SCPSs.

$$di_L/dt = (V_{IN} - 2V_{O1})/L \quad (1)$$

Fig. 4 shows the V_{O1}-loaded power stage configuration of the ICI mode. All sub-SCPSs work at phase 2 mode and do not switch during the ICI mode. Thus, all flying capacitors C_{1-6} are connected in parallel with the output capacitor C_{O1} to serve as the on-chip output decoupling capacitor. The inductor is connected between V_{IN} and V_{O1}, allowing the inductor current to ramp up at a rate of:

$$di_L/dt = (V_{IN} - V_{O1})/L \quad (2)$$

The inductor current can be regulated by adjusting the duty cycles of ICD and ICI modes to achieve the voltage-second balance in the steady-state. The energy can be delivered to the three outputs by turning on the three power-splitting switches SW_1, SW_2 and $SW_3$with the control signals of ϕ_{O1}, ϕ_{O2} and ϕ_{O3}.

It is noteworthy that the previous inductor-first hybrid converters have limited conversion ratio range of 0.5x-1x [23] or 1/3x-1/2x of one output level [22]. In these topologies, the power inductor is connected between the input source and an intermediate node with voltage V_{int} in the power stage. To ensure the proper operation, the power inductor needs to satisfy the voltage-second balance principle in the steady state. Hence, V_{int} must be higher than the input voltage V_{IN} during one phase in the two-phase operation structure, resulting in the limited conversion ratio. This reason requires the node V_X voltage be higher than V_{IN} in the ICD mode to overcome

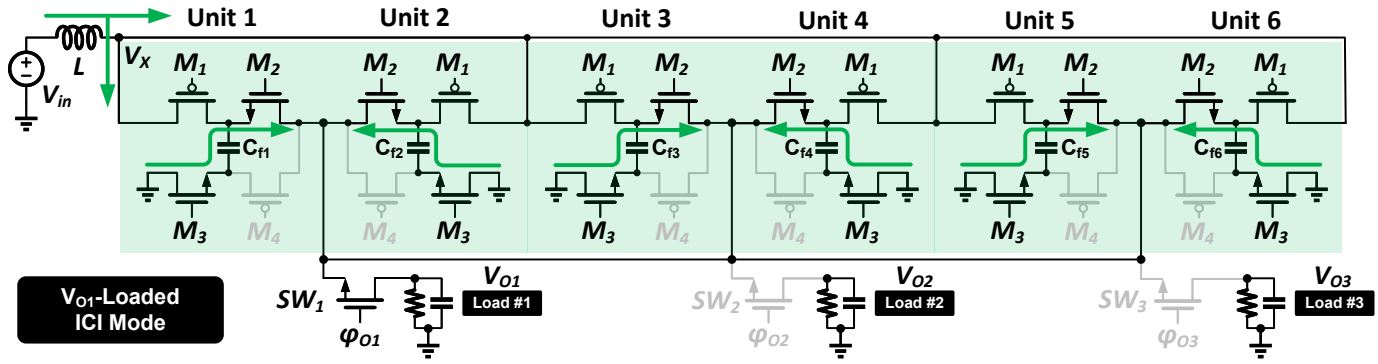


Fig. 4. Power stage configuration of the proposed SIMO hybrid converter at inductor current increasing (ICI) mode.

conversion ratio limitation: extending conversion ratio can be achieved by forcing one of the outputs to be regulated higher than $0.5V_{IN}$. For example, if $V_{O3} > 0.5V_{IN}$, the voltage difference across the inductor shows a negative value of $V_{IN} - 2V_{O3}$ to guarantee the correct ICD mode. There's no voltage level requirement for node V_{O1} and V_{O2} since all output voltages are lower than input voltage guaranteeing correct ICI mode. Thus, the proposed inductor-first hybrid power stage successfully extends the conversion ratio to 0x-1x of V_{IN} in the ideal case. The conversion ratio of the fabricated chip is determined considering multiple factors such as switching frequency, delay of controller, etc.

III. Power Stage Loss Analysis

A power loss analysis in DC-DC converters is important to get a design guidance of the converter's implementation. In this section, we analyze main loss components and derive output impedance of the proposed converter by using an ideal transformer model of a DC-DC converter [39]. In this model, the output impedance Z_O represents the conduction losses of the converter and can be estimated as

$$Z_O = \sqrt{{Z_{SSL}}^2 + {Z_{FSL}}^2} \tag{3}$$

where Z_{SSL} is the slow-switching limit (SSL) impedance and Z_{FSL} is the fast-switching limit (FSL) impedance. Z_{SSL} is related to the charge redistribution losses of capacitors in the converter and Z_{FSL} is related to the conduction loss due to the resistive elements in the converter. Switching losses of the switch gate charge or switching node capacitance can also be added with the conduction losses to estimate the overall power loss or power efficiency.

A. SSL Impedance

As described in Section II, one of the outputs should be higher than 1/2x of input voltage for the proposed converter to be regulated. To facilitate the Z_{SSL} analysis, it is assumed that V_{O3} is higher than 1/2x of input voltage and all flying capacitance values, C_{1-6}, are the same. As shown in Fig. 4, in the ICI mode, all the flying capacitors in the SCPS are configured as by-pass capacitors of the outputs. Thus, there is no loss contribution from Z_{SSL} caused by reconfiguration of SCPS in the ICI mode.

During the ICD mode, the flying capacitors in the SCPS are charging and discharging to transfer power to the output with power loss. As shown in Fig. 3, red and blue arrows represent charge flows in the power stage at each switching phase. Based on the charge flow and the assumption of the same flying capacitances, Z_{SSL} can be estimated as follows:

$$Z_{SSL} = \sum\nolimits_{i\in caps} \sum\nolimits_{j\in phases} \frac{\left(a_{c,i}^{j}\right)^2}{2C_i f_{sw}} \tag{4}$$

where $a_{c,i}^{j}$ is the charge multiplier, which is flowing through flying capacitors i, j is the state of the SCPS during ICD mode, C_i is the capacitance of a flying capacitor, and f_{sw} is the switching frequency of the power stage. Since the SCPS can be seen as a 6-state interleaved two-phase 2:1 SCVR and the inductor behaves as a current source, based on (4),

$$\begin{aligned} Z_{SSL} = &\frac{\left(a_{c,1}^{5\to1}\right)^2}{2C_1 f_{sw}} + \frac{\left(a_{c,1}^{2\to4}\right)^2}{2C_1 f_{sw}} + \frac{\left(a_{c,2}^{6\to2}\right)^2}{2C_2 f_{sw}} + \frac{\left(a_{c,2}^{3\to5}\right)^2}{2C_2 f_{sw}} \\ &\cdots + \frac{\left(a_{c,6}^{4\to6}\right)^2}{2C_6 f_{sw}} + \frac{\left(a_{c,6}^{1\to3}\right)^2}{2C_6 f_{sw}} \end{aligned} \tag{5}$$

where $a_{c,k}^{i\to j}$ indicates the charge multiplier of the flying capacitor k from state i to j as each sub-SCPS is operating in two-phase.

However,it can be seen that the flying capacitors are soft-charged with the current flow (red) from the inductor and hard-discharged with the current flow (blue) to the output as illustrated in Fig. 3. Thus, there is no charge redistribution loss associated with C_1 in state $S_{1,5,6}$, C_2 in state $S_{1,2,6}$, C_3 in state $S_{1,2,3}$, C_4 in state $S_{2,3,4}$, C_5 in state $S_{3,4,5}$ and C_6 in state $S_{4,5,6}$. This results in the Z_{SSL} is reduced to

$$Z_{SSL} = \frac{\left(a_{c,1}^{2\to4}\right)^2}{2C_1 f_{sw}} + \frac{\left(a_{c,2}^{3\to5}\right)^2}{2C_2 f_{sw}} \cdots + \frac{\left(a_{c,6}^{1\to3}\right)^2}{2C_6 f_{sw}} \tag{6}$$

By using the Kirchhoff's Current Law (KCL) and the constraint of steady state assuring that the incoming and outgoing charges through each flying capacitor should be equal in one full switching period [40], the charge multiplier of a single-flying capacitor two-phase 2:1 SCVR is $\frac{1}{2}$. Thus the charge multiplier of the 6-state interleaved SCPS can be determined as

$$a_{c,k}^{i\to j} = \frac{1}{12} \tag{7}$$

With the following assumption:

$$C_1 = C_2 = C_3 = C_4 = C_5 = C_6 = \frac{1}{6} C_{F,TOT} \tag{8}$$

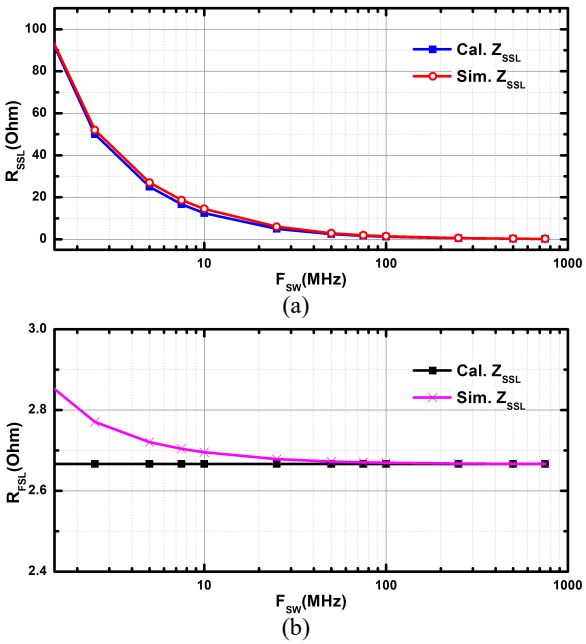


Fig. 5. Comparison between simulation and analytic results of (a) Z_{SSL} and (b) Z_{FSL} impedance. The two results are closed matched.

where $C_{F,TOT}$ is the total flying capacitor value. Plugging the values of $a_{c,k}^{i\to j}$ from (7) and capacitor values from (8) to (6), the Z_{SSL} is determined as

$$Z_{SSL} = \frac{1}{8C_{F,TOT}f_{sw}} \tag{9}$$

Note that C_{1-6} are regulated to V_{O1}, V_{O2} or V_{O3} during V_{O1}-loaded, V_{O2}-loaded or V_{O3}-loaded conditions, respectively. Since the output voltages of V_{O1-3} are normally regulated at different voltage levels, the flying capacitors will be hard-charged/discharged when the SCPS is switched to charge a different output. This charge redistribution loss associated with this transition can be estimated as

$$\begin{aligned} P_{loss,SSL2} = &\sum\nolimits_{ij\in SCPS_{V_{Oi}\to V_{Oj}}} \frac{1}{2}C_{F,TOT} \\ &* \left(V_{Oi} - V_{Oj}\right)^2 f_{ij} \end{aligned} \tag{10}$$

where f_{ij} indicates the frequency of the transition that the SCPS is switched to charging V_{Oj} from charging V_{Oi}. The power loss due to this transition is highly depending on the specifications of the desired output voltage levels and load current conditions. For example, in the case of $V_{O3} > 0.5V_{IN} > V_{O1,O2}$ and $I_{O3} >> I_{O1,O2}$, this charge redistribution loss is negligible.

B. FSL Impedance

As previously mentioned, FSL impedance is related to the conduction loss due to the resistive elements, such as turn-on resistance of switch and ESR of capacitor, in the power stage. In this analysis, we only account the loss contribution from the turn-on resistance of switches. There are FSL power losses from both the ICI and ICD modes in this hybrid converter.
For the FSL conduction loss in the ICI mode, there are only switch conduction losses from switches M_1 and M_2 and the power splitting switches SW_{1-3}. The V_{Oi}-loaded FSL impedance in the ICI mode, $Z_{FSL,V_{Oi},ICI}$, can be simply estimated as follows:

$$\begin{aligned} Z_{FSL,V_{O1,ICI}} &= R_{on,SW_1} + \frac{1}{6}(R_{on,M_1} + R_{on,M_2}) \\ Z_{FSL,V_{O2,ICI}} &= R_{on,SW_2} + \frac{1}{6}(R_{on,M_1} + R_{on,M_2}) \\ Z_{FSL,V_{O3,ICI}} &= R_{on,SW_3} + \frac{1}{6}(R_{on,M_1} + R_{on,M_2}) \end{aligned} \tag{11}$$

where R_{on,SW_i} is the turn-on resistance of the power splitting switch and R_{on,M_i} is the turn-on resistance of the M_1 and M_2 switches in the SCPS. Note that for any output regulated lower than $0.5V_{IN}$, that output will be charged only in the ICI mode. Hence only $Z_{FSL,V_{Oi},ICI}$ is contributed by that specific output.

In the ICD mode, since there is current flow through the switches in the SCPS, V_{Oi}-loaded conduction loss in the ICD mode $P_{cond,V_{Oi},ICD}$ can be estimated as follows:

$$\begin{aligned} P_{cond,V_{Oi},ICD} = &\sum_{k\in switches}\sum_{j\in phases} R_{on,M}\left(I_{ICD,M}^{j}\right)^2 \\ &+ R_{on,SW_i}I_{Oi}^2 \\ P_{cond,V_{Oi},ICD} = &R_{on,M_1}\begin{pmatrix}\left(I_{ICD,M_1}^{1\to3}\right)^2 + \left(I_{ICD,M_1}^{2\to4}\right)^2 \\ + \cdots + \left(I_{ICD,M_1}^{6\to2}\right)^2\end{pmatrix} \\ &+R_{on,M_2}\begin{pmatrix}\left(I_{ICD,M_2}^{1\to3}\right)^2 + \left(I_{ICD,M_2}^{2\to4}\right)^2 \\ + \cdots + \left(I_{ICD,M_2}^{6\to2}\right)^2\end{pmatrix} \\ &+\cdots+R_{on,M_4}\begin{pmatrix}\left(I_{ICD,M_4}^{1\to3}\right)^2 + \left(I_{ICD,M_4}^{2\to4}\right)^2 \\ + \cdots + \left(I_{ICD,M_4}^{6\to2}\right)^2\end{pmatrix} \\ &+R_{on,SW_i}I_{Oi}^2 \end{aligned} \tag{12}$$

where $I_{ICD,M}^{i\to j}$ is the RMS value of current flowing through the turn-on switch M in the SCPS from state i to j in the ICD mode, with the SCPS modeled as 6 two-phase SCVRs. $R_{on,M}$ is the turn-on resistances of the switches in the SCPS, M_{1-4} and I_{Oi} is the output current of V_{Oi}. As pointed out in [40], $I_{ICD,M}^{i\to j}$ can be derived with the charge multiplier in (7),

$$\left(I_{ICD,M}^{i\to j}\right)^2 = D_{i\to j}\left(\frac{a_{c,k}^{i\to j}I_O}{D_{i\to j}}\right)^2 = \frac{1}{72}{I_O}^2 \tag{13}$$

where $D_{i\to j}$ is the ratio of the time duration from state i to j per switching period, which is 0.5. Therefore, V_{Oi}-loaded FSL impedance $Z_{FSL,V_{Oi,ICD}}$ in the ICD mode can be determined as follows:

$$\begin{aligned} Z_{FSL,V_{Oi,ICD}} = &\frac{1}{12}(R_{on,M_1} + R_{on,M_2} + R_{on,M_3} + R_{on,M_4}) \\ &+ R_{on,SW_i} \end{aligned} \tag{14}$$

The calculated impedances of the proposed converter under different switching frequency, f_{sw}, were verified and compared with the simulation in Fig. 5. For the simplicity, the simulation was made under the following conditions: 1V of input voltage, 1nF of C_1 to C_6, and 0.3, 0.5, 0.7 V of V_{O1}, V_{O2}, V_{O3}, respectively. Moreover, each turn-on resistance is set to 2Ohm. The simulated and calculated results match with minimal error. The small differences are caused by non-ideal switches in Fig. 5(a) and non-zero charge transfer loss in Fig. 5(b).

C. Inductor DCR Loss

The inductor conduction loss $P_{loss,L}$ contributed by the inductor DC resistance (R_L) can be estimated

$$P_{loss,L} = \left(I_L\right)^2 R_L \tag{15}$$

where I_L is the inductor RMS current.

The DC-DC converter can be modeled as an ideal transformer whose turns ratio is equal to the ideal conversion ratio of the converter. With the inductor directly connected

to the input power source, the ideal input current I_{IN} can be approximated as

$$I_{IN} = I_L = \frac{I_{O1}V_{O1} + I_{O2}V_{O2} + I_{O3}V_{O3}}{V_{IN}} \quad (16)$$

Compared with the conventional buck, 3-level and DSD typologies that have $I_L = I_{O1} + I_{O2} + I_{O3}$, this proposed hybrid converter reduces the inductor current proportional to the step-down conversion ratios of the outputs to decrease the inductor conduction loss.

IV. Implementation Details

A. Feedback Controller

Fig. 6 shows a block diagram of the proposed converter. The feedback controller consists of output voltage sensing stage, VCO clock generator, mode selector of power stage, switch signal generator, dead-time generator, level shifter and power MOSFET driver. The converter uses comparator-based voltage-mode control to generate the pulse width modulation (PWM) signals for regulating the output voltages.

The output voltage detector is illustrated in Fig. 7(a), consisting of two feedback resistors, R_{F1} and R_{F2}, and one low power clock comparator for each output. The comparator is driven by a 500MHz system clock to enable fast dynamic response to the load/line transition. The 500MHz system clock is generated from a voltage-controlled oscillator (VCO) with 378uW power consumption. Error signals, a, b, and c, generated from the comparators are fed into a finite state machine (FSM) that generates power stage mode signal (ICI or ICD) and power splitting control signals. Error signals, a, b, and c, are 0 when V_{O1}, V_{O2}, and V_{O3} are lower than the reference voltages, V_{ref1}, V_{ref2}, and V_{ref3}, respectively. Fig. 7(b) illustrates the flow chart of the proposed controller. When the code abc turns to '000', the power stage is switched to ICI mode; when the code abc turns to '111', the power stage is switched to ICD mode. The power stage will not change the operation mode if abc changes to other codes.

The FSM also generates signals for the three power splitting switches, SW_{1-3}. SW_{1-3} are controlled in descending order from V_{O1} to V_{O3} in order to share the current of the inductor in ICI mode and the SCPS in ICD mode. FSM state diagram in Fig. 8(a) presents the states of ICD, ICI mode and the power splitting signals versus the error signal code abc. For example, when the error signal a is low, V_{O1} is charged regardless of the states of b and c: the gate driver signal ϕ_{O1} is high to turn on the power switch M_{O1}. When the error signal a is high and b is low, V_{O2} is charged regardless of the states of c. Otherwise, V_{O3} is charged. Fig. 8(b) shows an example of the inductor current waveform and the corresponding timings of the power splitting control signals, ϕ_{O1}, ϕ_{O2} and ϕ_{O3}, and the error signals, a, b and c. The slew rate equations of the inductor current in both ICI and ICD modes are also presented. Since output will be charged only in ICI mode when the output is regulated below $0.5V_{IN}$, the controller will force the power stage to skip charging the output in ICD mode. The power stage will charge the next output by the controller. For example, when the error signals a and b are low in ICD mode with V_{O1} regulated at $0.3V_{IN}$ and V_{O2} at $0.8V_{IN}$, V_{O2} instead of V_{O1} will be charged.

During the ICD mode, the SCPS is switching in 6-state interleaved phases with the 500MHz system clock. Thus, each sub-SCPS is switching around 83MHz. This switching frequency is chosen by considering the trade-off between impedance loss and switching loss of the SCPS. This switching frequency can efficiently generate the output power with a total of 2.3nF on-chip flying-capacitor implemented using metal-insulator-metal (MIM) capacitor. The circuit implementation of key digital blocks is illustrated in Fig. 9.

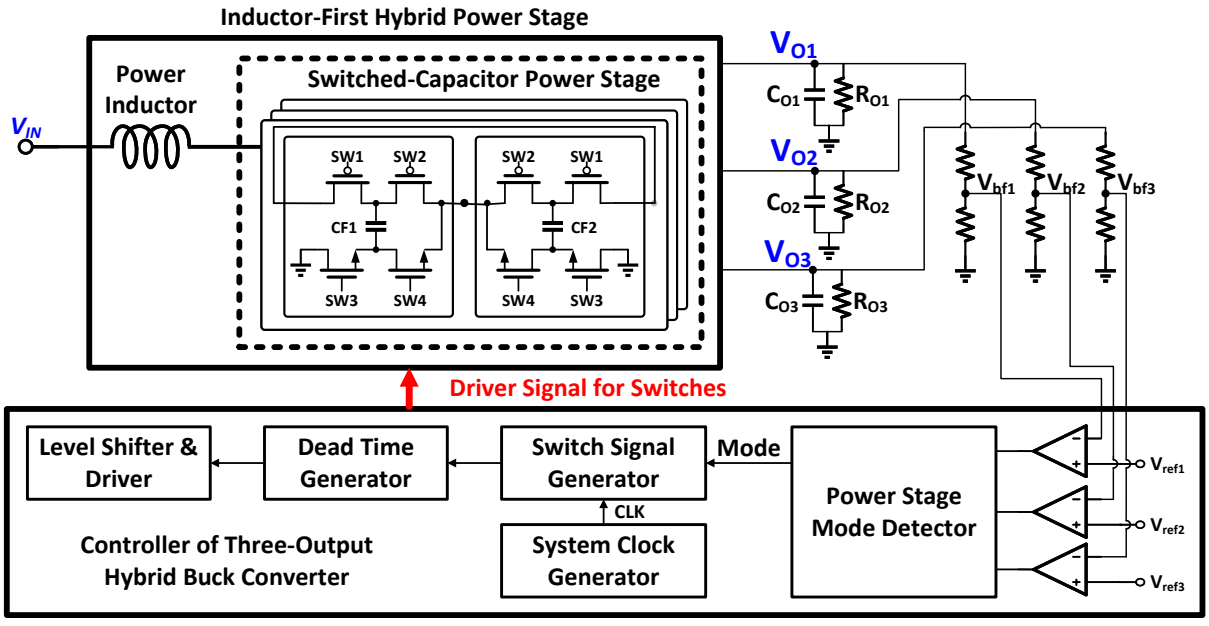


Fig. 6. System-level overall block diagram of proposed SIMO hybrid buck converter.

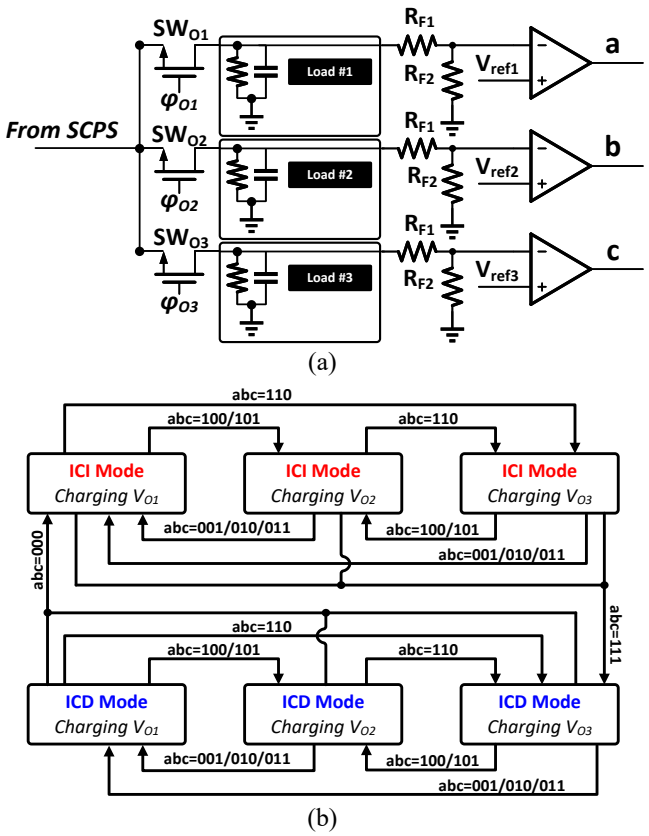


Fig. 7. (a) Output voltage sensing stage, (b) flow chart of the proposed feedback controller.

B. Fast Transient Response and Efficiency Enhancement

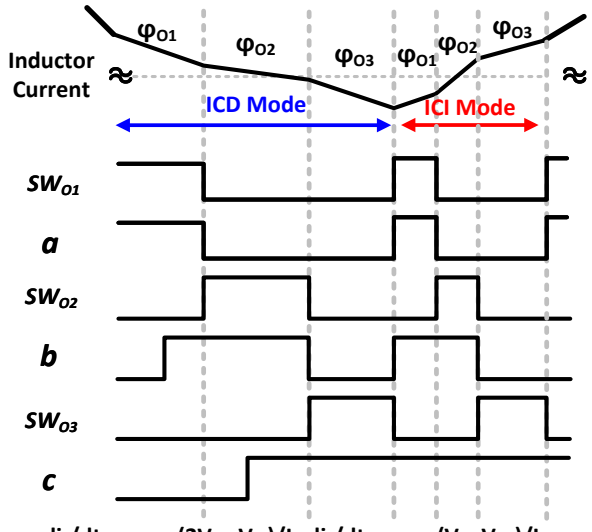
In this SIMO hybrid converter implementation, the flying capacitor is designed with a limited value considering chip size and power density. Coincidentally, the on-chip flying capacitor can enhance the efficiency and response speed as shown in Fig. 10(a). In state 1 of the ICD mode, the flying capacitor C_1 in the first sub-SCPS is connected in series with the output capacitor and charged by the inductor current. The voltage of C_1,C_2 and C_3 (in state 1, these flying capacitors are connected in parallel) is charged up to 2.3V since flying capacitor size is around 100x smaller than output capacitor size. In the next state, the C_1 will deliver the energy to the output capacitor and be discharged to the output voltage, while C_4 in the fourth SCPC will be charged around 2.3V. Thus, during this period, V_X will be boosted around 3.8V. The high V_X voltage helps a faster ramping down of the inductor current. This fast ramping down causes the duty-cycle of ICD mode to be much shorter than that of the ICI mode. To avoid over-voltage stress, a 3.3V thick-oxide MOSFET is used for M_1 and M_2 in the SCPCs.

Fig. 10(b) illustrates the simulated waveforms of inductor current, node voltage of V_X and top-plate voltage of C_1 during one period of ICD and ICI cycle. The time of one period is 1.3us, while the duty cycle of ICD mode is 14%. It is because the node voltage V_X is charged to a high value (peak of 3.8V) when the inductor current is relatively high (>230mA in this case). This phenomenon vanishes when the inductor current ramps down to a low current (<230mA in this case). In this

abc	ICD	ICI	SW_{O1}	SW_{O2}	SW_{O3}
000	0	1	1	0	0
001	*hold*	*hold*	1	0	0
010	*hold*	*hold*	1	0	0
011	*hold*	*hold*	1	0	0
100	*hold*	*hold*	0	1	0
101	*hold*	*hold*	0	1	0
110	*hold*	*hold*	0	0	1
111	1	0	0	0	1

a=0/1 → $V_{O1}<V_{ref1}$ / $V_{O1}>V_{ref1}$
b=0/1 → $V_{O2}<V_{ref2}$ / $V_{O2}>V_{ref2}$
c=0/1 → $V_{O3}<V_{ref3}$ / $V_{O3}>V_{ref3}$

(a)



(b)

Fig. 8. (a) FSM diagram of the ICD, ICI and output charging states, (b) waveform and slew rate of inductor current with error signals and power splitting signals in descending order.

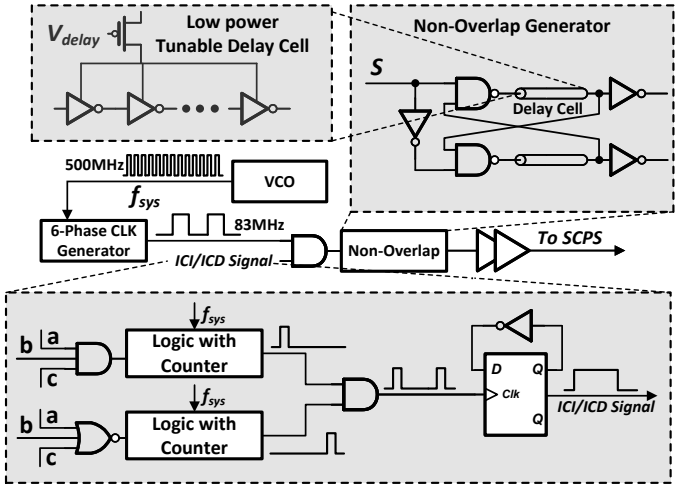


Fig. 9. Circuit implementation of key digital control blocks.

design, the SCPC is switching at a high frequency in ICD

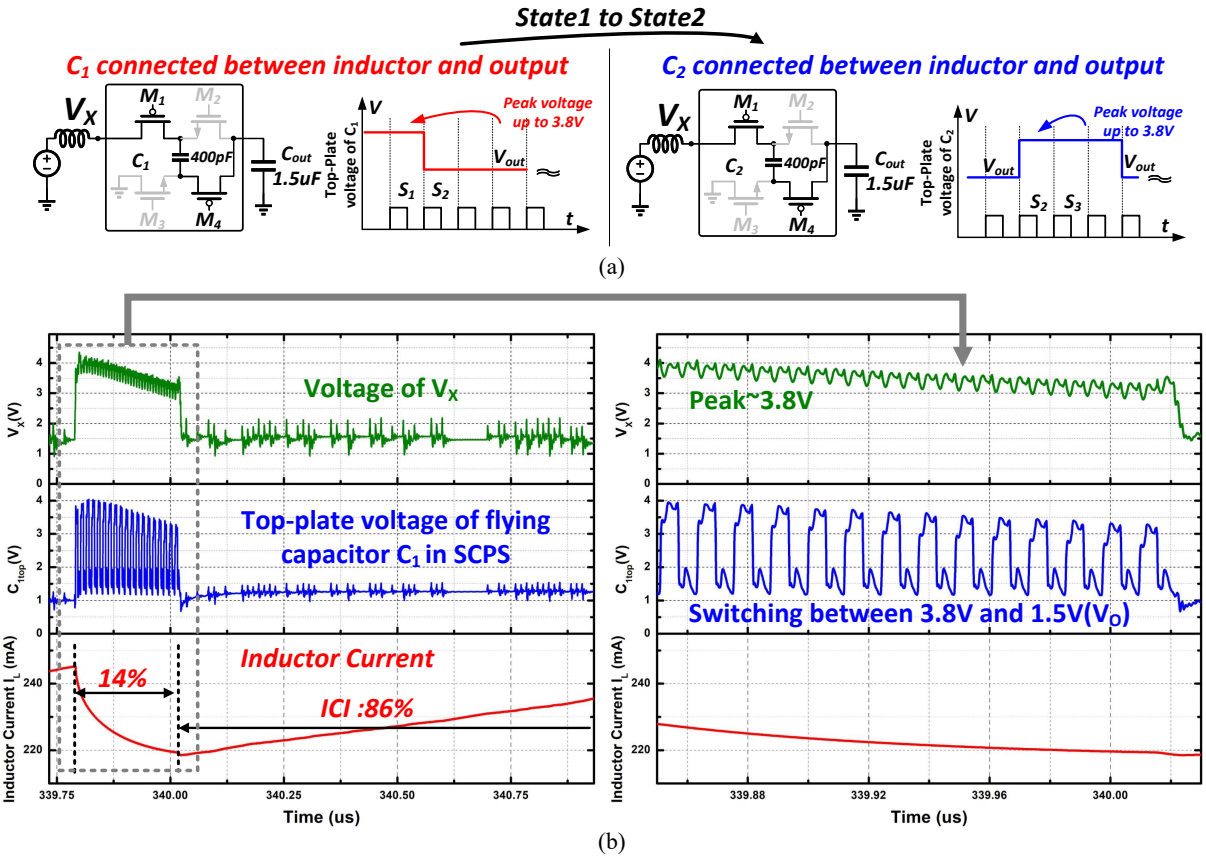


Fig. 10. (a) Over-voltage charging timing diagrams and a node voltage waveform of the SIMO hybrid at ICD mode for fast response and enhanced efficiency, (b) simulated waveforms of node voltage V_X, top-plate voltage of flying capacitor C_1 and inductor current I_L.

mode and not switching in ICI mode. Consequently, the short duty cycle of ICD mode significantly reduces switching loss of the proposed hybrid converter, without compromising line regulation performance. It is also noteworthy that the hard-charging happens only in the ICD mode. Furthermore, it helps to enhances the response speed when the converter switches from high load to low load condition due to large voltage across the inductor.

C. Gate Driver Implementation

Fig. 11 shows energy-area efficient driver and power switches. High-side power switches in the SCPS require additional gate driver voltages that do not exceed the device gate oxide breakdown voltage. A dynamic bootstrap scheme is employed to power up the M_1 and M_2. The gate driver signal is switched between V_X and V_O during the ICD mode with V_X=2V_O. Supply voltage of the level shifter is boosted to V_X with a local bootstrap capacitor C_{BST}. C_{BST} is implemented using MOS capacitor of high cap-density to save silicon area. Simulated waveform of V_X in steady-state is illustrated in Fig. 11 (c). During the ICI mode, the gate driver signal is switched between V_{IN} and Gnd. In fact, M_1 and M_2 in all the sub-SCPSs turn off during the ICI mode. The C_{BST} is charged to V_{IN} while the level shifter acts as normal driver. The latch-based level-shifter is implemented using a cross-coupled inverter to ensure the fast rail-to-rail swing for level shifter outputs. Tunable delay cells are also added in the signal paths to minimize signal skew between different signal paths of driver. For switches M_3 and M_4, conventional drivers are implemented under 1.8V input voltage.

D. Cross-Regulation

The regulation of the converter includes inductor current regulation and output voltage regulation. The output voltage is precisely regulated by high-speed high-precision comparator with 500MHz clock and the inductor current is regulated with the error signal code abc. Cross-regulation is minimized since the output voltage and inductor current are independently regulated while regulation accuracy and speed of each output voltage are ensured by the comparator.

V. Measurement Results

To demonstrate the performance of the SIMO hybrid converter, the converter is implemented in TSMC 180nm conventional CMOS technology. The fabricated chip integrates power switches, gate drivers, flying capacitors and control blocks. Fig. 12 shows the fabricated die micrograph with the size of 1.955 mm^2 excluding PADs. Fig.13 illustrates the measurement set-up and lab measurement environment to evaluate the performance of the converter. PCB test board with wirebonding is implemented carefully to reduce power paths, maintain low loss from the chip to PCB power traces and minimize the parasitic effects. An off-chip pre-charging method is implemented on the testing board for start-up. The

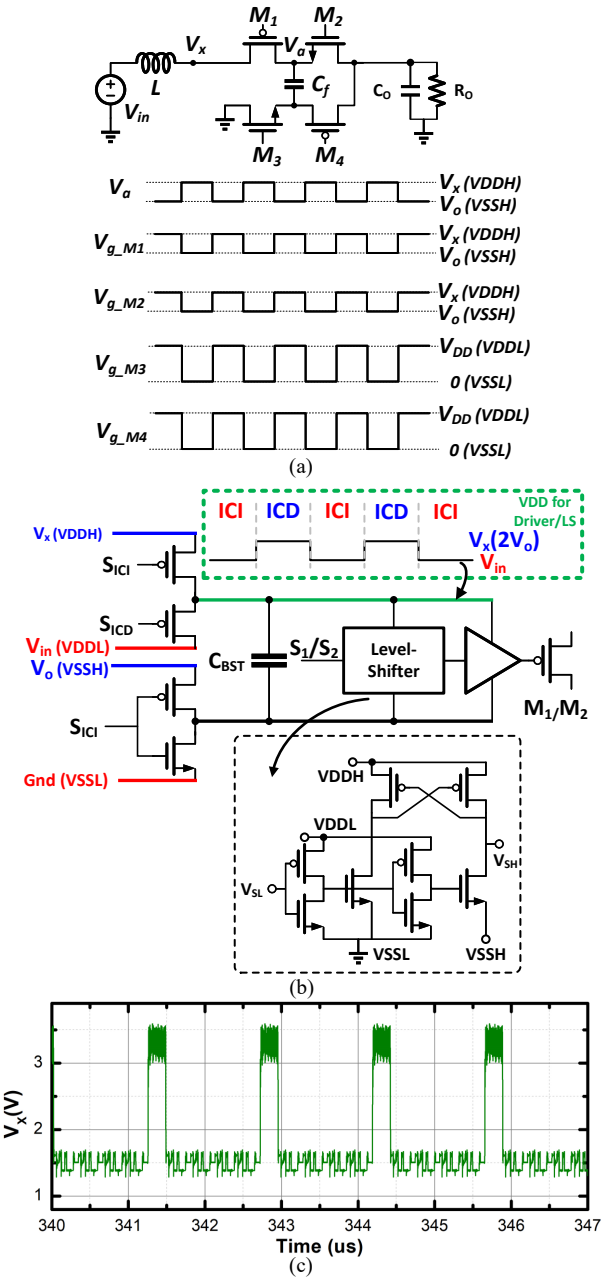


Fig. 11. (a) Gate drive voltages of switches in SCPS, (b) Circuit implementation of energy-area efficient driver and level shifter and (c) simulated waveform of V_X in steady-state with parastics included.

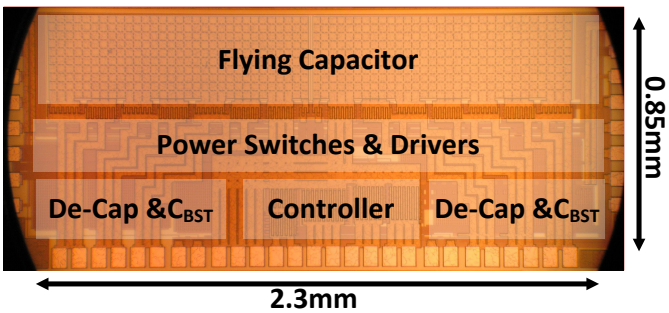
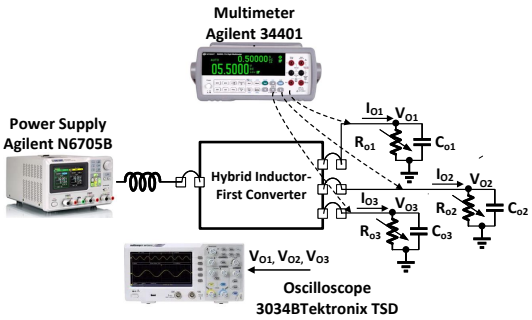
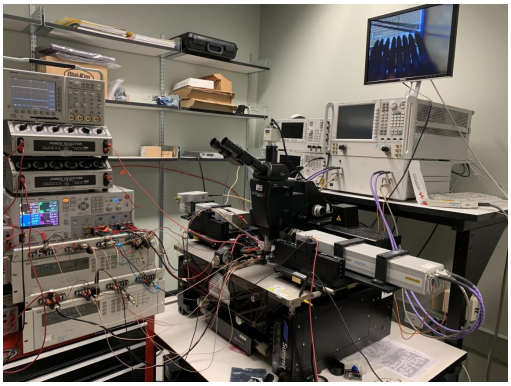


Fig. 12. Fabricated chip micrograph of the proposed converter (0.85mm x 2.3mm excluding pads).

outputs and flying capacitors are pre-charged to 1.5V. This pre-charge method prevents the inductor current ramping up to a very high value to avoid damage of the chip during the start up period. With the 1.8V input voltage, all the devices are operating under safe region lower than the breakdown voltage level. A discrete 4.7μH inductor with 26mOhm DCR is used. Two 1.5μF and one 3μF reverse geometry capacitors with low equivalent series resistance (ESR) are used as output capacitors, C_{O1}, C_{O2} and C_{O3}, respectively. C_{O3} is chosen with a larger capacitor value so that no free-wheeling switch is required with the reduced time duration of ICD mode. Due to the proposed inductor-first SIMO structure, the number of wirebonding is significantly reduced. The prototype operates with an 1.8 V input voltage and generates three regulated outputs from 0.4 to 1.6 V.

Fig.14 demonstrates the close-loop load transient response, under the condition of V_{O1}=1.1V, 1.3V and 1.5V. In this measurement, two of the outputs are loaded with fixed 70mA (half load) while one output steps between 10mA and 150mA with 20ns edge-time, which is very-light load and full load conditions. The settling time is 40μs with undershoot of 140mV and observed cross-regulation of 0.29mV/mA at the rising edge of I_{O1} transition. The worst cross regulation is observed when I_{O1} varies. The 34 mV and 44mV undershoots of V_{O2} and V_{O3} are observed at the rising edge of I_{O1} transition, which is caused by the intrinsic characteristic of the feedback controller. Since the three outputs are charged in the order from V_{O1} to V_{O3} to share the inductor current as explained in Section IV, the V_{O2} and V_{O3} will be charged after the recovery of V_{O1} and V_{O3} starts to recover after V_{O2}'s





(b)

Fig. 13. (a) Measurement setup, (b) lab measurement environment.

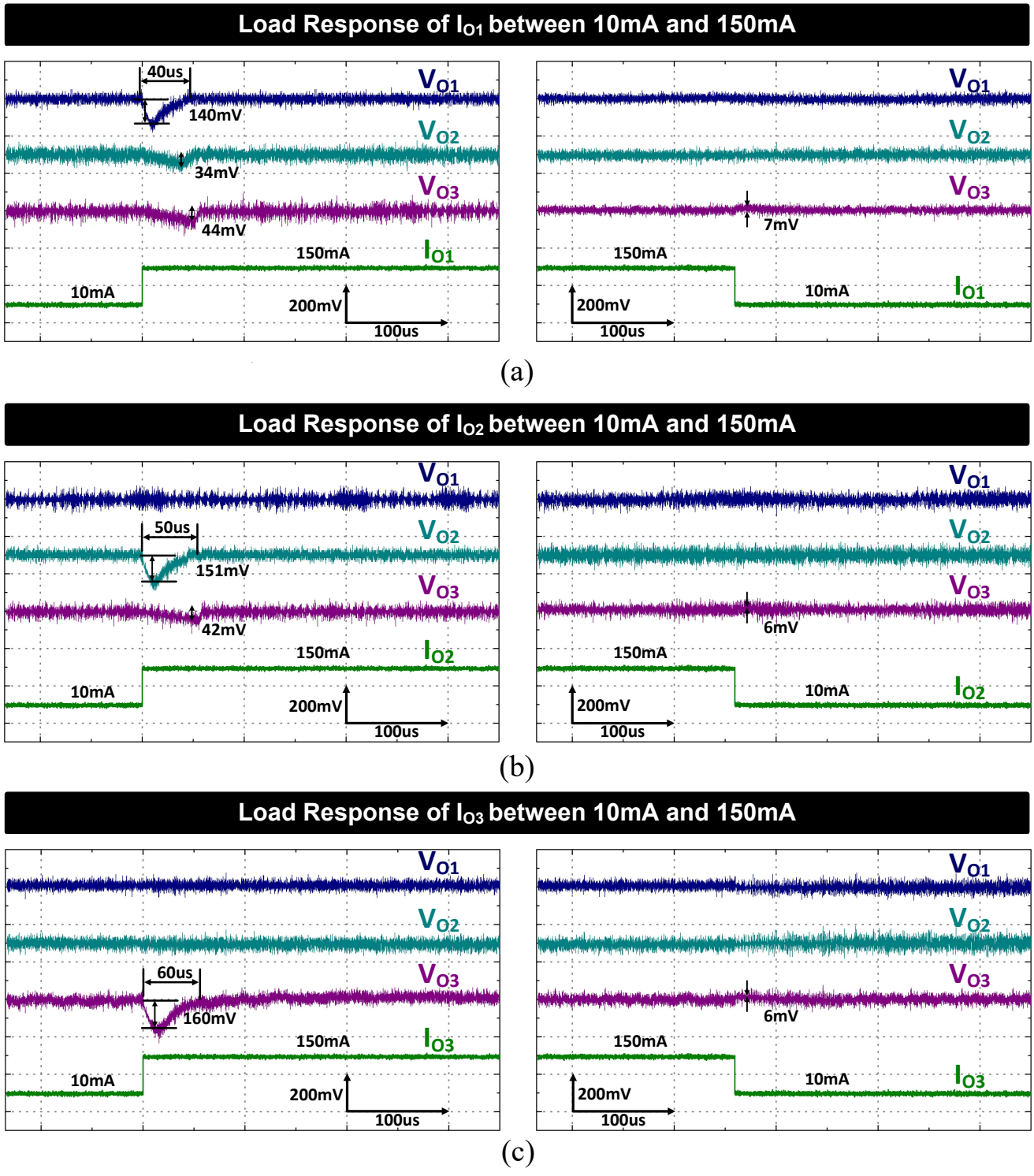


Fig. 14. Measured load transient response with 20ns load current edge-time at V_{O1}=1.1V, V_{O2}=1.3V and V_{O3}=1.5V: (a) I_{O1} transient between 10mA and 150mA with I_{O2}=I_{O3}=70mA, (b) I_{O2} transient between 10mA and 150mA with I_{O1}=I_{O3}=70mA, and (c) I_{O3} transient between 10mA and 150mA with I_{O1}=I_{O2}=70mA.

settled down. For the load current transition of I_{O2}, V_{O1} is charged first and V_{O3} will be charged after the recovery of V_{O2}. Hence, there is only a 42mV undershoot at V_{O3}. For the load current transition of I_{O3}, there will be no undershoot for V_{O1} and V_{O2} since V_{O1} and V_{O2} have higher charging priority to V_{O3}. As shown in Fig. 14(c), the best performance of cross-regulation, which is not observable (<0.001mV/mA), is measured at the rising edge of I_{O3} transition with a settling time of 60μs and undershoot of 160mV. It is worth noting that at the falling edge of all cases, no cross-regulation are observed with overshoot of less than 7mV and response time of less than 2μs, which is expected due to comparator-based

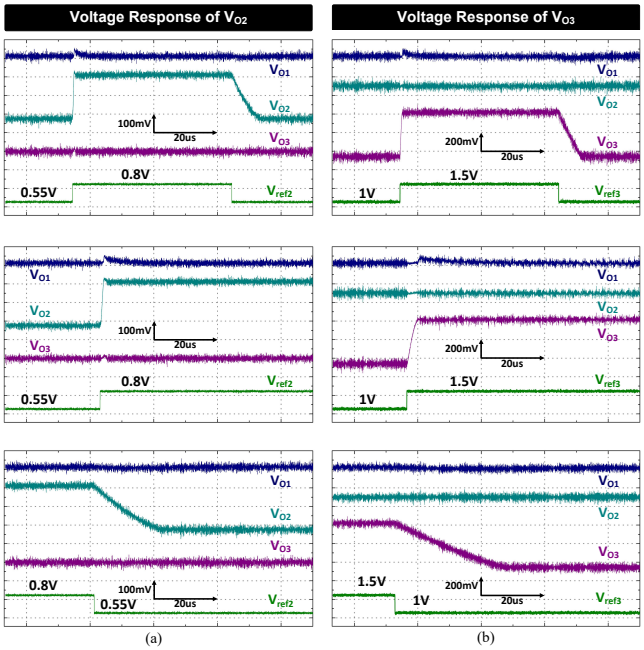


Fig. 15. Measured voltage transient response of (a) V_{O2} changes between 0.55V and 0.8V with V_{O1}=0.6V, V_{O3}=1.5V with the zoomed in waveforms, (b) V_{O3} changes between 1.1V and 1.5V with V_{O1}=0.6V, V_{O2}=0.8V with the zoomed in waveforms.

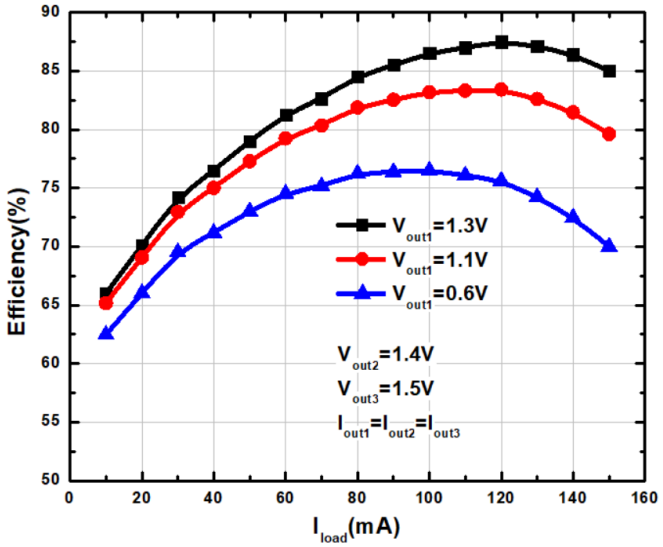


Fig. 16. Measured efficiency of the proposed SIMO converter.

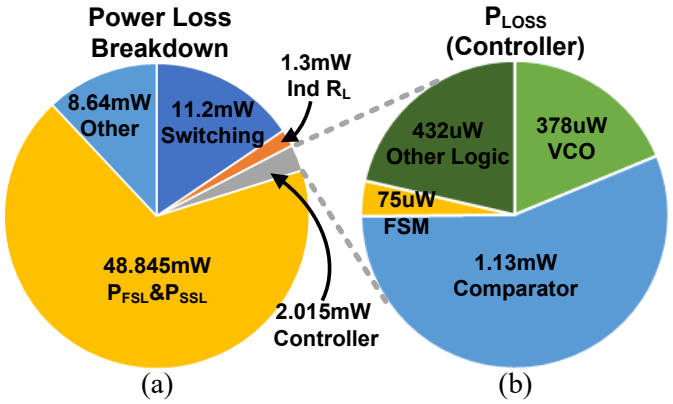


Fig. 17. Estimated power loss breakdown at peak efficiency point: (a) total power loss, (b) controller loss.

power splitting, high frequency system clock and fast inductor current ramping down with the on-chip SCPS.

Fig. 15(a) shows voltage transient response when the reference voltage of V_{O2} changes between 0.55V and 0.8V with V_{O1}=0.6V, V_{O3}=1.5V and Fig. 15(b) shows voltage transient response when V_{O3} switches between 1.1V and 1.5V with V_{O1}=0.6V and V_{O2}=0.8V. It shows that a less than 60μs of settling time with no overshoot and cross regulation at falling edge, and an 8us of settling time with no overshoot and cross regulation at rising edge.

Fig. 16 presents the measured power efficiency versus the load current I_{load} and V_{O1} under input voltage of 1.8V. The X axis indicates the value of the load current at each output under I_{O1}=I_{O2}=I_{O3}. The three curves show the power efficiency at V_{O1}=0.6V, 1.1V and 1.3V with V_{O2}=1.4 and V_{O3}=1.5V. The peak efficiency is 87.5% at I_{O1}= I_{O2}=I_{O3}=120mA (I_{total}=360mA) with V_{O1}=1.3V. The efficiency degrades at low load since the duty cycle of the ICD mode increases, resulting in higher switching loss. The efficiency at high load degrades due to a higher conduction loss. Fig. 17(a) shows a simulated power loss breakdown at the peak efficiency point. The Z_{FSL} and Z_{SSL} power losses account for 67% of the total power loss. The portion of the switching loss approximates 15% of the total power loss. The detailed power loss breakdown of the controller is also illustrated in Fig. 17(b).

Table I shows a summary of performance of the proposed converter and comparisons with state-of-the-art SIMO converters. The proposed inductor-first hybrid converter can achieve a better efficiency compared with both conventional and hybrid SIMO converters in [24], [25], [36], [37]. Unlike previous inductor-first hybrid topology in [22], the proposed hybrid power stage extends the conversion ratio and supports a much higher switching frequency with on-chip flying capacitor to achieves up to 250 times faster response speed. Our SIMO converter shows a significantly better cross-regulation suppression than the low-frequency SIMOs such as [22], [25], [36], [37] under load transition between very light load and full load condition. Moreover, a 13.5% efficiency improvement is achieved compared with the high frequency design in [24] since the switching loss of SCPS is minimized. The inductor-first structure also reduces the inductor conduction loss and excludes the requirement for the free-wheeling switch, resulting in boosting conversion efficiency and saving chip area. Compared with conventional SIMO topology in [25], the proposed hybrid converter reduces the required output capacitor that targets a similar current per load. Finally, It also has an enhanced falling load transient response due to the inductor current ramping down speed.

VI. Conclusion

This paper presents a SIMO hybrid converter for SoC applications that delivers independent supply power to each output channel. The architecture and circuit implementation details are discussed. This design incorporates an on-chip SCPS-based inductor-first hybrid power stage to achieve higher efficiency without compromising the output voltage conversion ratio and

TABLE I. PEFROMANCE COMPARISON OF SIMO CONVERTERS

		[25] ISSCC 2012	[36] TPE 2018	[24] JSSCC 2016	[22] JSSCC 2019	[37] JSSCC 2022	***This Work***
Process		65nm	180nm	65nm	130nm	65nm	***180nm***
Topology		Conventional SIMO	Conventional SIMO	Conventional SIMO	Hybrid SIMO	Conventional SIMO	***Hybrid SIMO***
Supply Voltage (V)		3.4-4.3	3.3-4.0	1.6-2.0	9.0	1.8	***1.8***
# of Outputs		5	5	4	2	4	***3***
Output Voltage Range (V)		1.2-2.8	0.9-2.2	0.4-1.4	3-4.2, 6-8.4	0.6-1	***0.4– 1.6***
Switching Frequency (MHz)		1.2	1	20MHz/100MHz	1.8-2.3	NA	***500MHz (system)***
Load Regulation Methods		AERC	OVACC	Dual-frequency PWM	PWM	PWM	***PWM***
Total Off-chip Ind. (uH)		2.2	4.7	2x0.2 (dual inductor)	1/0.522	10	***4.7***
Output Cap. (uF)		5x4.7	5x10	0.01	30, 48	4x1	***1.5, 1.5, 3***
Flying Cap. (nF)		NA	NA	NA	13200, 52000 (off-chip)	NA	***2.3 (on-chip)***
Max Load Current (mA)		1150	2310*	1000	3400	210*	***450***
Max Output Power (mW)		2232	2280	1200	12200	210*	***720***
Load Transient Response (20ns edge-time)	**Load Step (mA)**	50-200 (light-full)	250-500 (half-full)	125-250 (half-full)	500-1500 (light-full)	16	***10-150 (very light-full)***
	Cross Regulation (mV/mA)	0.067	0.016-0.035	<0.001	NA	0.42*	***<0.001 (best)-0.29(worst)***
	Settling Time (us)	100*(rising)/ 85*(falling)	60	0.08	300*(rising)/ 500*(falling)	4*	***40-60(rising)/ 2(falling)***
Area (mm^2)		1.86	5.52	10.8	7.37	4.95	***1.95***
Eff. @ Max Power (%)		NA	84	N/A	90	NA	***83.5***
Peak Eff. (%)		83.1	86	74	93.4	84.11	***87.5***

*Estimation from reported measurement.

reduce the number of on-chip pads for packaging. The fully-integrated SCPS results in a smaller form factor to compensate for the cost and volume overheads. The proposed feedback controller with a 500MHz system clock ensures the response speed and cross-regulation behavior. A fast inductor current ramping down speed in the ICD mode further improves the response while maintains the efficiency at a relatively high value. Finally, the proposed converter has been fabricated in a conventional 180nm CMOS process and the performance is verified with measurement results.

ACKNOWLEDGMENTS

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