Perspectives on spintronics technology development: Giant magnetoresistance to spin transfer torque magnetic random access memory

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ABSTRACT

The discovery of the giant magnetoresistance (GMR) effect in 1988 started a new field called spintronics and was recognized with the 2007 Nobel Prize in Physics, which was awarded to Fert and Grunberg. Spintronics is based on the contribution of both electron spin and electron charges of materials to facilitate electronic functions, enabling one extra degree of freedom for device operations. Spintronics has grown rapidly during the past three decades with significant discoveries, technological advancements, and material and device developments that have led to numerous product applications. Furthermore, new research fields and technology areas have been discovered and continue to expand. In this Perspective, key technological advances in the field during the past three decades will be highlighted, starting with the developments that led to the first use of the GMR effect in hard disk drives and its impact in the spintronic ecosystem to currently used perpendicular magnetic tunnel junctions (pMTJs) for spin transfer torque magnetic random access memory (STT-MRAM) devices. The important aspects of the pMTJ characteristics for the application of STT-MRAM will be discussed. This Perspective will present perspectives on a new structure that enhances the efficiency of the pMTJ-based STT-MRAM and research directions that can drive further advances in spintronics.

INTRODUCTION

Discoveries in magnetism and magnetic materials have driven enormous advances in information storage technology and digital information storage density.[1–8] The corollary is also true: advances in industry have enabled more sophisticated devices and material structures that challenge our understanding of the underlying physics. In this Perspective, we highlight this productive interplay between magnetism research and its applications and provide our views on present research developments that can have a technological impact.

We begin with the discovery of giant magnetoresistance (GMR) in 1988,[9,10] the observation that the resistance of a magnetic/nonmagnetic metallic multilayer is a strong function of the magnetization alignment of the layers. As magnetoresistive effects [the relatively small anisotropic magnetoresistance (AMR)[11]] were already being used to read magnetic information on hard disk drives (HDDs),[2] it was quickly recognized that GMR structures could significantly enhance the read signal and, hence, HDD memory capacity. This discovery, thus, started a worldwide effort to develop the technology of highly sensitive GMR read sensors for HDD applications. As a result, after the discovery of GMR, research and development in the spintronic field was largely carried out by HDD magnetic head industry.

While the first spintronic applications were in HDD industry in the 1990s, spintronics started impacting the semiconductor industry in the early 2000s. The key advance was in tunnel magnetoresistance (TMR), an effect in magnetic tunnel junctions, two magnetic electrodes separated by a thin insulating tunnel barrier. The initial observation of TMR was in the 1970s[12] and early 1980s[13]—with

the effects being small and occurring at low temperature (4 K). However, in 1995, two groups—one at MIT[14] and the other at Tohoku University[15]—independently showed ~20% TMR with an AlO_x barrier at room temperature. This discovery enabled a solid-state memory technology and eventually the first magnetoresistance random access memory devices. Two further advances have been game-changers, significantly increasing the operation speed and density of solid state magnetic memory devices: (1) the prediction[16] and discovery of even larger TMR in junctions with crystalline MgO barriers[17,18] and (2) the theoretical prediction and discovery of spin-transfer torques,[19–21] which we will discuss in more detail below.

We start with an overview of GMR and the developments from its discovery to the first commercial products. We then discuss TMR and the advances that have brought us present day spin-transfer torque magnetic random access memory (MRAM). The last section, Future Spintronics, discusses perspectives on advancing the field and promising directions.

GMR TECHNOLOGY DEVELOPMENT; FOUNDATIONS OF SPINTRONICS ECOSYSTEM

In the GMR structure, it was discovered that the resistivity of a multilayer structure changed significantly depending on the magnetic orientation of the layers that were separated by non-magnetic metal layers.[9,10] The resistance when the magnetic layers were magnetized in a parallel direction was much lower than that in antiparallel configuration. The resistance change due to changes in magnetization orientation is called magnetoresistance (MR) ratio and is given by

$$\%MR = (R_{high} - R_{low})/R_{low}. \quad (1)$$

For GMR magnetic multilayers, the change in resistance is called giant magnetoresistance (GMR) because of its large value relative to anisotropic magnetoresistance (AMR) and orbital effects associated with changes in electron trajectories due to the Lorentz force. High GMR values ignited broad research and development efforts for new materials, multilayer structures, and deposition techniques, aiming to exploit the GMR effect that could be mass produced for HDD products.

Original GMR multilayer structures required relatively large magnetic fields (>25 mT)[9,10] to switch the magnetization of the layers from an anti-parallel to a parallel orientation. This magnetic field requirement had to be lowered significantly for product application. In 1990, a new structure called a "spin valve" was discovered at IBM[22] that operated at much smaller fields. In this structure, the magnetization of one of the layers was fixed with an antiferromagnetic layer, while the magnetization of the second layer was free to rotate with the application of small magnetic fields. These two magnetic layers were separated with a thin Cu layer. The necessary magnetic field to switch the free layer was on the order of only fractions of a mT (<0.1 mT), which could easily be supplied by a written bit on a magnetic disk.

The discovery of the spin-valve structure (which is also often referred to simply as a GMR structure) in 1990 provided the pathway to utilize the GMR effect for HDD applications. However, the ecosystem to deposit such structures for product applications was not sufficient. Spin-valve structures were significantly different from the previous AMR technology, for the first time below atomic level thickness control, sharp interfaces, very high-quality thin film depositions down to 2 Å, and new materials, which were all essential to make GMR read sensors for HDDs.

Over the next several years, the materials and technologies were developed, and a sufficient ecosystem was established. Following the discovery of the spin-valve structure, two more critical challenges had to be overcome to make the GMR sensor ready for first mass production. The first challenge was to form a pinned layer that was stable against temperature and magnetic fields in an HDD product environment. The original spin-valve structure used FeMn,[22] which was practically the only available anti-ferromagnetic (AFM) material at that time that could pin the magnetization of the fixed layer. This AFM material had room temperature characteristics sufficient for demonstrating the concept but did not have a high enough blocking temperature[23] or magnetic anisotropy at operating temperature to fix the magnetization of the pinned layer for HDD use. The second challenge was to be able to deposit very high quality thin film layers with angstrom level thickness accuracy and high quality multilayers with sharp interfaces. The available conventional sputter processing tools did not have sufficient complexity and, as a result, were marginal for such demanding thin film depositions for product applications.

The first challenge was addressed with the use of a "synthetic anti-ferromagnet" (SAF)[24,25] structure combined with a reactively sputtered NiO AFM material.[26] A SAF has two ferromagnetic layers that are strongly coupled antiferromagnetically through a metallic spacer by Ruderman–Kittel–Kasuya–Yosida (RKKY) interactions.[27] An applied field only couples weakly to a SAF because the magnetic moments of the two ferromagnetic layers nearly cancel each other; the reduction of the net magnetic moment in a SAF structure results in a significantly enhanced pinning field provided by the AFM layer while also significantly reducing the stray field exerted on the free layer. The use of a SAF in the GMR structure was essential to have sufficient pinned layer magnetic stability, while a reactively sputtered NiO AFM provided a high enough blocking temperature for HDD applications.[26] Figures 1(a) and 1(b) show the GMR structures with and without SAF layers. Figure 1(c) shows the stability of the GMR ratio for these two structures. The GMR ratio stability with the SAF was clearly superior after exposure to the 200 Oe reverse magnetic field at 150 °C for 100 h, representing extreme HDD conditions. The HDD industry has used the SAF structure ever since, and it is also used today (in the perpendicular form and without an AFM) for MRAM products as part of the perpendicular magnetic tunnel junctions (pMTJs) to pin the magnetization of one of the junction electrodes.

Ion beam sputtering (IBS) was used to deposit the GMR sensor (spin valve) for the first mass produced HDD products.[26] This deposition technology provided a number of advantages for GMR sensor deposition.[28,29] It operated at much lower sputtering gas pressures of ~0.1 mTorr (about 2 orders of magnitude lower than conventional sputtering) that provided long mean free path (~50 cm) and higher energy for the sputtered particles resulting in smoother layers, higher density films, and sharper interfaces. In addition, IBS targets and substrate faced each other at an oblique angle and had a significantly larger target to substrate separation (>25 cm). This allowed for the use of a relatively small target area to deposit films on

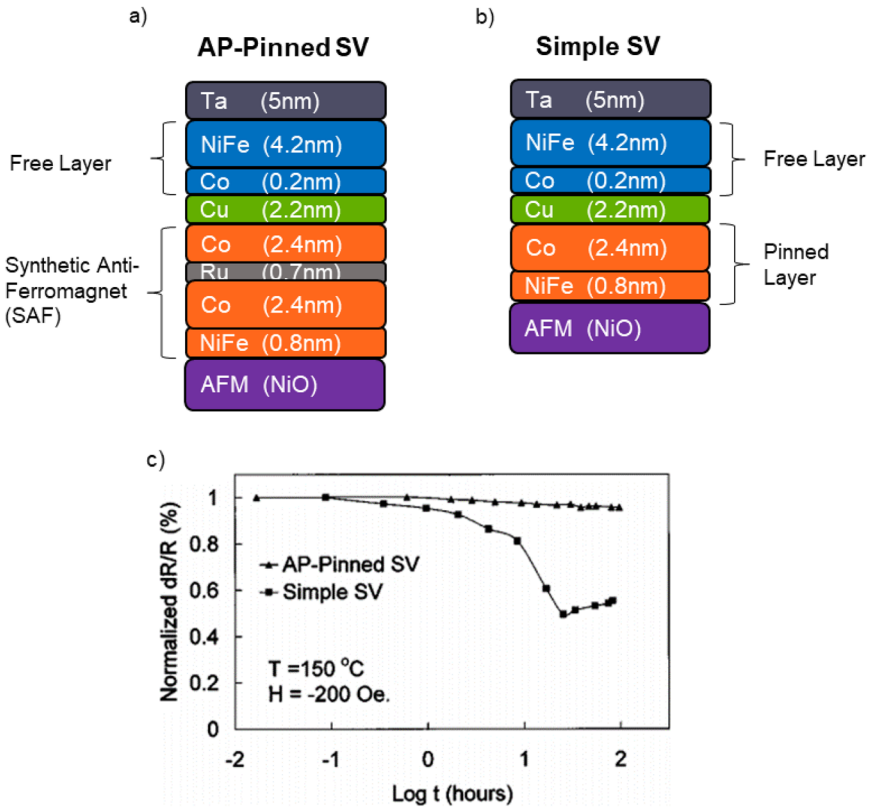

FIG. 1. The structure and data for the first mass produced spintronic device used in HDDs in 1997.[26] (a) Layers of the "AP-pinned spin valve" structure that was used in HDD products. This device uses the SAF structure. (b) The layers for a "simple spin valve" structure (no SAF). (c) The stability provided by the SAF for the GMR structure exposed to 150 °C and 200 Oe reverse field for 100 h.

large substrates. These unique characteristics, coupled with the substrate rotation, provided the necessary thin film quality, including thickness and uniformity control, across the wafers. Conventional sputtering is a widely used manufacturing friendly deposition technology; hence, these features of the ion beam sputtering technology were subsequently designed and incorporated into a conventional sputtering technology tool developed by Anelva. This new tool was specifically designed for GMR (as well as TMR) depositions and was ready in 2001 for GMR sensor production for HDDs. Indeed, MRAM manufacturing tools today by Anelva, TEL, and Applied Materials all have these unique features (low operating pressure, long target to substrate spacing, and oblique angle between targets and the substrate).

Significant GMR development efforts finally resulted in the first spintronic device for mass production. IBM announced the first HDDs with the GMR sensor [shown in Fig. 1(a)] in 1997.[30] The HDD industry adopted the GMR sensors rapidly. The use of the GMR effect, along with new technologies, has made it possible to increase the areal density of the HDDs more than two orders of magnitude in about a decade.[1,6] Furthermore, most of the materials, structures, and tooling and processing techniques that we use today for MRAM technology were initiated during the GMR sensor development by the HDD industry.

TUNNELING MAGNETORESISTANCE

GMR structures used Cu as a separation layer between the two magnetic electrodes.[22] As noted earlier, in 1995, Moodera *et al.*[14] and Miyazaki and Tezuka[15] demonstrated tunneling magnetoresistance with an AlO_x barrier. Tunneling magnetoresistance (TMR) of ~20% in this structure was significantly higher (>3X) with respect to the GMR effect observed on all metallic structures, and the device resistance-area product was also significantly larger. At this time, ideas were also forming for use of this technology to develop solid state memory devices. However, TMR research was still largely being carried out for HDD applications. A major breakthrough was the proposal by Butler *et al.* in 2001[16] of very high TMR values with a crystalline MgO barrier associated with a symmetry-based spin filter effect. Parkin *et al.*[17] and Yuasa *et al.*[18] independently demonstrated significantly higher TMR values with the MgO barrier layer in 2004. All TMR devices today for HDD, as well as for MRAM applications, use MgO as a tunneling barrier.

MRAM TECHNOLOGY

First generation MRAM devices, which were introduced in 2004,[31] operated in a similar way to read heads. For the read sensor, an external magnetic field from the disk changes the magnetization direction of the free layer, resulting in a resistance-change-based signal. In the first generation MRAM devices, the magnetic field from current carrying wires (electrically isolated from the MTJ) is utilized to switch the free layer magnetization. The first idea was to directly switch the free layer with the combined magnetic field from current in two orthogonal wires, called Stoner–Wohlfarth switching.[32] However, this method was unreliable, as it is very challenging to engineer a free layer shape anisotropy with a narrow distribution

of switching fields. It further suffered from the "half-select problem;" current in a single wire destabilized the free layer state and could lead to unwanted switching. These problems were overcome with a very innovative idea to use a SAF free layer in technology known as "Toggle MRAM."[31]

MRAM devices today utilize spin transfer torque (STT) to switch the free layer magnetization without any external magnetic field. STT based switching was first predicted in 1989 in MTJ structures by Slonczewski[19] and in GMR-based structures independently by Slonczewski[20] and Berger[21] in 1996. STT switching was demonstrated on all metallic pillars by Katine *et al.*[33] in 2000. STT-based switching of the AlO_x-based in-plane TMR structures was reported by Hui *et al.* and Fuchs *et al.* in 2004.[34,35]

In the in-plane MTJ structures, large current densities are required to switch the magnetization of the free layer. This is a result of a large demagnetization field associated with the in-plane magnetic free layer, which makes these structures very inefficient, with efficiency defined as the ratio of the energy barrier to thermal activated magnetization reversal to the threshold current [see Eq. (3)]. For in-plane magnetized free layers, the thermal stability of the free layer is defined by the magnetic shape anisotropy of an elliptically shaped pillar, while the threshold current is proportional to the easy-plane anisotropy set by the much larger demagnetization field.[36] Orthogonal spin transfer (OST) structures were developed[37,38] that enhanced the switching characteristics of the in-plane MTJs. However, the elliptical size and shape control of the in-plane MTJs, in addition to minimum size requirements for thermal stability, provided a limited window for product applications.

With the arrival of the perpendicular magnetic tunneling (pMTJ) structure, all efforts shifted to perpendicularly magnetized structures.[39] The switching efficiency can be large in such structures, as the threshold current is directly proportional to the energy barrier to thermally activated magnetization reversal. Toshiba was the first to demonstrate STT switching using perpendicularly magnetized structures.[40] The development of the interface-based perpendicular magnetic anisotropy using the CoFeB based free layer[41,42] led to the development of the pMTJ structures that are used today. The pMTJ structures provided significant performance advantages for STT-MRAM and paved the way for product development for a variety of applications, such as industrial,[43] MCU and IoT,[44] automobile,[45] and frame buffer memory[46] applications. Studies were also conducted for cryogenic[47] and L4 cache applications.[48]

STT-MRAM PERFORMANCE ATTRIBUTES

Solid state non-volatile memory performs three key functions: reading, writing, and storing the information. All of these memory functions in STT-MRAM take place in the MTJ structure. Basic device performance of the pMTJ structure can be characterized by the TMR ratio, critical switching current (voltage), and thermal stability. These parameters control reading, writing, and storing the information and collectively control the overall performance of the device for MRAM application.

The pMTJ structure can be simply depicted by two magnetic electrodes separated by thin tunneling oxide, as shown in Fig. 2(a). One of these electrodes has its magnetization fixed perpendicular to the plane (reference layer), while the second magnetic metal layer (free layer) is engineered to have two stable magnetization states. The relative magnetization orientations of the two electrodes define the two memory states. When the electrodes are parallel, it is a low resistance, or "0," state, and when they are anti-parallel, it is a high resistance, or "1," state, as shown in Figs. 2(a) and 2(b). Unlike the first-generation toggle MRAM devices or read sensors in hard disk drives, where the magnetic field is required to switch the free layer magnetization, the STT-MRAM MTJs require only electrical current to switch the magnetic orientation of the free layer. The fact that these MTJ devices operate only with electric current enables easy integration with logic circuits to build solid state memory devices. This also leads to far higher densities compared to the first generation toggle MRAM devices.

Figure 3(a) shows the STT-MRAM bit cell, and Fig. 3(b) shows the pMTJ pillar. The bit is selected with the word line through the transistor and operates with the bias applied to the source and bit lines. One transistor is needed to operate each bit cell, and the size

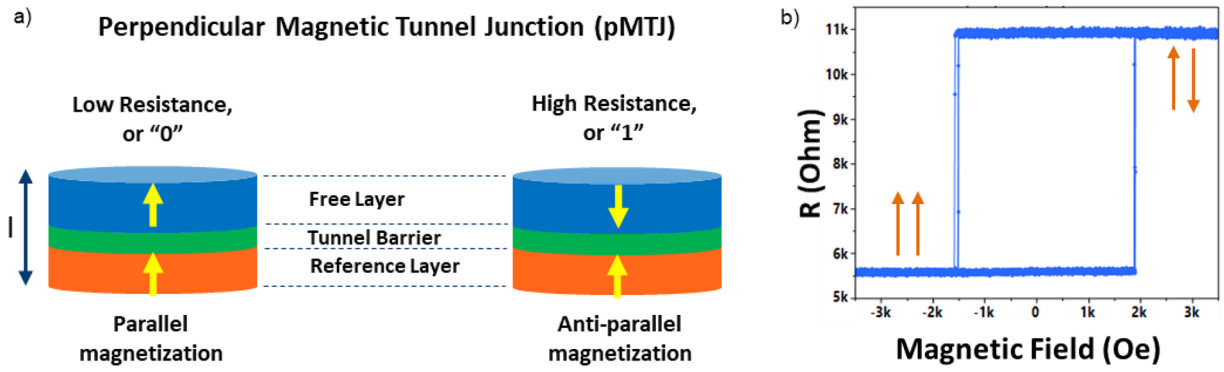

FIG. 2. (a) The simple depiction of the "0" and "1" logic states as defined by the relative magnetization orientation of free and reference layers. (b) An example of the resistance change between the two logic states as a function of the magnetic field strength. The higher the magnetic field required for switching, the higher the energy barrier and, hence, the data retention.

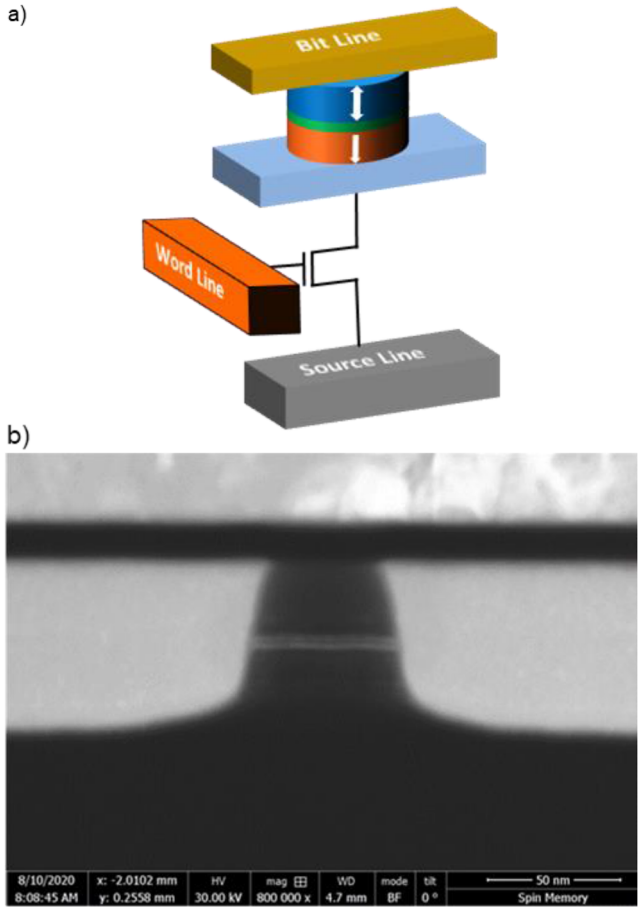

FIG. 3. (a) The pMTJ bit cell. Each bit cell requires one transistor. The bit cell is selected through the word line and operated by applying biases to bit and source lines. (b) SEM picture of an individual pMTJ pillar with ~40 nm diameter. The white lines denote the MgO tunnel barrier and capping layers.

of the transistor is determined by the required write current. Structurally, the pMTJ pillars, Fig. 3(b), can easily be integrated with the logic process flow between the metallization layers. The pMTJ deposition and the ion beam etching tools are the two unique tools with the associated processes that are needed to make MRAM devices in a complementary metal oxide semiconductor (CMOS) foundry. The pMTJ structures are deposited as full film layers using pMTJ deposition tools, annealed to crystallize the ferromagnetic electrodes, and then patterned into pillars. The pMTJ pillar definition step generally uses ion beam etching tools, which have been commonly used in the HDD industry for mass production going back to 1980s.[2,49]

Figure 4(a) shows the wafer surface with high density pillars at an intermediate processing step. The pillars are part of the 4 kb chip, and the picture is taken prior to ion beam etching of the pMTJ structure. After pMTJ structure and hard mask layer depositions and annealing, the wafer is processed through the photoresist patterning step, which defines the circular pillar size. A reactive ion etching process is then used to pattern the hard mask into a pillar shape, as shown in Fig. 4(a). The hard mask layer protects the pMTJ structure during the ion beam etching step. Figure 4(b) shows the cross section of these pillars after ion beam etching of the pMTJ structure, insulator fill, and chemical mechanical planarization (CMP) steps. At this point, pMTJ pillar processing is complete and ready for the top electrical contact. The pillars in Fig. 4(b) are about 25 nm in diameter with a 60 nm pitch. These dimensions indicate that current pMTJ MRAM technology can be extended to very high densities that can provide far higher than 1 Gb level capacities. Even smaller diameter pillars (~5–10 nm diameter and 20 nm height) are reported that rely on shape enhanced anisotropy.[50]

The resistance change between parallel and anti-parallel states, $\%TMR = (R_{high} - R_{low})/R_{low}$, is an important parameter for the pMTJ structure, especially for the reading process. The higher the TMR, the better the separation of "0" and "1" memory states, and the faster the reading process can be. After the initial demonstration of MgO-based MTJ devices,[17,18] significant improvement in the materials and processing over the years pushed the TMR values to several hundred percent.[51,52] Current TMR values for STT-MRAM applications are around 200% after optimizing the structure for the overall MRAM performance.

As a non-volatile memory, thermal stability of the written data is essential for product applications. Data retention is associated with the stability of the free layer magnetization under the device operating conditions. The lifetimes of the magnetic memory states are controlled by thermally activated transitions and can be approximated by the Arrhenius law:[7] $\tau = \tau_0 e^{E_b/kT}$, where E_b is the energy barrier, T is the temperature, k is the Boltzmann constant, and τ_0 is the characteristic attempt time, on the order of 1 ns. The energy barrier between the two states, E_b, is proportional to the effective anisotropy energy density (K) and free layer volume (V = area × thickness). The anisotropy energy (K) is determined by the bulk (K_b) and the interfacial anisotropy (K_i) contributions; $K = K_b - M_s^2/2\mu_0 + K_i/t$, where M_s is the free layer saturation magnetization, t is the free layer thickness, and μ_0 is the permeability of free space. High thermal stability factors ($\Delta = E_b/kT >= 60$) are needed to satisfy the retention requirements for demanding applications.[45] For smaller pMTJ dimensions, the interfacial anisotropy of the free layer has to be increased to compensate for the area reduction so that a large enough energy barrier can be maintained.

The writing process for STT MRAM devices is stochastic. In the macrospin model, the critical switching current and the energy barrier that provides the thermal stability for pMTJs are directly coupled,[53]

$$I_{c0} = \frac{4e\alpha}{\eta\hbar} E_b, \tag{2}$$

where α is the Gilbert damping parameter, e is the electron charge, η is the spin current polarization factor, and $\hbar$ is the reduced Planck constant. Unlike the in-plane MTJ structures, the write current and thermal stability correlation for the pMTJs make these structures far more efficient. For any given application, the lower the switching current, the better it is, but the data retention requirement must also be met. pMTJ structures are designed and formed for optimum performance by carefully managing the conflicting pMTJ parameters for a given application. A general figure of merit for the pMTJ device is its STT efficiency,[53] which is the ratio of the thermal stability factor to the critical switching current,

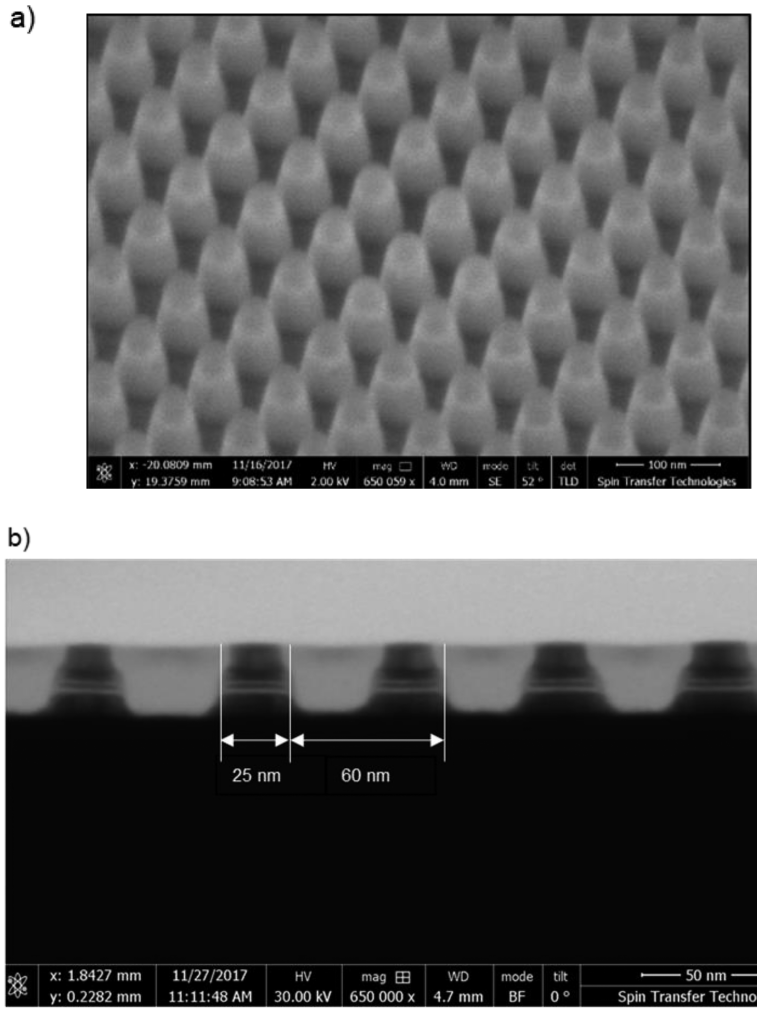

FIG. 4. (a) SEM picture shows the wafer surface for high density processing at an intermediate processing step. The pillar structures are shown after photoresist and reactive ion etching of the hard mask layer. The hard mask layer protects the pMTJ structure during the ion beam etching. (b) The cross section of the high density pillars after they are formed. The pillar diameters are ~25 nm with ~60 nm pitch, demonstrating capabilities to make high density chips.

$$\varepsilon = \frac{\Delta}{I_{c0}}. \tag{3}$$

For a given pMTJ material set, the STT efficiency value is constant in a macrospin model (proportional to the ratio of the spin current polarization factor to the Gilbert damping parameter: η/α). For high thermal stability applications, the energy barrier must be increased. For high speed applications, the energy barrier must be lowered (lower switching current/voltage), allowing for faster switching speeds and higher endurance. One has the freedom to tune the structure for high thermal retention or high speed and endurance within the confines of the STT efficiency, but one cannot enhance either one of these without degrading the other. This tunable behavior of the pMTJ structures led to flash-like (high thermal retention) or SRAM-like (high speed and endurance) STT-MRAM platforms.

For example, for some embedded memory applications (memory manufactured on the same chip as logic), the device must retain the information during the solder reflow process, which is done at 260 °C.[45] In this case, maximum E_b is required. Because of the high energy barrier, high retention devices have lower endurance. On the other hand, for high speed applications, thermal stability can be traded for lower switching current so that speed and endurance can be enhanced. As the pulse duration is reduced for high speed applications, the switching current increases for a given switching probability. The data in Fig. 5(a) show the stochastic nature of the switching process. The probability of switching is increased as the switching voltage (current) is increased. Figure 5(b) shows that, for a given switching probability, the switching voltage (current) has to be raised as the switching speed increases.

Increased switching voltage (current) for high speed puts great stress on the MgO barrier and significantly reduces the endurance.[54,55] Therefore, for a given application, the pMTJ structure has to be optimized to provide the needed TMR, switching current, retention, speed, and endurance all at the same time. As a result, STT efficiency is a key figure of merit defining the pMTJ performance.

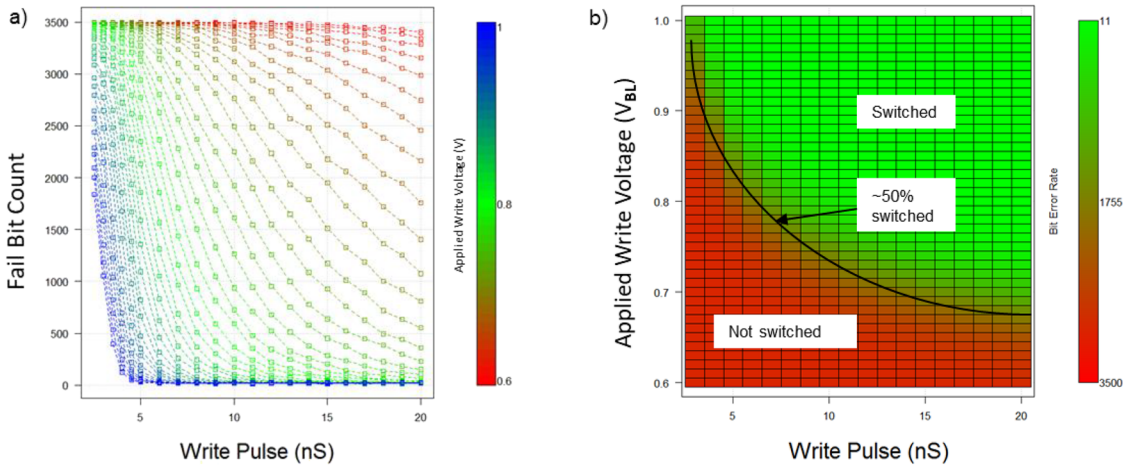

FIG. 5. (a) The chart shows that switching voltage has to be increased for higher writing probability or faster writing. (b) Voltage needed to get to 50% switching probability increases as the write pulse width is reduced. The voltage values are normalized to 1 V, and the line in (b) is drawn as a guide to the eye.

Over the years, significant R & D efforts resulted in complex and efficient perpendicularly magnetized free layer structures. The key enabler for perpendicular free layer magnetization was the reduction of the CoFeB thickness such that the CoFeB/MgO interface provides the necessary perpendicular interfacial anisotropy[41] that overcomes the in-plane anisotropy. The thickness of the CoFeB layer has to be kept below ~1.2 nm to maintain its perpendicular anisotropy. However, thermal stability degrades significantly as the pMTJ diameter (area) is reduced for high performance applications due to a significant reduction in the interfacial anisotropy and magnetic material. To achieve higher thermal stability, MgO was used as the capping material where CoFeB layers were sandwiched between two MgO layers, creating two CoFeB/MgO interfaces.[56] To increase the interfacial anisotropy further, thin heavy metal layers, such as Ta,[56] Mo,[57] and W,[58] were inserted in the CoFeB free layer (see Fig. 6—pMTJ structure). MgO was also used as an insertion layer to obtain quad CoFeB/MgO interfaces.[59] The thickness of the insertion layer has to be carefully chosen to keep the exchange coupling between the separated CoFeB layers. As the thickness of the metal layers increases, the exchange coupling degrades rapidly.[60] Micromagnetic modeling[61] and experiments on 8 Mb pMTJ chips[62] show that the exchange coupling, perpendicular magnetic anisotropy, and free layer volume all play an important role in setting the thermal stability of the free layer.

pMTJ Layers and Materials

Oxide Cap		MgO	0.6 to 0.9nm	Cap
Free Layer	Free layer 2	CoFeB	0.4 to 1.0nm	Free Layer
	Anisotropy layer	Ta, Mo or W	0.2 to 0.4nm	
	Free layer 1	CoFeB	1.1 to 1.6nm	
Tunnel Barrier		MgO	1nm	MgO
Reference layer (SAF 2)	Ferromagnetic layer	CoFeB	0.5 to 1.0nm	Pinned Layer
	Anisotropy Layer	Ta, Mo or W	0.2 to 0.4nm	
	Ferromagnetic layer	Co	0.1 to 0.4nm	
	2 to 6x Multilayer	Pt	0.1 to 0.4nm	
		Co	0.1 to 0.4nm	
SAF Coupling layer		Ru	0.7nm	
SAF 1	3 to 5X Multilayer	Co	0.1 to 0.4nm	
		Pt	0.1 to 0.4nm	

FIG. 6. The typical layers for the pMTJ structure. The thickness values are shown as an example and can be modified to meet specific application requirements. Note a couple of the similarities between the GMR structure [Fig. 1(a)] used in the first HDD production in 1997 and the current pMTJ structures. First, both structures are using the synthetic AFM (SAF) structure with ~7A Ru as the exchange coupling layer and second very thin film, on the order of 2A, being part of the multilayer structures.

Typical pMTJ layers are shown in more detail in Fig. 6 where the thickness values are shown as an example. The specific layers, compositions, and thickness values are part of the optimization of the pMTJ structure that can be modified to meet the requirements for a specific application. It is interesting to note a couple of the similarities between the GMR structure used in the first GMR-based HDD in 1997 and the current pMTJ structure. Both devices are using SAF structures with ~7A of Ru as the exchange coupling layer, and both need the deposition of very thin films, on the order of 2A, as part of the device.

Flash-like applications require very high thermal stability pMTJs but generally work with ~50–100 ns speed and ~10^7 or 10^8 endurance. Indeed, pMTJ structures have been developed that meet the most stringent retention conditions (retaining the data during the solder reflow process at 260 °C) for embedded flash applications.[45] For high performance applications, replacement of SRAM-like devices with non-volatile MRAM is still challenging where pMTJ device must provide high speed, high endurance, and required data retention. Even slower SRAM-like applications may require ~10 ns speed and >10^{12} endurance. Time resolved measurements show that the mean switching time is inversely related to the pulse amplitude for varying junction sizes (50–100 nm), but switching dynamics strongly depend on the junction size and pulse amplitude.[63] In another study on 40 nm devices, it is also observed that as the switching speed increases from 5 to 1 ns, the switching voltage increases rapidly in the ballistic regime.[47] An example is shown in Fig. 7 where the critical switching voltage increases ~2x for a pMTJ device (from ~300 to ~650 mV as the pulse width decreases from 5 to 1 ns) for the case of 50% switching probability. An additional ~50% or more (depending on the write speed and required write error rate) increase in voltage (current) may be needed to obtain sufficiently small write error rates (WERs).[64] This demonstrates the challenge to increase the switching speed, keeping high endurance at the same time. Lowering the RA (resistance area product) of the pMTJ can lower the voltage across the MgO barrier, but this also lowers the TMR values. Lower TMR values compromise the fast reading while providing limited relief. In addition, pMTJ structures have to perform across the full product operating temperature range, for example, from −40 to 125 °C or −40 to 150 °C for high grade level products. Therefore, particular attention is needed to meet writing speed and endurance requirements at low temperatures (i.e., −40 °C) and reading and bit reversal (during reading) at high temperatures (i.e., 125 °C). These competing requirements of high speed, high endurance, and required thermal stability have to be balanced against each other to design the device for a full operating temperature range. Further improvements are needed to be able to use STT-MRAM for SRAM-like and other high performance applications.

It is important to note that developing new technologies and making new and advanced products based on these technologies takes many years of research, development, and resources. STT-MRAM is one of these new technologies resulting in unique memory products that are being produced by major foundries around the world today. Therefore, enhancing the performance of these devices and expanding their application areas provide a significant economic value (i.e., it does not require additional large investments, such as in new tools or the development of new processing techniques). To enhance the performance of STT-MRAM, continued material improvements are essential. These could be the development of new alloys with high spin polarization and low damping, multilayer material systems with high thermal stability and low damping, and engineered interfaces that can enhance the interface anisotropy for smaller pMTJ structures. In the next section, Precessional Spin Current STT-MRAM, we will discuss a new multilayer structure that utilizes the basic pMTJ structure, material set, and processing techniques, yet enhances its performance significantly. Because of the above reasons, the new structure will be covered in greater detail below.

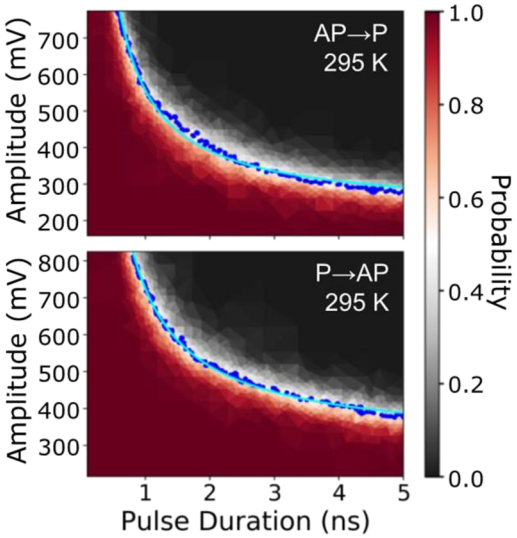

FIG. 7. Increase in the critical switching voltage as the pulse width deceases from 5 to 1 ns.[47]

PRECESSIONAL SPIN CURRENT STT-MRAM

Recent development of a novel concept called Precessional Spin Current (PSC) structure[65–67] delivers significantly increased thermal stability for pMTJs without increasing switching current.[68] Figure 8

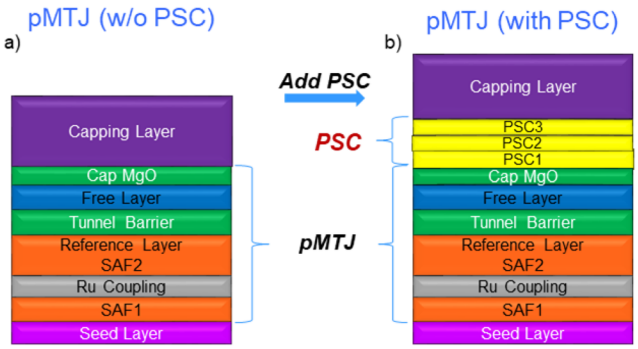

FIG. 8. The pMTJ layer structure without (a) and with PSC (b) is shown. The base pMTJ is the same for both cases. The PSC structure is around ~4 nm thick and added on top of the cap MgO layer.

shows the conventional pMTJ structure (see Fig. 6 for more detailed version) and pMTJ with the PSC structure. The pMTJ structure utilizes a synthetic antiferromagnet structure, a MgO barrier, and the free layer. The PSC structure uses an identical pMTJ but adds the PSC layers on top of the MgO cap. The PSC layers are magnetically and electronically coupled to the base pMTJ. The PSC structure thickness is on the order of only 4 nm (PSC1: ~0.6 nm Fe, PSC2: ~1.5 nm Ru, and PSC3: ~1.8 nm CoFeB) and does not introduce any new materials. The thin PSC1 layer has an interface with a MgO cap and is only 0.6 nm thick and therefore has perpendicular magnetization, whereas the PSC3 layer is ~1.8 nm thick and has in-plane magnetization and does not have a fixed magnetization direction. The PSC3 magnetization is magnetostatically coupled to the free layer, and its magnetization is free to precess with the free layer magnetization under the electrical bias, hence the term "precessional spin current" structure.

Experiments have shown that the STT efficiency with the PSC structure can be significantly increased compared to the base structure, as shown in Fig. 9. For high speed applications, smaller diameter pMTJs are preferred. Figure 9 also shows that the PSC's efficiency improvement is even stronger for smaller pMTJ structures.

To further quantify the PSC improvement, two pMTJ structures (one with PSC and one without PSC) were integrated onto two 200 mm complementary metal oxide semiconductor (CMOS) wafers. The base pMTJ structure was the same for both wafers. Approximately 25 test chips (each chip with 4 kb devices) from each wafer were completed and tested to determine the device performance. The electrical size of the tested devices was ~45 nm. The results were obtained using the 10 ns pulse width and are summarized in Table I. Both switching voltage and switching current values are the median values, covering all the devices from each wafer. As the switching data show, there are no significant differences in the median switching voltage or current for wafers with and without PSC.

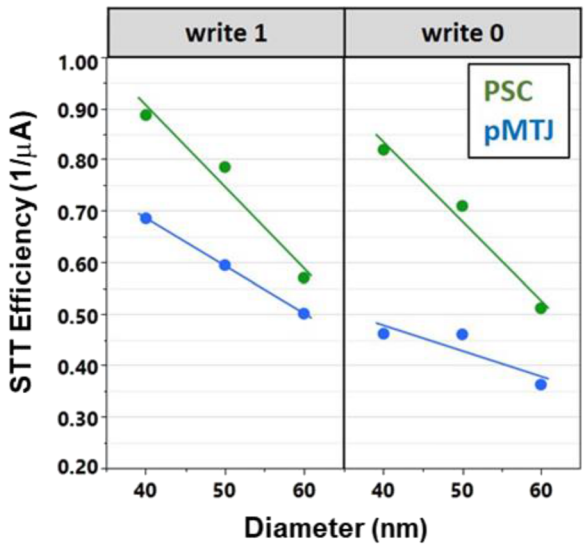

FIG. 9. Spin transfer torque efficiency improvement with the addition of the PSC structure is shown.[68] The relative gain is larger for smaller diameter devices.

TABLE I. This summarizes the switching and the retention data for two wafers: one without PSC and the other one with PSC. Twenty five test chips (each with 4 kb devices) across each wafer were tested. The median switching current and median switching voltage for all devices are listed for "0" and "1" transitions with 10 ns pulse width. No switching differences between these two wafers were observed. However, the wafer with PSC shows more than 3 orders of magnitude higher data retention values as measured on 4 MB chips from the same wafers.

Parameters	pMTJ w/o PSC	pMTJ w/PSC
V_{median} (0 to 1)	0.37 V	0.35 V
V_{median} (1 to 0)	0.58 V	0.55 V
I_{median} (0 to 1)	105 μA	103 μA
I_{median} (1 to 0)	100 μA	101 μA
Data retention time at 85 °C (10 ppm failure rate)	~1 h	~8×10^3 h

From the same wafers, three 4Mbit chips for each design were selected from identical locations. The thermal failure rates for 4 kb and 4 Mb chips from each wafer showed the same behavior, but data from 4 Mb chips were used for better statistics. The analysis was done using the effective delta method.[69] These results are also shown in Table I. There is more than 3 orders of magnitude increase in retention time for the MRAM devices with the PSC structure, while both sets have the same base pMTJ structure. The extrapolation of these data to room temperature shows that the energy barrier increases from ~1.6 eV ($\Delta \sim 62$) to ~2.1 eV ($\Delta \sim 82$) with the addition of PSC.

The median voltage and current values for these test chips show the same behavior across the full test range from 10 to 100 ns pulse widths. The measurements at 50 and 100 ns along width ten pulse widths are shown in Fig. 10.

Figure 11 shows the bit error rate (BER) measurements for 100 randomly selected MRAM cells from each design. Because of the large sample size, the experiments were conducted down to the 10^{-5} bit error rate (BER) level. The BER curves for 20, 50, and 100 ns pulses are listed in Fig. 11. All samples show very smooth transitions in all the cases, and no differences have been observed.

Data from these wafers show that the addition of the PSC structure provides a significant advantage to the pMTJ structure. The STT efficiency increases ~40%, which is mainly due to the increase in thermal stability. The thermal stability increase is thought to be related to the magnetic coupling of the free layer to the PSC magnetic layers that acts as an additional magnetic volume during the off state. During the switching process, it is likely that additional spin polarization in the in-plane magnetic layer[70] in PSC3 and tilting of the free layer magnetization (due to magnetostatic coupling to PSC) help keep the switching current similar to the base pMTJ. Further experiments are needed to understand the details of the switching process with the PSC structure.

The STT efficiency enhancement can especially be useful to meet the requirement for SRAM-like applications in terms of speed and endurance. In the set of experiments reported, the switching voltage and current were the same for both wafers, but PSC wafers demonstrated significant retention improvement. Utilizing

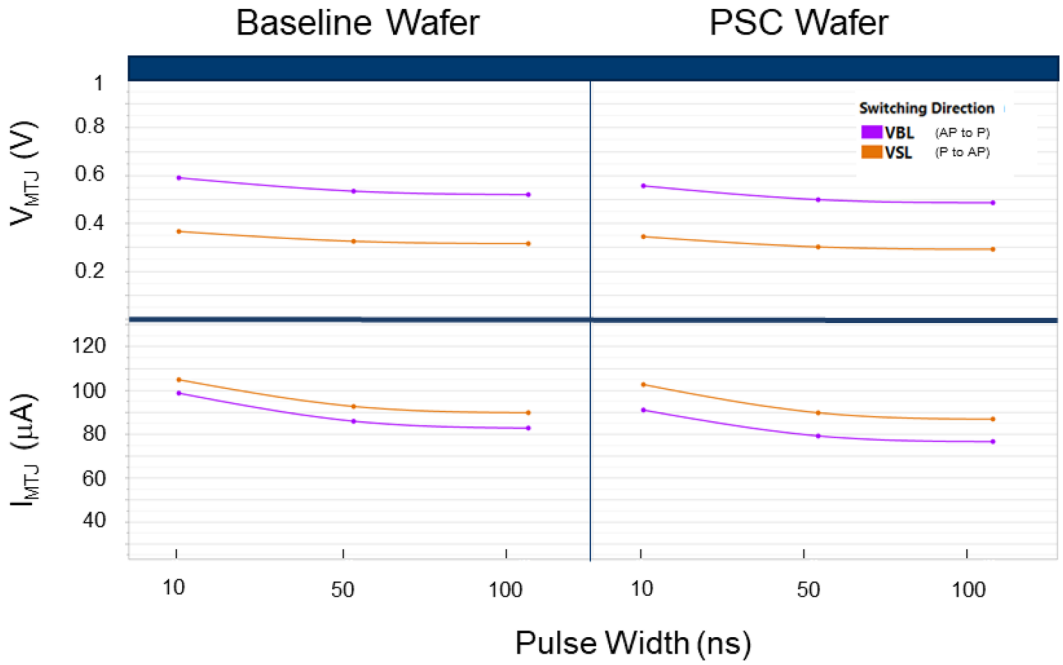

FIG. 10. Median switching voltage and median switching current values for each wafer are shown. The data are shown for both transitions at 10, 50, and 100 ns pulse widths. The switching characteristics of both wafers are very similar.

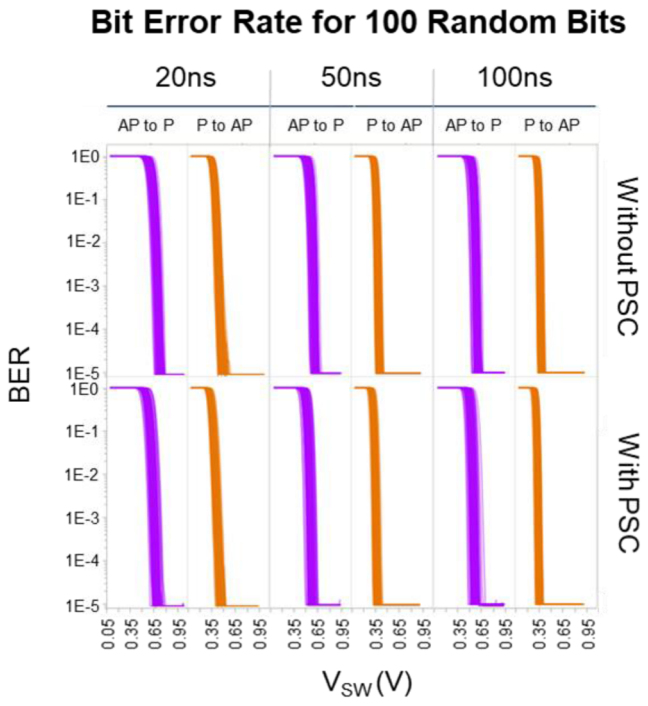

FIG. 11. One hundred randomly selected devices from each wafer have been tested down to the 1E-5 BER level. The foot at 1E-5 is due to the limit in the measurements, not write errors. The BER curves for these devices are shown for both (AP to P and P to AP) transitions tested at 20, 50, and 100 ns pulse widths. No differences have been observed in the switching behavior of these two cases.

the tunability characteristics of the pMTJ structures, the PSC data retention can be traded-off for more speed and endurance. This is schematically shown in Fig. 12.

For example, by modifying the free layer, the base pMTJ can be made with lower thermal stability, i.e., having lower E_b (lower switching current and voltage). This structure can be faster with higher endurance since both switching voltage and current will be lower as a result of lower E_b. The addition of the PSC to this pMTJ will bring up the thermal stability, yet keep the lower voltage (current) advantage of the modified base pMTJ. This will result in further improvements in speed and endurance and have the required thermal retention for SRAM-like applications.

FUTURE SPINTRONICS

There have been many promising research advances in the last decade that can impact technology. The one with the most likely near-term impact is the discovery of magnetization switching by spin–orbit torques[71] and the observation of a giant spin-Hall effect by Ta,[72] characterized by a large spin-Hall angle, a large ratio of the spin current to the charge current. This enables a three-terminal device, with separate write and read contacts, as illustrated in Fig. 13 and, as a result, the possibility of separate optimization of write and read processes. This structure reduces the stress on the magnetic tunnel barrier as the current flow through the tunnel barrier is only used for readout, which can be done at low bias voltage. A down-side is the larger area is needed—and in most implementations—the need for two transistors per MTJ. However, the fact that the TMR can be increased while the impedance of the write channel can be separately varied and higher endurance (due to lower stress on the

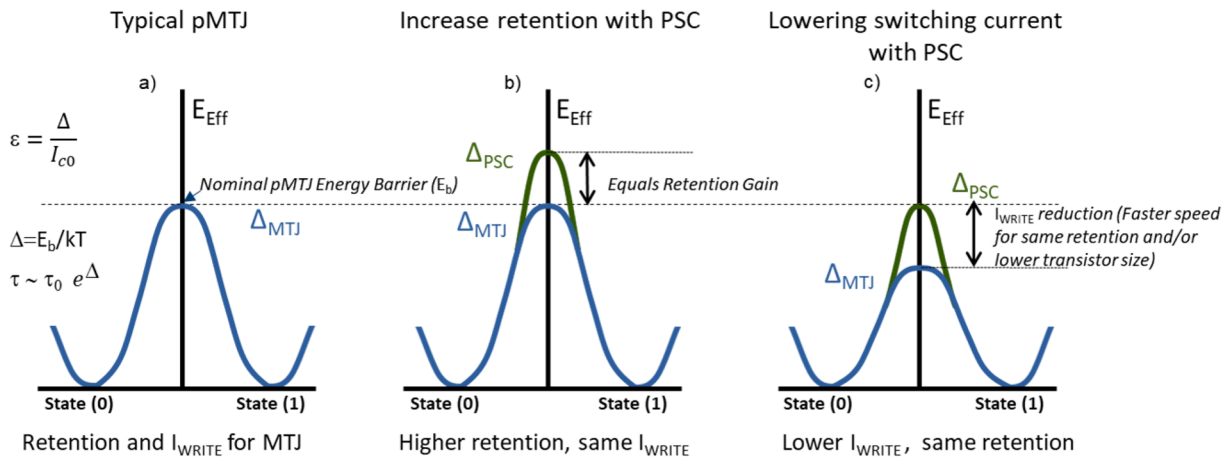

FIG. 12. Schematic presentation of the PSC effect. (a) Energy barrier (in blue) for a pMTJ structure defines the writing and data retention characteristics. (b) Addition of the PSC increases the energy barrier for data retention shown in green. However, the writing voltage and current do not change, as shown in Table I. This indicates that we are dealing with two effective energy barriers: one for retention (green) and the other for switching (blue). (c) Another option is to design a free layer with a lower energy barrier, hence providing a faster switching and/or smaller switching current. In this case, however, the base pMTJ will have lower data retention. Adding PSC to this pMTJ will increase the data retention (green), while switching is defined by the pMTJ energy barrier (blue). Therefore, the PSC can be used for data retention increase or can be utilized for faster switching.

MgO barrier) are an advantage. For example, this enables the application of currents further above the threshold value, which increases the switching speed.[73]

Increasing the charge-to-spin conversion efficiency has led to the exploration of topological insulators. Here, extremely large spin-Hall angles have been observed independently by two groups.[74,75] Recently, switching of the ferromagnetic metal has been observed at room temperature, showing that topological insulators as a source of spin angular momentum is not simply a physics curiosity.[76]

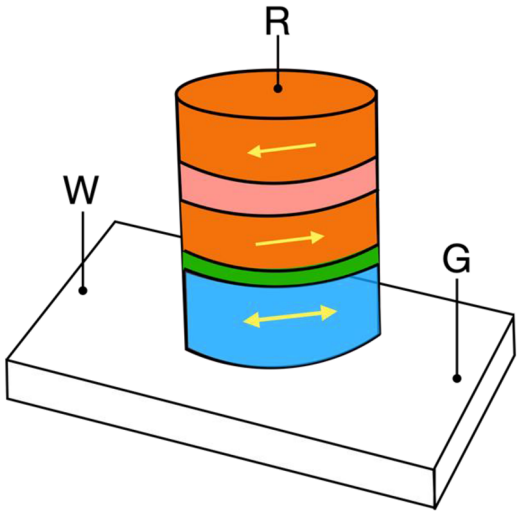

FIG. 13. Spin–orbit torque device showing write (W), read (R), and ground (G) contacts. The free layer (blue) is part of an MTJ with the reference layer that is part of a SAF (orange layers).

Composition changes and interface engineering have also been shown to increase the charge-to-spin conversion efficiency of heavy metals, such as Pt.[77]

It is important to note that spin–orbit torques associated with the spin-Hall effect in heavy metals and topological insulators are generally polarized parallel to the thin film plane, making them most efficient for switching in-plane magnetized elements. As discussed above, the switching current is generally larger for in-plane elements because of their strong easy plane anisotropy, associated with their demagnetization field. Furthermore, the elements' thermal stability is associated with magnetic shape anisotropy, leading to a minimum element size.

The benefits of perpendicularly magnetized MTJs are clear. Their switching efficiency can be large. Utilizing a ferromagnetic layer that provides the in plane magnetic field for deterministic switching has been demonstrated for pMTJs where the ferromagnetic layer was deposited as part of the hard mask layer.[78] Switching pMTJs with low currents (and without a symmetry breaking magnetic field, an in-plane magnetic field) can also be accomplished if spins have a polarization with a component perpendicular to the film plane. Spin polarized currents of this type can be generated by a ferromagnetic layer by the mechanism of the anomalous or planar Hall effects, as discussed theoretically[79] and recently observed in the experiment.[80,81] The challenge is that the magnetization of the write magnetic layer needs to be canted with respect to the sample plane. Nonetheless, these approaches appear fruitful in that they build on material optimization and processing learning associated with the development of present day two-terminal pMTJ STT-MRAM.

SOT MRAM, even with two transistors, can have a smaller footprint than SRAM. However, SOT fabrication is more challenging than STT-MRAM. The thickness of the heavy metal SOT layers is usually less than 4 nm as higher thickness values of W result in a

lower spin-Hall effect due to heavy metal (W) phase change.[82] In addition, once the layer thickness is comparable to its spin-diffusion length (also, typically several nm), there is no increase in the charge-to-spin efficiency with increasing heavy metal layer thickness. The very thin heavy metal SOT layer makes fabrication challenging as the etching of the MTJ pillar must stop precisely below the free layer.

SUMMARY

Significant developments in the spintronics field from the GMR invention to STT-MRAM technologies were presented. Early work during the development of the GMR technology for HDD application started with magnetic materials, processing, magnetic multilayers, deposition tooling, and device applications and, therefore, initiated the formation of the ecosystem that we use today for MRAM technology. Discovery of the spin transfer torque effect made it possible to develop solid state memory devices operating with electric current only. STT-MRAM has a unique place in the memory hierarchy because of its thermal stability, speed, endurance, and easy integration to CMOS logic technology. It is also unique in the sense that its performance can be tuned through the pMTJ structure to meet a wide variety of applications, including applications requiring very high thermal stability or high performance. As noted, speed, endurance, and thermal retention are all interconnected and STT efficiency is the parameter that controls these device performance characteristics. A novel PSC method is shown to significantly increase the STT efficiency of the devices. Addition of this structure to the base pMTJ shows very similar switching current (voltage) while increasing the data retention more than 3 orders of magnitude. Since PSC is added on top of the MgO cap, PSC improvement is additive to any enhancements to the base pMTJ. Alternatively, the thermal retention improvement provided by a PSC can be traded in for speed and endurance gain, therefore offering an additional pathway to meet the requirements for high performance SRAM-like applications. Finally, recent discoveries can impact technology, particularly the large charge-to-spin conversion efficiency associated with spin-Hall effects in heavy metals and ferromagnetic metals and strong spin–orbit coupling in topological insulators. Significant increases in energy efficiency and advances that enable further scaling can justify the development efforts required to incorporate new materials into MTJ devices.

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

DATA AVAILABILITY

The data that support the findings of this study are available within the article.

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