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Nanoscale Control of the Metal-Insulator Transition at LaAlO₃/KTaO₃ Interfaces

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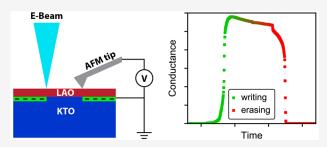
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ABSTRACT: Recent reports of superconductivity at KTaO₃ (KTO) (110) and (111) interfaces have sparked intense interest due to the relatively high critical temperature as well as other properties that distinguish this system from the more extensively studied SrTiO₃ (STO)-based heterostructures. Here, we report the reconfigurable creation of conducting structures at intrinsically insulating LaAlO₃/KTO(110) and (111) interfaces. Devices are created using two distinct methods previously developed for STO-based heterostructures: (1) conductive atomic-force microscopy lithography and (2) ultralow-voltage electron-beam lithography. At low temperatures,



KTO(110)-based devices show superconductivity that is tunable by an applied back gate. A one-dimensional nanowire device shows single-electron-transistor (SET) behavior. A KTO(111)-based device is metallic but does not become superconducting. These reconfigurable methods of creating nanoscale devices in KTO-based heterostructures offer new avenues for investigating mechanisms of superconductivity as well as development of quantum devices that incorporate strong spin—orbit interactions, superconducting behavior, and nanoscale dimensions.

KEYWORDS: LAO/KTO, c-AFM lithography, ULV-EBL, nanoelectronics, superconductivity

The rich physical properties of complex-oxide heterostructures and the paradigm of semiconductor nanoelectronics have begun to overlap, resulting in the emerging field of correlated nanoelectronics. Significant advances have been made with SrTiO₃ (STO)-based heterostructures, which host an exceptionally wide range of gate-tunable physical properties including superconductivity, magnetism, ferroelectricity, and ferroelasticity. Superconductivity in STO was discovered more than half a century ago, and there is still no consensus about the underlying mechanism.

The discovery of superconductivity in heterostructures based on KTaO₃ (KTO) represents a breakthrough as a "sibling" system that share many similarities with STO. 15-17 Liu et al. reported superconductivity at EuO/KTO(111) and LaAlO₃ (LAO)/KTO(111) interface with a superconducting transition temperature $T_c \approx 2 \text{ K.}^{15}$ Interfacial superconductivity was subsequently observed with LAO/KTO(110) heterostructures with $T_c \approx 0.9 \text{ K.}^{17}$ The band structure of KTO is similar to STO except that the conduction band of KTO comes from the 5d orbital of Ta rather than 3d orbital of Ti. 18,19 Like STO, KTO is a "quantum paraelectric" with a nearly diverging permittivity that saturates at low temperatures,²⁰ presumably due to quantum fluctuations of the ferroelectric soft mode. It was known previously that superconductivity at the KTO(001) surface, with carriers induced by electrolyte gating, is exceptionally weak, with $T_c \approx$

50 mK and with very low critical current densities. ²¹ LAO/KTO(001) heterostructures host 2D electron gases (2DEGs), but superconductivity was not reported. ¹⁵

Insight into correlated electron phenomena, such as superconductivity at oxide interfaces, can be obtained by the creation of nanoscale devices. Among the various methods, conductive atomic-force microscopy (c-AFM) lithography enables sub-10 nm devices to be "sketched" and "erased", 22 resulting in a wide range of mesoscopic devices whose properties can help constrain physical mechanisms and potentially find use in future quantum device applications. Experiments with LAO/STO devices have created quasi-2D, 1D, and 0D structures that provide insight into the nature of the superconducting state. 23-29 Recently, Yang et al. reported an alternate way to create electronic devices at the LAO/STO interface using ultralow-voltage electron-beam lithography (ULV-EBL). This technique offers significantly faster writing speed compared with c-AFM lithography, while maintaining comparable resolution and device quality. This technique

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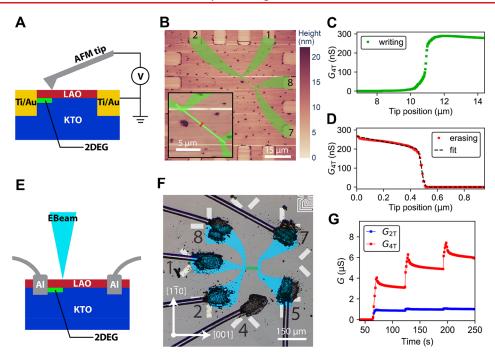


Figure 1. Reconfigurable patterning of LAO/KTO(110) heterostructure. (A) C-AFM method in which a biased conductive AFM tip is scanned over the LAO surface. (B) Top view of c-AFM pattern, where green areas depict regions where $V_{\rm tip} > 0$, and red regions depict areas where $V_{\rm tip} < 0$. Inset: zoom-in view of the main channel. (C,D) Combined experiment where a single nanowire is sketched between leads 1,2 and 7,8. Subsequent erasure yields an estimate of the nanowire width $w \sim 20$ nm. (E) ULV-EBL writing method in which ~ 500 V electrons are focused on a pattern, also resulting in local changes to the conductance at the LAO/KTO interface. (F) Top view of a patterned area. Interface contacts are obtained by Al wire bonds, and blue regions represent "virtual electrodes". Electrical conductance between leads 8,1,2 and 5,7, $G_{\rm 4T} = I_{15}/V_{87}$ is achieved by a final rectangular pattern (width w = 15 μ m, length l = 60 μ m indicated in green. (G) Measured four-terminal and two-terminal conductance G as the last rectangular region is patterned. Each conductance jump corresponds with one exposure with 10 μ C/cm².

provides a new avenue for producing significantly more complex devices and for integrating complex-oxide heterostructures with other quantum materials.

Here, we adapt the c-AFM lithography and ULV-EBL techniques to patterning the LAO/KTO(110) and LAO/ KTO(111) interfaces. The conductivity of the KTO interface depends on the thickness of the LAO layer with an observed critical thickness $t_{\rm c} \approx 3$ nm.³¹ A LAO/KTO heterostructure is prepared by depositing a 3 nm-thick amorphous LAO film on KTO(110) single crystal by pulsed laser deposition. Electrical contact to LAO/KTO interface is fabricated by Ar⁺ milling, followed by sputter deposition of Ti/Au; a second layer of Ti/ Au on top is added to create pads for wire bonding. The c-AFM lithography setup is illustrated in Figure 1A. The LAO/ KTO(110) interface is initially insulating with G < 1 nS conductance measured between any pair of electrodes. Figure 1B shows an AFM image of one of the LAO/KTO(110) "canvases". Green areas indicate regions that are to be scanned with a positive bias and red areas indicates regions to be scanned with negative bias. As the one-dimensional path (green line, Figure 1B inset) is sketched by the AFM tip ($V_{\text{tip}} =$ +16 V), a sharp four-terminal conductance jump $\Delta_{\rm 4T} \approx 300 \text{ nS}$ is observed (Figure 1C), indicating the creation of conducting path between the two pairs of leads 1,2 and 7,8. The details of LAO film growth, Ti/Au electrodes deposition, and c-AFM lithography can be found in Supporting Information. The c-AFM writing with LAO/KTO(110) is reversible. When the tip is negatively biased ($V_{\text{tip}} = -8 \text{ V}$) and moved across the existing wire along the red path in Figure 1B, inset (with tip velocity $v_{tip} = 50 \text{ nm/s}$), a steep drop in the conductance is observed (Figure 1D). By curve fitting the conductance drop

(black dashed line in Figure 1D, see Supporting Information and ref 22), the width of the nanowire can be extracted $W \sim 20$ nm. The conductance and the width of the nanowire is comparable to wires created at the LAO/STO interface, 22 indicating a similar mechanism for creating and erasing conducting channels. Most likely, the surface charging of the LAO surface, created by the voltage-biased c-AFM tip, is responsible for nanoscale control of the insulator-to-metal transition at LAO/KTO(110) interface. 32,33 The nature of the surface charges has not been determined, but the most likely sources are ionized oxygen vacancies and water-derived protons. 34,35

We also demonstrate creating conducting channels at LAO/ KTO(110) interface with ULV-EBL. The experimental setup of ULV-EBL is shown in Figure 1E. Six aluminum wire bonds are affixed onto the LAO surface in a circular arrangement to form a ULV-EBL canvas (Figure 1F) that is initially insulating with conductance between any two pairs of wire bonds G < 1nS). During ULV-EBL (see Supporting Information), a voltage V_1 is sourced from electrode 1 and current I_{15} is measured through electrode 5 along with voltage V_{87} across electrode pair 8 and 7 (Figure 1F). Thus, two-terminal conductance is given by $G_{2T} = I_{15}/V_1$, while the four-terminal conductance is given by $G_{4T} = I_{15}/V_{87}$. At first the blue regions are exposed with a total aerial dose of 30 μ C/cm² (Figure 1F). Then the main channel (Figure 1F, green, length = $60 \mu m$, width = 15 μ m) is thrice exposed with an aerial dose of 10 μ C/cm², causing three conductance jumps to be observed (Figure 1G). The four-terminal conductance reaches $G_{4T} = 6 \mu S$, indicating the creation of conducting channels at the LAO/KTO interface ("Device A").

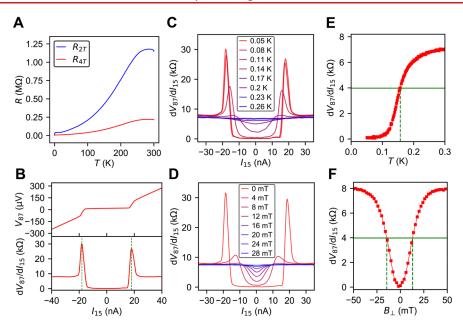


Figure 2. Temperature-dependent magnetotransport of LAO/KTO(110) Device A patterned with ULV-EBL. (A) Two-terminal and four-terminal resistance versus temperature. (B) I-V and dV/dI versus I at T=50 mK and B=0 T. Green dashed lines indicate the critical current. (C) dV/dI versus I over a temperature range 50 mK $\leq T \leq 260$ mK. (D) dV/dI versus I for 0 T $\leq B \leq 0.028$ T acquired at T=60 mK. (E) Zero-bias (I=0) differential resistance versus temperature. Green dashed line indicates temperature at which resistance drops by 50%. (F) Zero-bias (I=0) differential resistance vs magnetic field at T=60 mK. Green dashed line indicates magnetic field at which resistance drops by 50%.

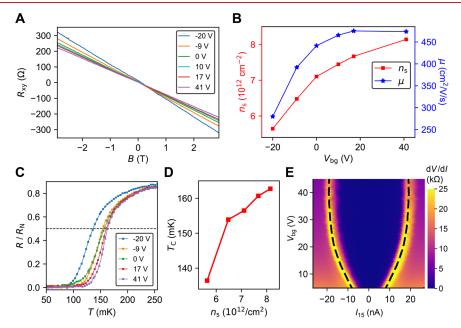


Figure 3. Back gate (V_{bg}) -dependent transport for Device A. (A) Hall resistance versus magnetic field. (B) Hall carrier density n and mobility μ . (C) Normalized resistance versus temperature. Black dashed line indicates where $R/R_N=0.5$. (D) T_c versus carrier density n_s . (E) Differential resistance versus I and V_{bg} at I = 50 mK and I = 0. T. Black dashed lines indicate the critical current I_c .

Device A is transferred to a dilution refrigerator immediately after exposure by ULV-EBL. The decay of KTO-based devices is slowed significantly when the device is stored in vacuum, similar to LAO/STO devices, 32 and conductance decay is completely arrested when the device is cooled to low temperatures. The time when the sample is exposed to air is less than 5 min (Figure S3). Device A remains metallic down to the lowest temperatures measured (\sim 50 mK) (Figure 2A). At T=50 mK and B=0 T, a flat region in four-terminal current-voltage measurement (I-V measurement) is observed for small current values (Figure 2B). On the basis of the I-V

curve, the four-terminal differential resistance $\mathrm{d}V/\mathrm{d}I$ drops sharply from ~7 k Ω to ~110 Ω when the bias current falls below a critical current I_c , defined as the averaged values where the differential resistance reaches a sharp maximum (Figure 2B). For Device A, $I_c = 18$ nA, corresponding to a critical current density $j_c = 12~\mu\mathrm{A/cm}$.

Figure 2C shows dV/dI versus I curve acquired at B = 0 T and temperatures in the range T = 50-260 mK, and Figure 2D shows dV/dI versus I curves acquired at T = 60 mK with different out-of-plane magnetic fields. The superconducting critical current appears to decrease monotonically under

elevated temperature or applied magnetic field. Figure 2E is the plot of differential resistance at zero bias (dV/dI at I=0 nA) versus temperature, which yields $T_{\rm c}=60$ mK, defined to be where the resistance reaches half of the normal state resistance $R_{\rm N}$. The upper critical field $B_{\rm c2}$ can be similarly defined to be the field at which the zero-bias differential resistance reaches half of its normal-state value. Here we find (Figure 2F) $B_{\rm c2}=140$ Oe.

Since the dielectric constant of KTO grows to $\epsilon \approx 4500$ at low temperatures,²⁰ applied voltages to the back of the KTO substrate (V_{bg}) are able to modulate the carrier density of interface devices. Details about the backgating sequence is described in Figure S4, where we noticed hysteretic behavior of Device A indicated by its normal state resistance. Hall measurements are performed at temperatures above the superconducting phase (at T = 0.7 K) for various back gate voltages, while sourcing from electrode 1 to electrode 5 and measuring voltage V_{82} across electrode pair 8 and 2 (Figure 3A). The measured sheet carrier density n_s and electron mobility μ are summarized in Figure 3B. Through back gating, the carrier density can be tuned from $5.6 \times 10^{12}/\text{cm}^2$ to $8.1 \times$ 10¹²/cm². The average carrier density is approximately an order of magnitude lower than what has been previously reported for KTO(110) or KTO(111). At these densities, we approach the antiadiabatic regime,³⁶ where the Fermi energy is comparable or smaller than all known phonon modes (TO, LO) in KTO, which may attribute to the low T_c and B_{c2} of this device. The mobility μ increases significantly when the gate voltage is increased from -20 to +10 V and saturates when $V_{\rm bg}$ > 10 V. This may occur due to the improved screening of disorder potential at higher densities. Normalized resistance versus temperature plots are shown in Figure 3C, where blacked dashed line at $R = R_{\rm N}/2$ is used to define $T_{\rm c}$. Extracted T_c increases monotonically with increasing n_{2D} (Figure 3D), providing evidence that the device is in the underdoped regime. The exact mechanism for superconductivity and the increase of T_c with n_s is still not yet established, although there is a theory proposed in ref 37 to explain this phenomenon. We note that at T = 140 mK there is a crossing between the R versus T curves at $V_{bg} = 0$ V and $V_{bg} = -9$ V in Figure 3C, which may be due to enhanced proximity of the electron gas to the interface at $V_{\text{bg}} = -9 \text{ V.}^{37}$ Figure 3E shows an intensity plot of dV/dI as a function of V_{bg} and I at T=50mK and B = 0 T. The critical current (black dashed line) increases monotonically with increasing $V_{
m bg}$. We note during the I-V measurement in Figure 3E, the device experiences a significant "shift" compared to what is shown in Figure 3A–C, which is due to the hysteretic effect under backgating (details in Figure S4). Such hysteretic behavior is commonly observed in LAO/STO systems, which is explained by the transfer of mobile charges into trapped states during the first positive ramp of backgate (often referred as the "forming step"). 38-40 There is no other report so far on gate-induced hysteresis in KTO systems, but we believe a similar mechanism applies, although the origin of the trapped states requires further investigation. Regions that have not been exposed by ULV-EBL remain insulating up to the largest back gate voltages applied, as verified by two-terminal I-V measurements between electrode 5 and 4 at V_{bg} = +45 V (Figure S5).

It should be noted that Device A is parallel to the [001] crystallographic direction of this 3 nm LAO/KTO(110) sample (Figure 1F). To study if there is any in-plane anisotropic transport, we performed low-temperature measure-

ments on Device D, which is patterned at the same ULV-EBL canvas, while parallel to the [110] crystallographic direction (Figure S6). We also studied another pair of devices: Device E and F with perpendicular directions (Figure S7), which is located ~1 mm away from Device A and D. Along both crystallographic directions, we did not observe any resistance upturn prior to the superconducting transition, which was reported by ref 15 in KTO(111) samples. At T = 50 mK, Device D (parallel to $[1\overline{10}]$) has a residual resistance that is higher than Device A (parallel to [001], patterned at the same canvas). A similar phenomenon is observed in Device E and F, but this type of anisotropy is qualitatively different from the anisotropy reported in ref 15. To the best of our knowledge, there is no report of stripe phase in KTO(110) samples yet. It is therefore too early to draw conclusions about possible anisotropy and how it shows up in mesoscopic and nanoscale devices. Our devices are also quite different in that they are defined electrostatically rather than through subtractive lithography methods or macroscopic Van der Pauw configurations. $^{15-17}$ In addition, the electron density of our devices is significantly lower than what was reported in ref 15. We are not currently able to access carrier densities needed for direct comparison, but we believe anisotropy in transport is important for future investigations of both KTO(110) and KTO(111) devices.

Low-temperature transport properties of c-AFM-lithography-patterned devices on LAO/KTO(110) are also studied. For a device written on the c-AFM canvas surrounded by Ti/ Au electrodes (Figure S8A,B), the measured two-terminal resistance increases with decreased temperature, whereas the four-terminal resistance stays roughly the same (Figure S8C), indicating poor contacts between LAO/KTO 2DEG and Ti/ Au electrodes. From the Arrhenius plot of the two-terminal conductance, we can extract a Schottky barrier height around 45 meV (Figure S8D). We are able to avoid the Schottky contact issue by contacting the LAO/KTO 2DEG with aluminum wirebonds, similar to ULV-EBL canvases. However, the AFM tip cannot directly sketch on aluminum wirebonds due to the drastic height difference (>2 μ m) and its long distance apart (\sim 100 μ m). Thus, we first expose the two rectangular regions (marked in blue, Figure S9A) near the wirebonds by ULV-EBL to make the interface down below conducting. During the following c-AFM lithography step, the AFM tip only needs to rasterize the green main channel in Figure S9B without the need to touch the wirebonds. During c-AFM lithography, two-terminal conductance between the two wirebonds increases from 0 to $G_{2T} \approx 3 \mu S$ (Figure S9C). The device is then cooled down to 50 mK in a dilution fridge, where it remains metallic and shows a sharp resistance drop below 1 K (Figure S9D), which is an indication of a superconducting transition. We note that we can not exclude the possibility of the EBL-exposed region (marked in blue, Figure S9A) causing the superconducting transition. Thus, further four-terminal measurements are needed to confirm the superconductivity of c-AFM-patterned devices. We believe the material growth determines the underlying properties of the 2DEG, while c-AFM and ULV-EBL enable us to create devices with interesting shapes and mesoscopic dimensions.

We also demonstrate a quasi-one-dimensional conducting channel at the LAO/KTO(110) interface created by ULV-EBL. Prior to ULV-EBL writing, the sample is left in ambient conditions for 1 week to allow previously written conducting patterns to decay, thus restoring the insulating interface (<1 nS

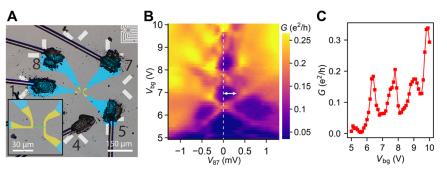


Figure 4. Transport measurements on a quasi-1D nanowire Device B. (A) Nanowire device design. Inset: zoom-in view of the nanowire. (B) Differential conductance dI/dV versus V and V_{bg} showing evidence for discrete charging of islands. The white arrow line shows the size of Coulomb diamond \sim 0.3 mV. (C) Line-cut showing resonant tunneling peaks.

between electrodes). The layout of the device ("Device B") is shown in Figure 4A. The blue-shaded region is exposed three times with an aerial dose of 10 μ C/cm², while the yellow region is exposed six times with 10 μ C/cm² dose. The main channel (Figure 4A inset, green) consists of a single line that is 16 μ m long, exposed 40 times with linear dose of 50 pC/cm. The resolution of ULV-EBL writing is reported to be comparable to c-AFM lithography, 30 so we estimate that this nanowire device has a width comparable to what is measured by c-AFM lithography ~20 nm.

As $V_{\rm bg}$ increases from 0 V, differential conductance ${\rm d}I/{\rm d}V$ versus $V_{\rm bg}$ measured at T = 50 mK shows a sequence of diamond-shaped low-conductance regions (Figure 4B). The zero-bias conductance (Figure 4C) shows a series of conductance peaks as a function of $V_{\rm bg}$, with a factor of 2.5 difference between adjacent peaks and bottoms. The overall characteristic strongly resembles the behavior of a singleelectron transistor, except that there is no artificially defined island. Rather, it is more likely that the disorder potential has produced a landscape where resonant tunneling through a quasi-zero-dimensional island dominates the overall transport. The electron addition energy is $\Delta E = 0.3$ meV (Figure 4B), and the irregularity of the peak spacing indicates that orbital energy spacings are comparable with Coulomb charging energy, as with LAO/STO. According to $\Delta E = e^2/C$, we can estimate the capacitance of the randomly formed Coulomb island to be in fF range. Further experiments are needed in order to effectively create, manipulate, and utilize quantum dots at the LAO/KTO interface and to deliberately create single-electron transistors and ballistic quantum channels, similar to what has been demonstrated in LAO/STO. ^{24,25} Furthermore, charging of these islands may indicate a state of electron pairing without superconductivity.²⁴ Here, no evidence of such a pairing transition is reported, but more samples and devices with different growth conditions, ULV-EBL dose, device dimensions, device orientations, and so forth, are yet to be explored.

C-AFM lithography and ULV-EBL have also been tested with the LAO/KTO(111) heterostructures. An intrinsically insulating 6 nm LAO/KTO(111) interface was created by PLD. Similar to LAO/KTO (110), we can use c-AFM lithography to write and erase conductive channel at the interface of this sample (Figure S10A–C). The width of the nanowire is extracted to be 17 nm (Figure S10C). ULV-EBL is performed on another intrinsically insulating 3 μ m LAO/KTO(111) sample to create Device C (Figure 5A,B). This device is metallic down to ~2 K but does not go superconducting (Figure 5C). At T=1 K, Hall measurements

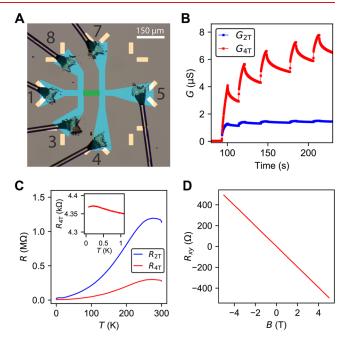


Figure 5. Device C patterned by ULV-EBL on 3 nm LAO/KTO(111) sample. (A) Layout of Device C. The blue region is exposed by a total aerial dose of 50 μ C/cm². Then the green main channel is exposed five times, each time with an aerial dose of 10 μ C/cm². The main channel has width $w=30~\mu$ m and length $l=85~\mu$ m. (B) Measured two-terminal and four-terminal conductance: $G_{2T}=I_{15}/V_1$ and $G_{4T}=I_{15}/V_{87}$ during exposure. (C) Resistance versus temperature of the device depicted in (A). Inset: zoomed-in plot of R_{4T} versus temperature below 1 K. (D) Hall resistance versus magnetic field measured at T=1 K, giving a 2D carrier density $n_s=6.3\times 10^{12}/\text{cm}^2$.

give a carrier density $n_{\rm s}=6.3\times10^{12}/{\rm cm^2}$ (Figure 5D). The lack of superconductivity of this particular LAO/KTO(111) device can be ascribed to many factors, such as growth condition and nonoptimal ULV-EBL dose, and so forth. More trials and optimizations are needed to conclude whether microdevices or nanodevices created at LAO/KTO(111) interfaces can turn superconducting, as well as their similarities and differences compared to the LAO/KTO(110) devices. Connecting or overlapping with existing reports made on macroscopic devices would also be worthwhile.

In summary, we have demonstrated nanoscale control of the metal—insulator transition in LAO/KTO(110) and LAO/KTO(111) heterostructures, using two different techniques: c-AFM lithography and ULV-EBL. The devices which survive to

milli-Kelvin temperatures exhibit key signatures of superconductivity that are tunable with a back-gate voltage. A quasi-one-dimensional conducting channel is conductive to milli-Kelvin temperatures and exhibits signatures of single-electron-transistor (SET) behavior.

In terms of device patterning, each of these two techniques has its own strengths. ULV-EBL is able to create large 2D patterns quickly, while c-AFM lithography has the ability to erase locally, which is suitable for making nanoscale barriers. Both techniques offer a wealth of insight into the nature of the superconducting state, based on prior experiments performed with LAO/STO. In addition, the unique differences, that is the lack of a bulk structural phase transition and the significantly larger spin—orbit interaction strength, will help improve our understanding of how superconductivity arises with such dilute carrier densities and potentially create new families of quantum devices that can exploit these properties.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c00673.

Materials and methods and additional Figures S1-S10 (PDF)

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Author Contributions

J.L. and A.B. supervised the experiments. C.L., X.Y., Q.D., and D.F. performed the sample growth. M.Y., D.Y., and P.I. performed c-AFM lithography, ULV-EBL, and transport measurements at low temperature. M.Y. analyzed the data. All authors discussed the results and commented on the manuscript.

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Notes

The authors declare no competing financial interest.

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