A Dual-Channel High-Linearity Filtering-by-Aliasing Receiver Front-End Supporting Carrier Aggregation

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***Abstract*— A filtering-by-aliasing (FA) receiver front-end based on a slice-based time-varying architecture was described by Bu and Pamarti (2021). Unlike prior FA architectures, it demonstrated, using a 28-nm CMOS prototype IC, a time-invariant input impedance that enables dual-channel operation with high linearity. Up to 50-dB stopband rejection with a transition bandwidth (BW) of only 3.2 times the RF BW, out-of-band IIP_3 of +35 dBm, blocker 1-dB compression point of +12 dBm, and local oscillator (LO) leakage power better than −81 dBm were achieved, using a 0.9-V supply. This article elaborates on the design of this prototype, presents detailed analyses of the slice-based architecture, and shows how it addresses many of the prior FA receivers' problems.**

***Index Terms*— Carrier aggregation (CA), finite-impulse response (FIR) filtering, high-linearity receiver front-end, multi-channel receiver, periodically time-varying (PTV) circuit, programmable receiver, sampled PTV circuit, software-defined radio.**

I. Introduction

THE exploration of highly programmable surface acoustic wave (SAW)-less transceivers for emerging software-defined and cognitive radio applications [1], [2] has been an ongoing effort for many years. Several recent approaches, such as the *N*-path filters (NPFs) [3] and mixer-first receivers [4], have shown promising performance in terms of noise, filtering, and linearity, while maintaining reasonably good tunability of local oscillator (LO) frequency and bandwidth (BW). A noise figure (NF) as low as 2 dB has been demonstrated in [5]. Filters whose equivalent baseband filters are at least of second-order have been successfully realized in [6] and [7], while [8] has even shown an out-of-band (OOB) IIP_3 as high as +44 dBm using bottom-plate mixing in NPFs. However, they typically use 1.2 V or higher supply voltages to improve linearity even in advanced nodes such as 28-nm CMOS, where the core voltage is only 0.9 V. Their LO leakage power is generally larger than −70 dBm, not compliant with the Federal Communications Commission (FCC) requirement [9].

On the other hand, due to the demand for high data throughput and the scarcity of wide contiguous spectral bands in the sub-6-GHz spectrum, programmable receivers that can support carrier aggregation (CA) are also highly demanded. Unfortunately, conventional *N*-path mixer-first approaches cannot be readily extended to support CA. This is because while a single-channel *N*-path structure presents 50-Ω input impedance at the carrier frequency to achieve impedance matching, it presents low impedance at other non-harmonic frequencies. When two or more mixer-first receivers with different LO frequencies are connected in parallel, the resultant impedance is always low across all frequencies. It thus cannot be used to receive more than one channel concurrently. Several techniques have been proposed to overcome this problem [10]–[13]; however, almost all of them require a low-noise amplifier (LNA) at RF, which limits the linearity [typically <10-dBm OOB IIP_3 and <0-dBm blocker 1-dB compression point (B_{1dB})]. Even the purely mixer-first one [13], albeit using modulated clocks, still demonstrates only ∼15-dBm OOB IIP_3 and ∼5-dBm B_{1dB}, which is lower than what a single-channel mixer-first receiver can achieve (typically >20-dBm OOB IIP_3 and ∼10-dBm B_{1dB}).

Recently, the filtering-by-aliasing (FA) concept has been developed and used in receiver and spectrum scanner designs [14]–[18]. Fig. 1(a) shows a simplified block diagram of an FA receiver [16]. Essentially, the time-invariant resistor in an active *RC* integrator is replaced by a periodically time-varying (PTV) one. The operation is equivalent to an analog finite impulse response (FIR) filter, whose impulse response is controlled by the PTV resistor variation, followed by sampling. The frequency conversion enables bandpass filtering and is realized using passive mixers like in most mixer-first designs. Very sharp filtering, e.g., over 48-dB stopband rejection (A_{stop}), has been demonstrated in a single FA stage [16] and 70-dB A_{stop} in a time-interleaved [17] FA receiver. However, FA receivers present a time-varying input impedance that presents multiple problems. It can be matched to the antenna [16], but parasitics at RF and reactance from the source interact with it and degrade filter shape. In addition, it makes parallel multi-channel realization (e.g., for CA) difficult without careful co-design. In addition, their OOB linearity is not better than the conventional mixer-first receivers.

Manuscript received April 26, 2021; revised August 2, 2021; accepted September 4, 2021. Date of publication September 22, 2021; date of current version April 25, 2022. This article was approved by Associate Editor Danielle Griffith. This work was supported in part by the National Science Foundation under Award ECCS 1810268 and in part by the Qualcomm Innovation Fellowship and the Broadcom Foundation Fellowship programs. *(Corresponding author: Shi Bu.)*

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Color versions of one or more figures in this article are available at https://doi.org/10.1109/JSSC.2021.3112183.

Digital Object Identifier 10.1109/JSSC.2021.3112183

In [19], we presented a slice-based FA architecture offered time-invariance input impedance, which supports CA, and demonstrated high linearity (>+35-dBm IIP_3) and low leakage (<−81-dBm LO leakage). This article elaborates on the design of the slice-based FA receiver together with supporting theoretical analyses on filtering, linearity, and noise. Section II details the problems of the conventional FA receiver designs. Section III explains the proposed slice-based architecture in detail and shows how it resolves some of these problems. Section IV describes the dual-channel implementation with the proposed FA architecture. Detailed circuit implementation is presented in Section V, followed by measurement results in Section VI. Finally, relevant conclusions are drawn in Section VII.

II. Limitations of Prior FA Receivers

A. FA Receiver in the Presence of RF-Node Reactance

Consider again the representative FA receiver shown in Fig. 1(a) [16], where Z_p represents the reactive part of the antenna impedance and inevitable parasitics due to the board, bond pads, bond wires, etc. With a purely resistive source impedance, R_s, the FA filter's impulse response is [16]

$$g(\tau) = \frac{1}{C[R_s + R(-\tau)]} \tag{1}$$

where $0 \le \tau \le T_s$. However, with Z_p, (1) is no longer accurate. Intuitively, at different frequencies, Z_p will siphon away different amounts of current from the time-varying $R(t)$, leading to a distorted $g(\tau)$ and hence filter degradation. Fig. 1(b) illustrates the effect by plotting the simulated filter magnitude responses, $|G(j\omega)|$,[1] without Z_p and with $Z_p = 10$ pF for an example bandpass filter centered at 500 MHz (with $C = 100$ pF, amplifier gain = 40 dB, $f_{LO} = 500$ MHz, and $T_s = 100$ ns). As is apparent, the filter transition BW has almost doubled. With Z_p more complicated than a simple capacitor, the filter shape degradation might be worse. Furthermore, since the knowledge of Z_p is imprecise (because it is a real-world reactance) and Z_p may vary substantially over time (as is common with many antennas), its effect on filtering can be unpredictable.

B. Problems With Multi-Channel Operation

Fig. 2 shows a naïve extension of the FA receiver concept to multi-channel operation, where $R_i(t)$ is the time-varying resistor in the ith channel. Even ignoring any input reactance, it is apparent that the current flowing into any one channel depends on $R_i(t)$s of all the channels. This may lead to corruption of each channel's filter shapes. In principle, careful co-design of $R_i(t)$s can recover the filter shapes but can be challenging in practice owing to mismatches and timing errors in realizing precise $R_i(t)$s.

C. Linearity Issues

FA receivers demonstrated better close-in linearity than much of the other prior art [17],[2] but the linearity needs to be

[1] $G(j\omega)$ is the Fourier transform of $g(\tau)$.

[2] This is because FA filters do not use a feedback resistor to define the gain, but the capacitance C, whereas the BW is set by T_s. This decouples FA filter's gain and BW, and typically the required C for a 10-MHz BW FA filter with 10–20-dB gain is large. Therefore, the close-in linearity is better.

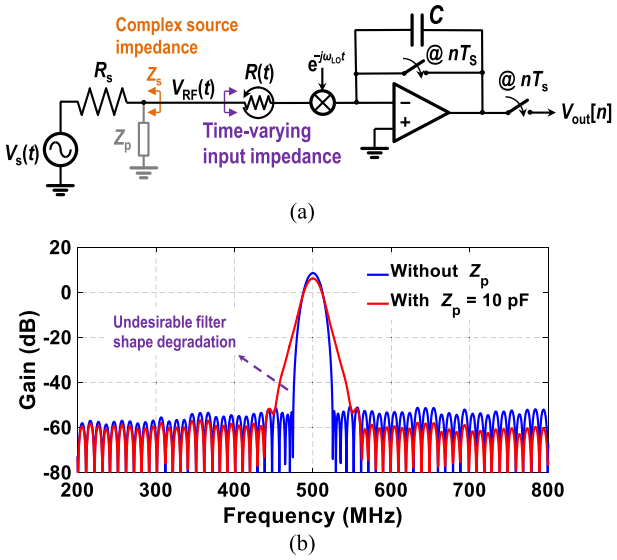

Fig. 1. (a) Prior FA receiver front-end with sampling period of T_s [16] in the presence of Z_p and (b) effect of Z_p on the attainable filter.

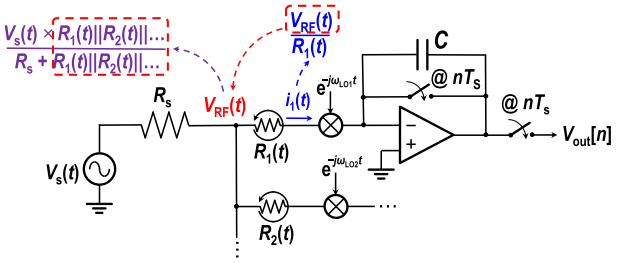

Fig. 2. Prior FA receiver front-ends in parallel for multi-channel operation.

further improved, especially at high offset frequencies. Consider the implementation of the PTV resistor using a resistor DAC (RDAC) [15]–[18] as shown in Fig. 3. A bank of resistors is placed in series with transmission gate switches controlled by a digital control code (B_0, B_1, ..., B_{M-1}). A small ratio of switch ON resistance to the physical resistor reduces the signal swings across the switch transistors resulting in reasonably high linearity. In [17] and [15], about +25- and +33-dBm OOB IIP_3 were achieved with $R_{sw,unit}$:R_{unit} = 1:4 and 1:10, respectively (all at 1.2-V supply). Reducing the ratio further is impractical since the large transistors introduce too much parasitic capacitance with attendant degradations of filter shape, S_{11}, etc. As such, the switch transistors present directly in the signal path can limit the linearity of the overall receiver. Mixer switches also contribute their own nonlinear currents but are less of a problem.

D. Residual Aliases

Since FA combines filtering and sampling into a single structure, any undesirable signals that are insufficiently filtered can alias back onto the desired signal. This is unlike in the mixer-first approaches where subsequent stages can provide additional filtering. Even with up to 70-dB A_{stop} reported by FA [17], residual aliases from very strong blockers pose a fundamental challenge to FA receivers. This remains an unsolved problem.

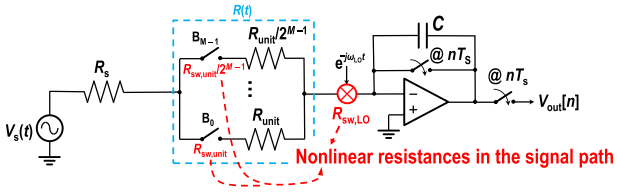

Fig. 3. Linearity limitation of prior implementation of FA receivers due to nonlinear switches in the signal path.

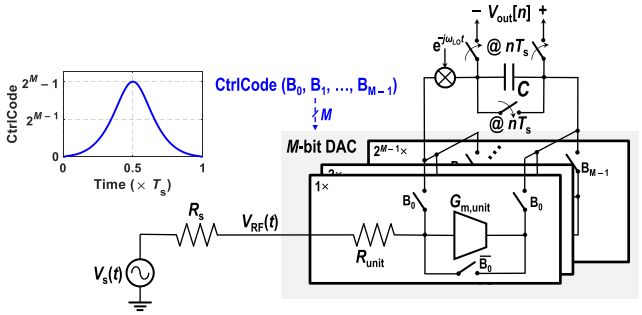

Fig. 4. Proposed slice-based FA architecture, where the G_m cells are integrated with the resistor in each slice, and switches are all moved within the feedback network.

E. Noise

The noise performance of FA receivers is generally slightly worse than the mixer-first ones, mainly because of the $R(t)$ variation and aliased noise from the source. To perform sharp filtering, the required $R(t)$ may be larger than 50 Ω for much of the period, T_s, leading to slightly more than 3-dB NF due to $R(t)$ alone. This part of NF deterioration can be improved using PTV noise cancellation techniques [18], but at the expense of degraded linearity. In addition, since the FA filter, $g(\tau)$, is not an ideal brick-wall filter, the source noise at frequencies outside the band folds in after sampling, albeit being attenuated. This in general adds another 1−2 dB to the average in-band (IB) NF, which is also inherent with FA.

III. Slice-Based FA Architecture

Instead of building the RDACs as shown in [15]−[18], Bu and Pamarti [19] proposed a slice-based FA architecture, where the DAC combines both the resistor and the baseband amplifiers, i.e., G_m cells, together in each slice, as illustrated in Fig. 4. No switches are present before the virtual ground created by the amplifiers in each slice, and all switches, including mixer switches, are moved into the feedback network. The switches are now, essentially, selection switches that either steer the current into the common integrating capacitor, C, or to the output of the G_m cells to form a unity-gain buffer, as illustrated in Fig. 5 for a single slice. An M-bit *CtrlCode* determines which slices, out of the total M binarily scaled ones, steer the current to C with the rest forming unity-gain buffers. As described in detail later, periodically varying the *CtrlCode* in time realizes the desired FA operation with the attendant sharp filtering.

As described below, the slice-based structure offers three major advantages: 1) constant input impedance while maintaining PTV operation, 2) linearity improvement, and 3) LO leakage suppression. The constant input impedance leads to easy multi-channel operation. A two-channel CA receiver implementation introduced in [19] will be detailed in Section IV. In the following, we analyze how the proposed architecture offers these benefits and solve the aforementioned problems with FA receivers at the expense of worsened noise performance. It is important to note that residual aliases mentioned in Section II-D remain a problem, and this work does not improve the performance in this respect. For certain applications, the achieved stopband rejection of ∼50 dB of this work might still be a problem.

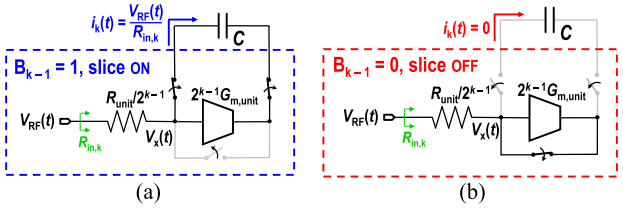

Fig. 5. Operation using the kth slice as an example when (a) the slice is ON and (b) the slice is OFF, where $R_{\text{in},k} = (R_{\text{unit}} + 1/G_{m,\text{unit}})/2^{k-1}$ to the first order.

A. PTV Operation and Input Impedance

Consider again Fig. 5, which illustrates the operation of the kth slice that is controlled by bit B_{k-1} in the *CtrlCode*, in both the ON and OFF states.[3] For simplicity, we assume here that the G_m cell is ideal. The input impedance of the kth slice is independent of whether the control bit, B_{k-1}, is 1 or 0. In fact, nominally, it is only dependent on the resistor and G_m, and it is equal to $(R_{\text{unit}}+1/G_{m,\text{unit}})/2^{k-1}$. This is because, regardless of the status of the slice, the G_m cell is always in negative feedback. In practice, the finite output impedance of the G_m cell has some small yet non-zero impact on the input impedance in the two states, but the effect is negligible as verified by simulations. Overall, independent of the *CtrlCode*'s value, the structure presents a constant, time-invariant input resistance of $R_{\text{in}} = (R_{\text{unit}} + 1/G_{m,\text{unit}})/(2^M - 1)$, which can be matched to R_s. Since both R_{in} and R_s are linear time-invariant (LTI), the overall impedance at the RF node also remains LTI even in the presence of reactance due to the antenna or parasitics.

Now consider the amount of current steered to the capacitor. The current from the ON kth slice to the capacitor is

$$i_k(t) = \frac{V_{\text{RF}}(t)}{R_{\text{in},k}} = \frac{2^{k-2}V_s(t)}{R_{\text{unit}} + 1/G_{m,\text{unit}}} \tag{2}$$

if the input of the receiver is matched to R_s. The current from the OFF kth slice to the capacitor, on the other hand, is zero. Therefore, the *CtrlCode* periodically changes the number of ON slices and hence the amount of current flowing into the capacitor over time. This enables the desired PTV operation just like the conventional FA filters.

The equivalent model of the proposed slice-based FA receiver is shown in Fig. 6(a). Essentially, at all times, t,

[3]For the proposed architecture, we call a slice ON if it steers current to C, and OFF if it does not.

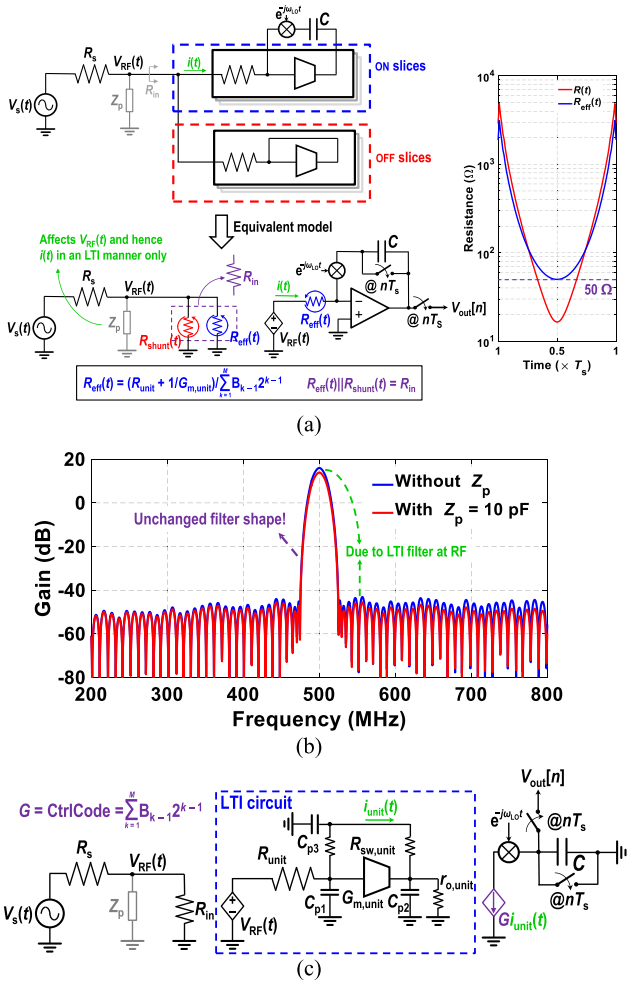

Fig. 6. (a) Equivalent model of the proposed slice-based FA receiver with an example of $R_{\text{eff}}(t)$, (b) effect of Z_p on the slice-based FA filter, and (c) alternative model of the proposed slice-based FA receiver for analyzing parasitics' effect on operation frequency.

the source is matched with an explicit resistor R_{in} that is time-invariant and $V_{\text{RF}}(t)$ is nominally half of $V_s(t)$. However, at time t, the ON slices, which account for an effective resistance of $R_{\text{eff}}(t)$, steer the current to the capacitor, whereas the OFF slices form a shunt resistor at the RF node,[4] $R_{\text{shunt}}(t)$, such that $R_{\text{eff}}(t)||R_{\text{shunt}}(t) = R_{\text{in}}$. Effectively, $V_{\text{RF}}(t)$ is processed by an equivalent FA filter with the PTV resistance, $R_{\text{eff}}(t)$. Note that the FA filter impulse response is now $g(\tau) = 1/(2CR_{\text{eff}}(-\tau))$. Recalling (1), we can see that $R_{\text{eff}}(t)$ should be a scaled version of $(R_s + R(t))$, to retain the same filter shape and achieve impedance matching. This is because R_{in} is formed by $R_{\text{eff}}(t)$ and $R_{\text{shunt}}(t)$ in parallel, hence $R_{\text{eff}}(t) \geq R_{\text{in}}$. To match R_{in} and R_s, the minima that $R_{\text{eff}}(t)$ can become is 50 Ω, whereas there is no such constraint in the prior FA approach [16]. Fig. 6(a) also shows an example of $R(t)$ used in the FA receiver of Fig. 1 and the corresponding $R_{\text{eff}}(t)$ needed in this work, to nominally realize the same FA filter shape. Note that the reactance at RF no longer sees any time-varying

[4]Another way to look at how the time-invariant input impedance is realized is that the ON slices realize a resistor of $R_{\text{eff}}(t)$, while the OFF slices create another resistor, $R_{\text{shunt}}(t)$ in parallel with $R_{\text{eff}}(t)$, and it follows that $R_{\text{eff}}(t)||R_{\text{shunt}}(t) = R_s$ if they are designed to match the source.

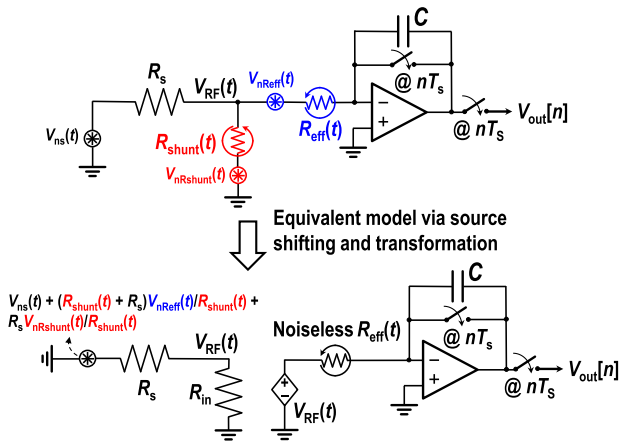

Fig. 7. Equivalent circuit for noise analysis in the baseband of the receiver.

resistance on the FA side, and hence the effect of it is the same as the conventional LTI front-ends. A filter is still formed at the RF node due to Z_p and $R_s||R_{\text{in}} = R_s/2$ if $R_{\text{in}} = R_s$. The PTV filter now simply acts on the LTI-filtered signal, $V_{\text{RF}}(t)$, instead of the original signal $V_s(t)$. Fig. 6(b) shows the filter shapes without Z_p and with $Z_p = 10$ pF, i.e., the same condition as that in Fig. 1(b). Apparently, the filter transition BW is intact, while the overall gain is gradually decreasing slowly as the frequency increases, due to the first-order RC filter at RF.

It is instructive to look at what limits the operational frequency of this architecture. The nature of the slice-based approach allows us to use simple LTI analysis to determine this. Consider a simplified model of the proposed FA receiver shown in Fig. 6(c), where the parasitics of the mixer and integrating capacitor are ignored for simplicity, and the other circuit parasitics are lumped into $C_{\text{p1}-3}$. Note that the time-varying aspect is confined to $G = CtrlCode$, the mixer, and the sampler, while the rest of the front-end, which represents the core of each slice, is an LTI circuit. Within the BW of this LTI circuit, $i_{\text{unit}}(t)$ is proportional to $V_s(t)$, and proper FA filtering can be achieved. Beyond the BW, $i_{\text{unit}}(t)$ starts getting filtered, and FA filtering is degraded.[5] In this work, large switches and unintended layout parasitics limit the BW, which is approximately estimated as $1/(r_{\text{o,unit}}\Sigma C_{\text{p1}-3})$ to the first order (here conservatively we consider the loop gain BW), where $r_{\text{o,unit}}$ is the output resistance of the unit G_m cell and $\Sigma C_{\text{p1}-3} \approx 0.5$ fF per unit slice, to about 1.3 GHz, and hence an operating frequency up to 1 GHz is chosen. More advanced nodes and careful layout help improve this frequency.

B. Baseband Filter Noise Performance

Although the proposed slice-based architecture does provide tolerance to reactance at the RF node due to its time-invariant input impedance, it comes with an NF penalty. This becomes apparent by input-referring the PTV resistor noise sources as shown in Fig. 7. Contrasting this with Fig. 1(a), it is easy to see that the NF of the proposed architecture will be worse than that in [16] because of two reasons. First, the noise source due to $R_{\text{eff}}(t)$ is effectively amplified by

[5]In reality, the ideally LTI circuit in Fig. 6(c) could still show certain PTV behavior, which causes extra filter degradations.

$(R_{\text{shunt}}(t)+R_s)/R_{\text{shunt}}(t)$, which is greater than unity. In other words, the smaller the $R_{\text{shunt}}(t)$, i.e., as more slices are OFF (unused for signal conduction), the more noise results. Second, the OFF slices themselves, i.e., $R_{\text{shunt}}(t)$, introduce some extra, though small, noise.

Mathematically, the corresponding NF caused by the baseband slice-based FA filter can be found by following the calculation method given in the Appendix of [18]. Note since we have input-referred all noise sources, the transfer function that these sources see is identical. The baseband noise factor is

$$F_{\text{baseband}} = 1 + \frac{\int_{t=0}^{T_s} dt/R_{\text{eff}}(t)}{R_s \int_{t=0}^{T_s} dt/R_{\text{eff}}^2(t)} + \left(2R_s + \frac{R_s^2}{R_{\text{in}}}\right) \frac{\int_{t=0}^{T_s} dt/[R_{\text{shunt}}(t)R_{\text{eff}}(t)]}{R_s \int_{t=0}^{T_s} dt/R_{\text{eff}}^2(t)}. \quad (3)$$

Here, the excess noise factor $\gamma = 1$ is assumed. If $R_{\text{eff}}(t) = R_s$ and $R_{\text{shunt}}(t)$ is infinity, then $\text{NF}_{\text{baseband}} = 3$ dB, as expected for an LTI system. The switches' noise contributions are negligible. They degrade the total NF by less than 0.1 dB according to simulation and hence omitted in our discussions. Comparing (3) with (13) in [16], we see that F_{baseband} of the slice-based FA is larger than the conventional FA because different $R_{\text{eff}}(t)$ is used, and an extra term, the last one, is introduced in (3) that further deteriorates the noise performance. The calculated $\text{NF}_{\text{baseband}} = 5.2$ dB, which is flat across the band. This is about 2 dB higher than that in [16], as expected. The contribution from the noise of $V_{\text{nRshunt}}(t)$ is small, about 0.3 dB only. A loose bound on the baseband NF can be found, since $R_{\text{shunt}}(t)_{\text{MIN}}$ is bounded to R_s, given by

$$F_{\text{baseband}} \le 1 + \left[1 + 2\frac{R_s}{R_{\text{shunt}}(t)_{\text{MIN}}}\left(1 + \frac{R_s}{2R_{\text{in}}}\right)\right] \times \frac{\int_{t=0}^{T_s} dt/R_{\text{eff}}(t)}{R_s \int_{t=0}^{T_s} dt/R_{\text{eff}}^2(t)}. \quad (4)$$

The second term is due to the noise of the receiver itself. In the case where $R_{\text{shunt}}(t)$ is not involved, i.e., $R_{\text{shunt}}(t) = R_{\text{shunt}}(t)_{\text{MIN}} = \infty$, the term in the square bracket is just 1. When finite $R_{\text{shunt}}(t)$ is added, $R_{\text{shunt}}(t)_{\text{MIN}} \ge R_s$. Then using $R_{\text{shunt}}(t) = R_s$, the term in the square bracket becomes 4. This means the penalty to the noise factor term contributed by the receiver will at most be worsened to 4× compared with without $R_{\text{shunt}}(t)$. As will be shown later in Section IV, the analysis here agrees with simulation and measurement well. Section IV describes how a two-channel implementation can reduce the impact of the OFF slices on NF and presents a complete noise analysis for the CA receiver.

C. Linearity Improvement

Moving the switches to within the feedback network brings a major advantage: owing to loop gain, nonidealities of the feedback network, both in terms of parasitics and nonlinearities, do not nominally matter. This can be seen from Fig. 5, where $i_k(t)$ only depends on R_{unit} and $G_{\text{m,unit}}$, and not on the feedback network's impedance, whether linear or nonlinear, which includes the switches' impedances. Essentially, to the first order, any nonlinear current generated will be greatly suppressed by the finite, but high, loop gain of the feedback.

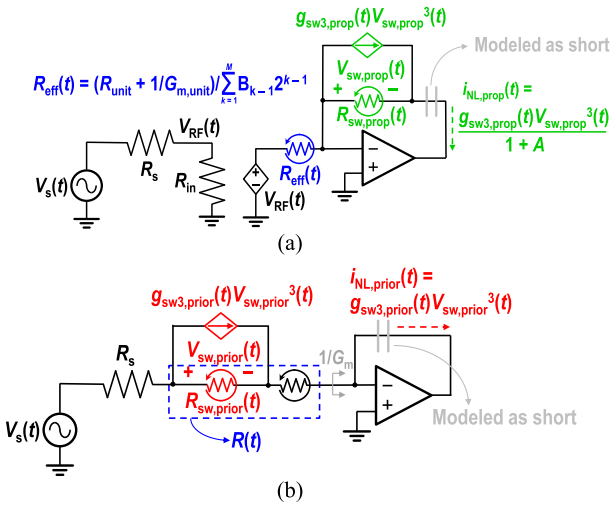

Fig. 8. Equivalent models for analyzing OOB switch nonlinearity in (a) slice-based FA receiver and (b) prior FA receiver.

1) Switch Nonlinearity: Its impact can be quantified using the simplified model shown in Fig. 8(a). $R_{\text{sw,prop}}(t)$ represents the total switch resistance of the ON slices. The switch nonlinearity[6] is modeled using a dependent current source of value, $g_{\text{sw3,prop}}(t)V_{\text{sw,prop}}^3(t)$, where $g_{\text{sw3,prop}}(t)$ is the total nonlinear conductance of all the ON slice switches at time t, and $V_{\text{sw,prop}}(t)$ is the voltage across the equivalent switch. For the sake of simplicity, the G_m cells are assumed perfectly linear and only OOB operation is considered, and accordingly, the capacitor is modeled as a short. Note that the ratio $R_{\text{sw,prop}}(t)$:$R_{\text{eff}}(t)$ is a constant, $R_{\text{sw,unit}}$:$(R_{\text{unit}} + 1/G_{\text{m,unit}})$, since both the resistors and the switches in each slice are similarly scaled. Similarly, $g_{\text{sw3,prop}}(t)R_{\text{sw,prop}}(t)$ is a constant set by the process technology and bias conditions. Fig. 8(b) shows a similar model for the prior FA receiver architecture [Fig. 1(a), [16]], where again, for OOB operation, the capacitor is assumed to behave as a short.

The slice-based architecture is much more linear than the prior FA architecture for two reasons. First, note that the introduced nonlinear current into the capacitor, $i_{\text{NL,prop}}(t) = g_{\text{sw3,prop}}(t)V_{\text{sw,prop}}^3(t)/(1+A)$, is suppressed by $(1+A)$, where $A = G_{\text{m,unit}}r_{\text{o,unit}}$ is the voltage gain of the G_m cells. A 20-dB voltage gain is typical. The second reason is subtler but more impactful. Note that in the slice-based architecture, the voltage swing across the switch is a time-invariant, scaled version of the input signal, expressed by

$$V_{\text{sw,prop}}(t) = V_{\text{RF}}(t)\frac{R_{\text{sw,prop}}(t)}{R_{\text{eff}}(t)} = \frac{V_s(t)}{2}\frac{R_{\text{sw,unit}}}{R_{\text{unit}} + 1/G_{\text{m,unit}}} \quad (5)$$

and can be reduced by a small $R_{\text{sw,unit}}$:R_{unit} ratio. In contrast, in Fig. 8(b), the voltage swing across the switch depends strongly on the PTV resistor, $R(t)$, given by

$$V_{\text{sw,prior}}(t) = V_s(t)\frac{R_{\text{sw,prior}}(t)}{R(t) + 1/G_m + R_s}. \quad (6)$$

[6]Only third-order nonlinearity is considered, but the discussion can be similarly extended to other orders of nonlinearity.

While $V_{\mathrm{sw,prior}}(t)$ is similar to $V_{\mathrm{sw,prop}}(t)$ for small $R(t)$, for large $R(t)$, $V_{\mathrm{sw,prior}}(t)$ can be significantly larger, e.g., for $G_{\mathrm{m}} = 125$ mS, $R(t)_{\mathrm{MIN}} = 16\ \Omega$, and $R_{\mathrm{sw,prior}}(t)$:$R(t) = 1$:5, which was used in [16], the swing across the switch can be about ~13 dB higher than in the slice-based architecture. Accordingly, the nonlinear current in Fig. 8(b), $i_{\mathrm{NL,prior}}(t)$, can be ~40 dB higher for parts of the PTV cycle. Overall, over the duration of the PTV cycle, the nonlinear current flowing into the capacitor in the slice-based architecture can be 20–60 dB lower than in the original FA architecture considering both effects. The exact improvement for a given $R(t)$ can be determined analytically by considering the ratio of the integrated error current over T_{s} in both the cases, given by

$$\frac{\int_{t=0}^{T_{\mathrm{s}}} i_{\mathrm{NL,prop}}(t)dt}{\int_{t=0}^{T_{\mathrm{s}}} i_{\mathrm{NL,prior}}(t)dt} = \frac{\int_{t=0}^{T_{\mathrm{s}}} g_{\mathrm{sw3,prop}}(t)\left[R_{\mathrm{sw,unit}}/\left(2\left(R_{\mathrm{unit}}+1/G_{\mathrm{m,unit}}\right)\right)\right]^3 dt}{(1+A)\int_{t=0}^{T_{\mathrm{s}}} g_{\mathrm{sw3,prior}}(t)\left[R_{\mathrm{sw,prior}}(t)/(R(t)+1/G_{\mathrm{m}}+R_{\mathrm{s}})\right]^3 dt} \approx \frac{\int_{t=0}^{T_{\mathrm{s}}}\left[R(t)_{\mathrm{MIN}}/(2R_{\mathrm{s}})\right]^3 dt/R_{\mathrm{eff}}(t)}{(1+A)\int_{t=0}^{T_{\mathrm{s}}} R^2(t)dt/(R(t)+1/G_{\mathrm{m}}+R_{\mathrm{s}})^3} \quad (7)$$

where, for simplicity, we assume $V_{\mathrm{s}}(t)$ is a constant since the models in Fig. 8 are not frequency-dependent, and $R_{\mathrm{sw,unit}}$ and $g_{\mathrm{sw3,unit}}$ are the same in both the approaches. Using $R(t)$ and $R_{\mathrm{eff}}(t)$ given in Fig. 6, (7) predicts about −52-dB less integrated nonlinear current, and hence 26-dB $\mathrm{IIP_3}$ improvement for the proposed architecture over prior FA implementation. Switch nonlinearity therefore becomes much less significant. Fig. 9 shows the behaviorally simulated OOB $\mathrm{IIP_3}$ for prior approach (limited by the RDAC, G_{m} nonlinearity introduces a difference of less than 1 dB at that linearity level) and this approach with switch nonlinearity only and a voltage gain of all G_{m} cells = 20 dB at an offset frequency of 82 MHz. Apparently, this approach is no longer limited by switch nonlinearities. The $\mathrm{IIP_3}$ improvement, ~28 dB, is very close to our previous calculation.

2) G_m Nonlinearity: Fortunately, this effect can be suppressed in a scalable manner. By increasing $G_{\mathrm{m,unit}}$, the virtual ground will be better and better, since $1/G_{\mathrm{m,unit}}$ is smaller and smaller compared with R_{unit}. The voltage at the input of the G_{m} cells, $V_{\mathrm{x}}(t)$ [see Fig. 5(a)], will be smaller and smaller as well for a fixed blocker power, because G_{m} cell and R_{unit} form a voltage divider for OOB blockers. The nonlinear currents, such as $G_{\mathrm{m3,unit}}V_{\mathrm{x}}{}^3(t)$, will also be much smaller, where $G_{\mathrm{m3,unit}}$ is the third-order transconductance of a unit G_{m}cell. Moreover, in this work, instead of using N baseband G_{m} cells for an N-path passive mixer, the mixer is implemented in the same manner as the selection switches in the DAC, both shown in Fig. 10. The currents are steered to N capacitors on a rotation basis to perform downconversion.[7] For the same power consumption of G_{m} cells, this work can enjoy N times larger G_{m} value than prior works, further enhancing the linearity. As also shown in Fig. 9, with G_{m} nonlinearity included, the slice-based approach still offers ~20 dBm $\mathrm{IIP_3}$ improvement. Here, as an optimal tradeoff among power, R_{unit} noise, and linearity, we choose a $G_{\mathrm{m,unit}}R_{\mathrm{unit}}$ value of about 15 in this work.

[7]The mixer architecture is essentially the same as the gain-boosted N-path filters [20], [21], but the motivation is not completely the same.

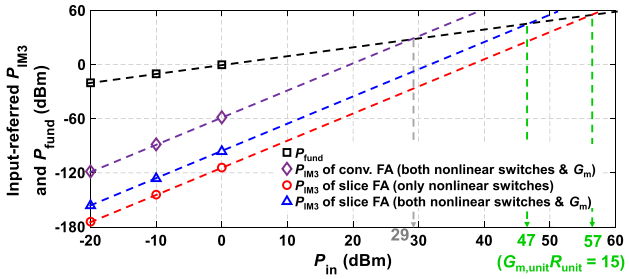

Fig. 9. Behavioral simulation results of input-referred P_{IM3} versus P_{in} for the prior FA approach (limited by RDAC nonlinearity), the proposed approach with only switch nonlinearities, and with both switch and G_{m} nonlinearities.

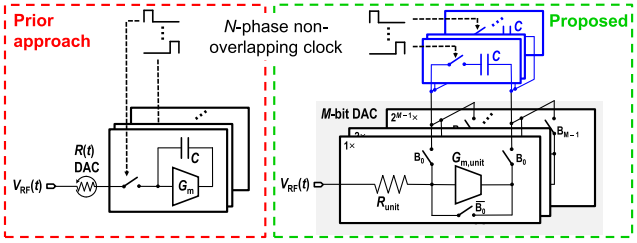

Fig. 10. Comparison between mixer implementations in the prior and proposed FA receivers.

D. LO Leakage Suppression

In receivers that use passive mixers without an upfront LN(T)A, various nonidealities, such as mixer switch mismatches, lead to undesirable leakage charge at the LO's fundamental frequency reaching the antenna [9]. For example, consider LO leakage in a conventional N-path mixer-first receiver. Fig. 11(a) shows a simplified model of LO leakage where $V_{\mathrm{LO}}(t)$, R_{drive}, and C_{eff} model the equivalent LO voltage source, mixer driver resistance, and an equivalent coupling capacitance that causes LO leakage, respectively. The LO leakage charge injected by the LO source is evenly split between the antenna and the amplifier since R_{in} is designed to match R_{s}. In contrast, the proposed architecture presents a high impedance on the antenna side (>100 Ω) and a low impedance on the amplifier side, R_{Gm}, as shown in Fig. 11(b). As a result, most of the leakage will not go to the antenna. A pessimistic estimate of the LO leakage reduction can be made by ignoring $R_{\mathrm{shunt}}(t)$ in Fig. 11(b), which would normally siphon away more of the LO leakage charge from the antenna. Now, the instantaneous LO leakage is determined by the relative magnitude of $(R_{\mathrm{eff}}(t) + R_{\mathrm{s}})$ compared with R_{Gm}, and the average LO leakage accordingly depends on the average of the former. The LO leakage reduction of the slice-based approach relative to the typical mixer-first receiver can now be shown to be

$$\frac{P_{\mathrm{s,prop}}}{P_{\mathrm{s,mixer\text{-}first}}} \approx \left(\frac{2R_{\mathrm{Gm}}}{R_{\mathrm{s}}+\mathrm{mean}[R_{\mathrm{eff}}(t)]+R_{\mathrm{Gm}}}\right)^2. \quad (8)$$

Note that R_{Gm} is ideally $1/G_{\mathrm{m}}$ at all frequencies, and in reality, $\sim 1/G_{\mathrm{m}}$ at non-zero offset frequencies from f_{LO} and ~30 Ω

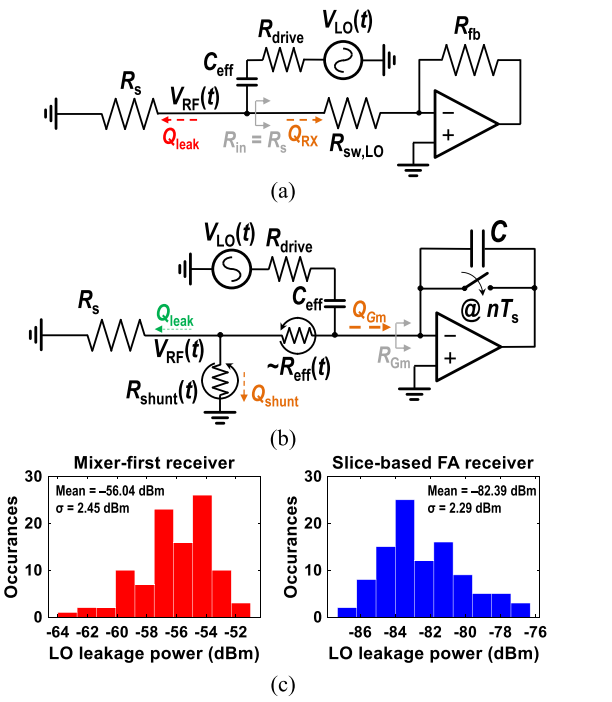

Fig. 11. Equivalent models for LO leakage in (a) mixer-first receivers, (b) slice-based FA receiver, and (c) histogram of 100-run Monte Carlo simulation results of LO leakage powers for a mixer-first receiver and the proposed FA receiver at $f_{LO} = 500$ MHz.

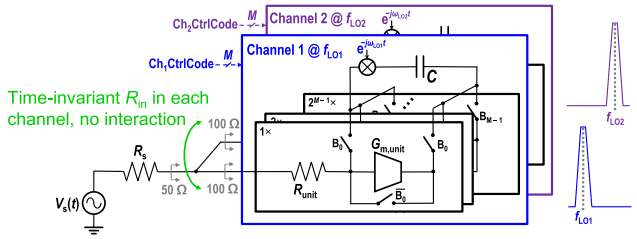

Fig. 12. Simplistic approach to realizing a two-channel receiver using the slice-based DACs by paralleling two single-channel DACs with scaled input resistances.

at f_{LO}, due to the equivalent Miller resistance of the capacitor under periodical reset. Using $R_{eff}(t)$ given in Fig. 6(a) and $R_{in} = 30\ \Omega$, ~22-dB reduction in leakage power is predicted by (8). This is validated by a 100-run Monte Carlo simulation of LO leakage at $f_{LO} = 500$ MHz in both a conventional mixer-first receiver and the slice-based FA receiver as shown in Fig. 11(c). In both the cases, the input impedances are matched to the source, and the same mixer and mixer driver sizes are used. As is evident, the mean of the LO leakage power of the proposed FA receiver front-end is less than −82 dBm, which has a reduction of about 26 dB compared with the mixer-first one, while the standard deviations are roughly the same.

IV. Dual-Channel Slice-Based FA Receiver

Using the proposed FA architecture, a naïve implementation of a two-channel FA receiver is depicted in Fig. 12, where two single-channel sliced-based DACs are placed in parallel. Given the time-invariant input impedance of the proposed approach,

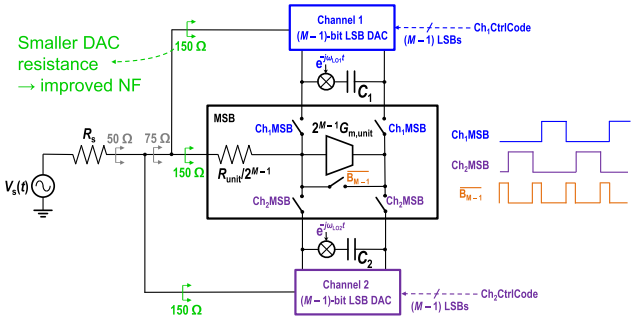

Fig. 13. Two-channel implementation with shared MSB and scaled down resistances to lower NF.

the two channels will concurrently receive signals with two different carriers without interaction.

However, note that in the naïve implementation, to guarantee 50-Ω impedance matching, each channel's R_{in} needs to be 100 Ω, resulting in about 4 dB higher NF than the single-channel case. To avoid this, the proposed dual-channel slice-based FA receiver uses dynamic reuse of one channel's OFF slices as the other channel's ON slices. In other words, instead of connecting an OFF slice of channel 1 in unity buffer configuration, and thereby wasting signal current, its current would be routed to the integrating capacitor of channel 2. Of course, if $R_{eff}(t)$ of channel 2, $R_{eff2}(t)$, is equal to the shunt resistance in channel 1, $R_{shunt1}(t)$, all wasted current of channel 1 will be reused by channel 2, and vice versa. However, this may not be possible to achieve, while simultaneously guaranteeing desired FA filter responses on both the channels. The proposed dual-channel FA receiver uses a good suboptimal solution, where we set $R_{eff2}(t) = R_{eff1}(t - T_s/2)$, where $R_{eff1}(t)$ is $R_{eff}(t)$ of channel 1. In addition, the MSB, which has the highest conductance among all slices, is shared between channels 1 and 2, as shown in Fig. 13. The MSB steers current to either channel 1's or channel 2's capacitor at a given time. When neither channel uses it, it forms a unity-gain buffer. Fig. 14 plots $R_{eff1}(t)$, $R_{eff2}(t)$, and the net effective shunt resistance at the RF node, $R_{shunt}(t)$, such that $R_{eff1}(t)||R_{eff2}(t)||R_{shunt}(t) = R_{in} = 50\ \Omega$ and matching is achieved. In this way, each channel presents effectively only 75-Ω input impedance, and parts of the shunt resistors in channels 1 and 2 are absorbed by the other channel to minimize the waste of source current. Note that this MSB sharing technique is only viable for the two-channel implementation and not scalable, unless the required filtering on the third channel is very relaxed. If more than two channels are desired, the extra channels will need to be added in the manner shown in Fig. 12, and the noise performance will degrade. Nevertheless, the proposed MSB sharing leads to an $NF_{baseband}$ of 7.9 dB, about 1.5 dB better than the naïve approach in Fig. 12. In this design, a slightly lower $NF_{baseband}$ of 7.6 dB is achieved by sizing down the slice resistances such that $R_{in} \approx 33\ \Omega$ targeting an S_{11} of −14 dB if no reactance were present at the RF node. This is simply a design choice and not fundamental to the architecture itself.

The NF of the complete receiver can then be readily calculated by accounting for contribution due to aliasing

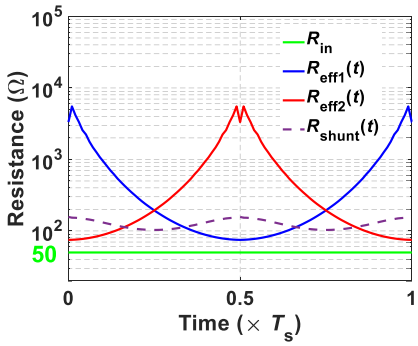

Fig. 14. Example of resistance variations over time for $R_{\text{eff1}}(t)$, $R_{\text{eff2}}(t)$, overall $R_{\text{shunt}}(t)$ due to two channels, and $R_{\text{in}} = R_{\text{eff1}}(t)||R_{\text{eff2}}(t)||R_{\text{shunt}}(t)$.

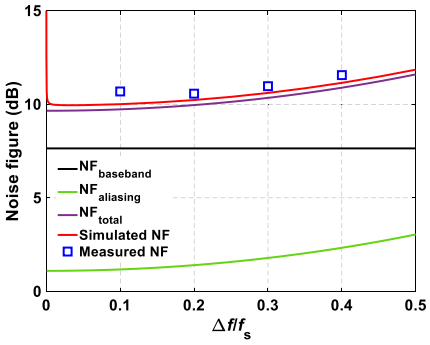

Fig. 15. Calculated NF for the receiver front-end and comparison with the simulated and measured results.

and four-path harmonic folding. Proceeding similarly as in [16]−[18]

$$\text{NF}_{\text{aliasing}}(\Delta f) = \frac{\text{PSD}_{\text{Rs}}(\Delta f)}{2kTR_s|G(\Delta f)|^2} = \frac{\sum_{n=-\infty}^{+\infty}|G(\Delta f + nf_s)|^2}{|G(\Delta f)|^2}$$
$$\text{NF}_{\text{harmonics}} = \frac{1}{\text{sinc}^2(1/4)} \approx 0.91 \text{ dB} \quad (9)$$

where $|\Delta f| \leq f_s/2$ is the IB offset frequency. The average IB NF_{alias} is about 1.8 dB, which is similar to prior FA works, as mentioned in Section II-E. Finally, the overall NF at a certain Δf for the complete two-channel system can be derived as

$$\text{NF}_{\text{total}}(\Delta f) = \text{NF}_{\text{baseband}} + \text{NF}_{\text{aliasing}}(\Delta f) + \text{NF}_{\text{harmonics}}. \quad (10)$$

The calculated NF_{total}, whose average across the band is about 10.3 dB, is shown in Fig. 15 together with the simulated and measured NFs for $f_s = 10$ MHz and $f_{\text{LO1}} = 500$ MHz (f_{LO2} is set to be 740 MHz). Both simulation and measurement agree with the calculation well, and the residual difference between simulation and calculation is due to parasitics.

V. Circuit Implementation

Fig. 16 shows the block diagram of the implemented dual-channel slice-based FA receiver front-end. The receiver front-end consists of only switches, inverter-based amplifiers, digital circuits, and passive devices (namely, resistors and capacitors). All switches are realized using equally sized PMOS and NMOS devices to minimize clock feedthrough and charge injection.

Each channel is realized by a four-path passive mixer and a 13-bit binary-weighted DAC using the slice-based architecture. This number of bits here is used to ensure that the DAC resolution does not limit filter shape [17]. The unit selection switches are designed to have a ratio of $R_{\text{sw,unit}}:R_{\text{unit}} \approx 1{:}10$, such that the linearity is not limited by switches. The bias of the receiver is set to about half of the supply voltage, V_{DD}, by resetting baseband amplifiers and OFF slices' self-bias. The DACs switch at a rate of $f_{\text{clk}}/2$, where f_{clk} is the frequency of an external clock signal. The effective PTV resistor variations in the two channels, $R_{\text{eff1}}(t)$ and $R_{\text{eff2}}(t)$, respectively, with a period of T_s, are also sketched in Fig. 16 to show how they are staggered to realize MSB sharing. The sampling and reset clocks are derived from the same f_{clk} signal. As discussed in Section IV, although this is not required, $R_{\text{eff2}}(t)$ is deliberately chosen to be an equal but shifted version of $R_{\text{eff1}}(t)$. This shift guarantees that $R_{\text{eff1}}(t)$ and $R_{\text{eff2}}(t)$ are never simultaneously low, allowing the MSB slice to be shared thereby saving power and area, and reducing the NF penalty from the OFF-slice shunt resistance. Also, it allows smaller area used for digital memory. This, however, also constrains the filter shapes of the two channels to be identical, and it is no longer possible to use different filter shapes in the two channels. The liberty of having different filter shapes in the two channels can be achieved using more digital memory to set $Ch_2CtrlCode$ separately and designing the two channels' impulse responses carefully to avoid overlapped usage of the MSB.

The integrating capacitors are realized in a ping-pong fashion to allow one capacitor integrating signal current while the other being read and then reset. They are tunable from 10 to 80 pF. The mixer switches are driven by two sets of 25% duty-cycled non-overlapping clock signals at f_{LO1} and f_{LO2}, respectively, to mix the RF current to baseband for integration. The mixer switches are designed to have a 4-Ω ON resistance. Note that f_{LO1} and f_{LO2} can be any value within the RF range from a functional perspective. The constrain mainly comes from the required sideband rejection, i.e., the rejection of the signal at the other channel's frequency at one channel's output, when operating with two channels.

A. Low-Noise Mode

The proposed operation of the FA receiver presents time-invariant input impedance and can therefore provide good filtering and high linearity, but it also leads to high NF (>10 dB), which is not preferred, especially when no strong blockers are present.[8] Therefore, in addition to the default high-performance (HP) mode that has been discussed so far, we also introduce an extra low-noise (LN) mode for the receiver front-end. This is done by disabling the switches that short the inputs and outputs of the G_m cells when the slices are OFF, i.e., $\overline{B_{k-1}}$, as shown conceptually in Fig. 17(a) using one of the channels. In the LN mode, the operation is very similar to the time-interleaved FA in [17], except the two paths have different LOs and their outputs are not summed. The second

[8]When no blockers are present, the NF requirement is more stringent, while when blockers are present, it may be relaxed [22], [23].

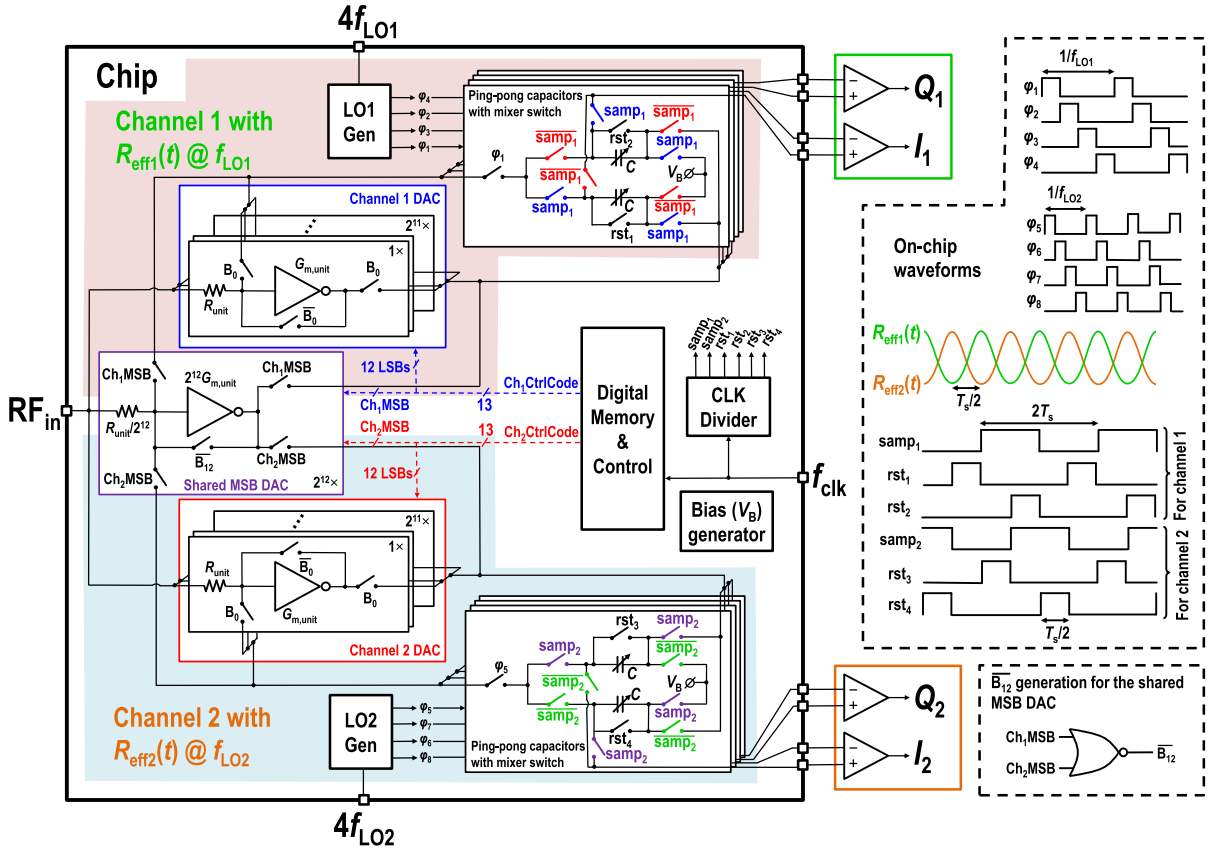

Fig. 16. Complete block diagram of the implemented receiver front-end.

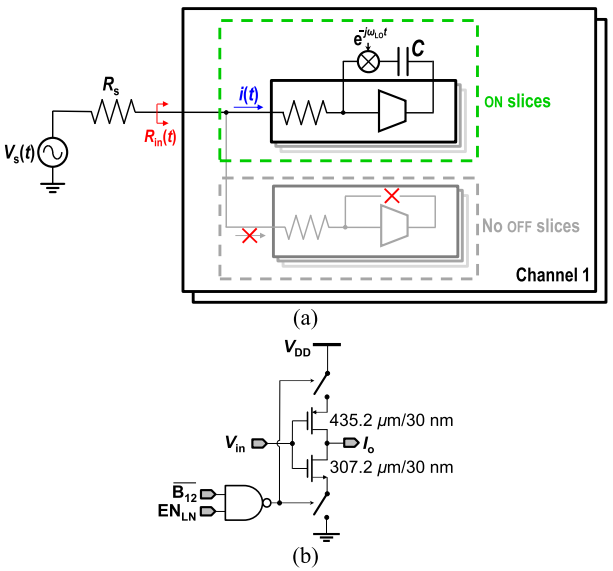

Fig. 17. (a) Operation principle of the LN mode and (b) schematic of the G_m cell in the MSB slice.

channel still presents itself like a shunt resistor to the first channel. However, as can be seen from the sketches of $R_{eff1}(t)$ and $R_{eff2}(t)$ in Fig. 16, the two resistances vary in a way that when one is high, the other is low, and vice versa. Their interaction is relatively weak, similar to [17]. This reduces $NF_{baseband}$ to about 5 dB, thus helping improve the NF by about 2−3 dB. The calculation for the LN-mode NF is almost the same as that in [17], except that the output noise power spectral density (PSD) is white as the outputs are not summed to realize time-interleaved FA filtering, so we omitted it here for brevity. However, some degradation (∼1−2 dB) compared with [17] is expected, since the minimum input resistance in [17] is $R(t)_{MIN} + R_{sw,LO} + 1/G_m \approx 30\ \Omega$, while it is about 50 Ω in this work. Adding few extra bits that are not used in the HP mode to lower the LN mode $R_{in}(t)_{MIN}$ will help in this regard (to achieve the same $R_{in}(t)_{MIN}$ as in [17]) but is not implemented on this chip. In the LN mode, the G_m cells in the OFF slices are powered down to save power by controlling switches at the inverter-based amplifiers' supply and ground, similar to the G_m cells in [18]. The schematic of the G_m cell in the MSB slice is shown in Fig. 17(b), where high-V_T devices are used to increase the gain and g_m/I_D efficiency, and those in the LSBs are binarily scaled from it. EN_{LN} is the control signal that enables power saving in the LN mode. Due to the lack of constant input impedance, some tradeoff in designing $R_{eff1}(t)$ and $R_{eff2}(t)$ for better noise performance, and the operation being less well behaved than the HP mode, the filtering, linearity, and some other metrics are expected to degrade slightly. Using an integrated blocker detector [24] or a spectrum scanner [15] to determine whether strong blockers exist, the HP or LN modes can be chosen for proper scenarios, respectively. Note that further NF improvement of close to

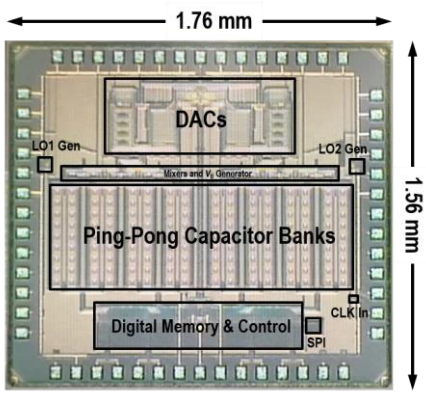

Fig. 18. Chip micrograph.

3 dB can be achieved using noise cancellation, which has been demonstrated in [18] for FA receivers, for both the HP and LN modes, at the expense of linearity, power, and silicon area.

VI. Measurement Results

The implemented test chip was fabricated in the TSMC 28-nm CMOS process. Fig. 18 shows the die photograph of the chip. The active area is 1.3 mm^2. The supply voltage of the whole chip is 0.9 V. At $f_{LO1} = 500$ MHz and $f_{LO2} = 740$ MHz, the entire chip consumes 50- and 42-mW power in the HP and LN modes, respectively. The DAC consumes 31-mA current in the HP mode and 22 mA in the LN mode. The digital control circuitry dissipates ~10 mA at a nominal f_{clk} of 2 GHz, regardless of the mode of operation. The frequency of f_{clk} is chosen to make the image of the filter passband caused by the sampled-and-held waveform of $R_{eff}(t)$ due to it being digitally controlled, driven by f_{clk}, suppressed by ~50 dB [16]. Each LO divider and its associated switch drivers consume about 11 mA/GHz. The sampled outputs are buffered externally on board for measurement. The DACs are dc calibrated at startup to account for mismatches of resistances in different slices.

Fig. 19(a) shows the measured single-channel 10-MHz BW filter responses in three different filter configurations (filters 1–3) with different transition BW and A_{stop} in the default HP mode. The transition BWs for filters 1–3 were 17, 22, and 31 MHz, respectively, while the achieved A_{stop} was observed to be better than 35, 45, and 51 dB, respectively. Fig. 19(b) shows the single-channel filter at different LO frequencies in filter 3 configuration, with zoomed-in views for the filter shapes around f_{LO} at the lower and higher ends of the LO range. Fig. 19(c) shows the filter shape at $f_{LO} = 170$ MHz. Like a four-path mixer-first receiver, the odd harmonics will fold in. The second-harmonic rejection was slightly worse than that in [16]. Fig. 19(d) and (e) shows the measured concurrent receiving two-channel filter responses with $f_{LO1} = 500$ MHz and $f_{LO2} = 520$ MHz, and $f_{LO1} = 330$ MHz and $f_{LO2} = 850$ MHz, respectively, in the HP mode. Fig. 19(f) shows the LN mode with $f_{LO1} = 500$ MHz and $f_{LO2} = 740$ MHz (for the frequency response at these LO frequencies in the HP mode, see figure 6.3.4 in [19]). It is observed that the stopband rejection was deteriorated to about 44 dB in the LN

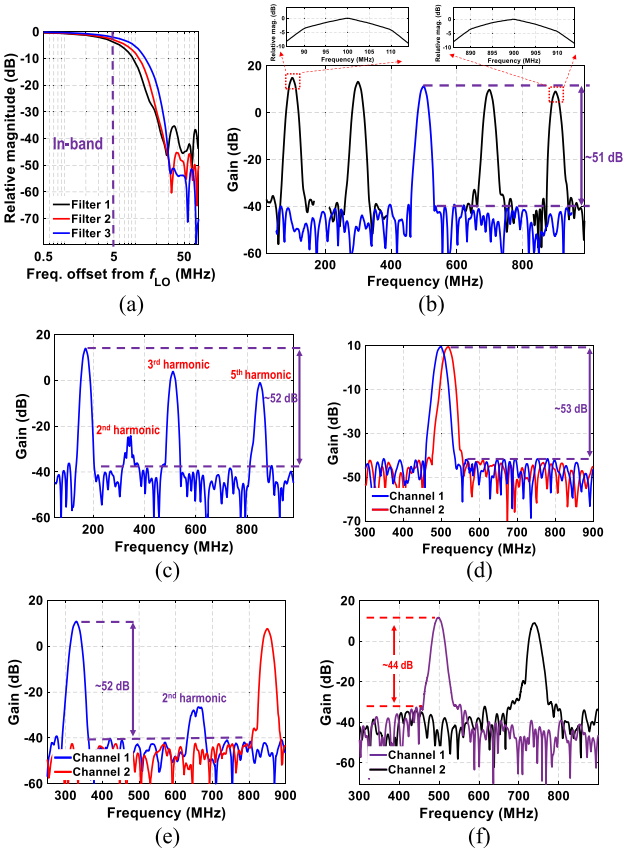

Fig. 19. (a) Measured single-channel 10-MHz RF BW filter responses in the HP mode, (b) single-channel filter 3 for different LO frequencies, (c) single-channel filter 3 at $f_{LO} = 170$ MHz, showing the harmonic responses, (d) concurrent receiving filter shapes in the HP mode at $f_{LO1} = 500$ MHz and $f_{LO2} = 520$ MHz, (e) at $f_{LO1} = 330$ MHz and $f_{LO2} = 850$ MHz, and (f) in the LN mode at $f_{LO1} = 500$ MHz and $f_{LO2} = 740$ MHz.

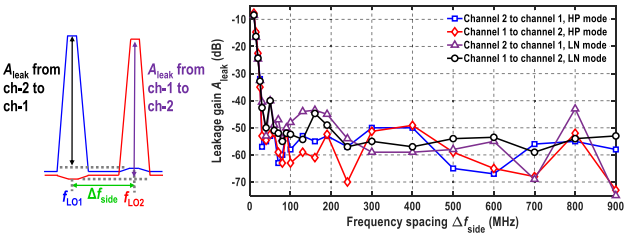

Fig. 20. Measured sideband leakage.

mode with worse filter shapes. The following measurements were performed with the same filter BW and LO frequencies as Fig. 19(f) unless otherwise specified.

The measured sideband rejection of both the channels in both the modes with different spacing between the two LO frequencies is depicted in Fig. 20. The measurement was performed by measuring one channel's output when the RF input frequency is close to the other channel's LO frequency. The sideband rejection is almost the same as the filter shape.

Fig. 21(a) shows linearity measurements for channel 1 with 10-MHz BW, $f_{LO1} = 500$ MHz, and $C = 80$ pF in both the modes. While IB IIP3 was measured to be about +12 dBm in both the modes, OOB IIP3 was about +35 dBm in the HP mode and about +27 dBm in the LN mode at an offset

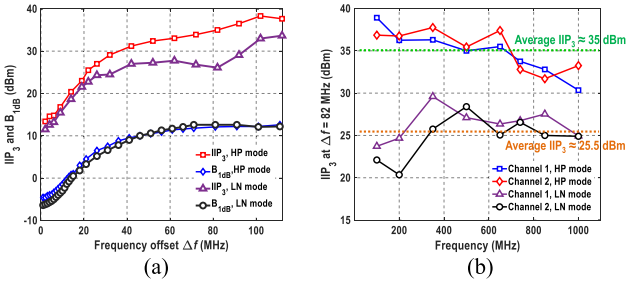

Fig. 21. (a) Measured IIP_3 and B_{1dB} of channel 1 at $f_{LO1} = 500$ MHz for different offset frequencies and (b) IIP_3 of both the channels at 82-MHz offset frequency for different LO frequencies, in both the modes.

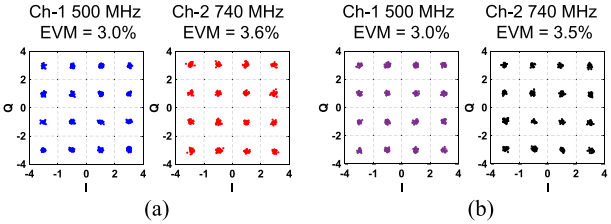

Fig. 22. Measured demodulated constellations of the two carriers in (a) HP mode and (b) LN mode.

frequency, Δf, of 82 MHz away from the corresponding channel's f_{LO}. In both the modes, B_{1dB} was better than $+12$ dBm at the same offset frequency. Fig. 21(b) shows the measured IIP_3 of both the channels in both the modes at $\Delta f = 82$ MHz at different LO frequencies. On average, IIP_3 was about $+35$ dBm in the HP mode and $+25.5$ dBm in the LN mode.

The receiver was further characterized with concurrently receiving error vector magnitude (EVM) measurements. Two different 2.5-MSps 16QAM modulated signals with $\alpha = 0.35$ were combined and fed to the input of the receiver. The power of each carrier is about -42 dBm at the input of the receiver, the power level of which is limited by the low gain of the front-end and the input-referred noise of the oscilloscope. The measurements were performed without IQ error calibration. The demodulated constellations in the two modes are shown in Fig. 22. The worst case EVM was 3.6% rms.

Fig. 24(a) shows the measured S_{11} in the two modes together with the simulation results. In the HP mode, S_{11} was better than -10 dB till about 2.3 GHz, partially confirming the achieved wideband input matching. At low frequencies, it was about -14 dB, as predicted by the designed input resistance. The dip at about 1.5 GHz is likely due to the reactance introduced in measurement, from measurement equipment, bond wire, board, etc. S_{11} was less well-behaved in the LN mode, but still better than -8.5 dB across the frequency of interest (0.1–1 GHz). Fig. 24(b) shows the worst case LO leakage power measured from three dies. In the HP mode, it was better than -81 dBm, and in the LN mode it was better than -68 dBm. The measured NF was 10.8 dB in the HP mode and 7.9 dB in the LN mode at 500-MHz LO. They were worsened to about 13.6 and 13.8 dB when a 0-dBm continuous-wave (CW) blocker was present at 60-MHz offset, as shown in Fig. 23(c). This is mostly due to the phase noise of the LO dividers, since the front-end itself is very linear. The

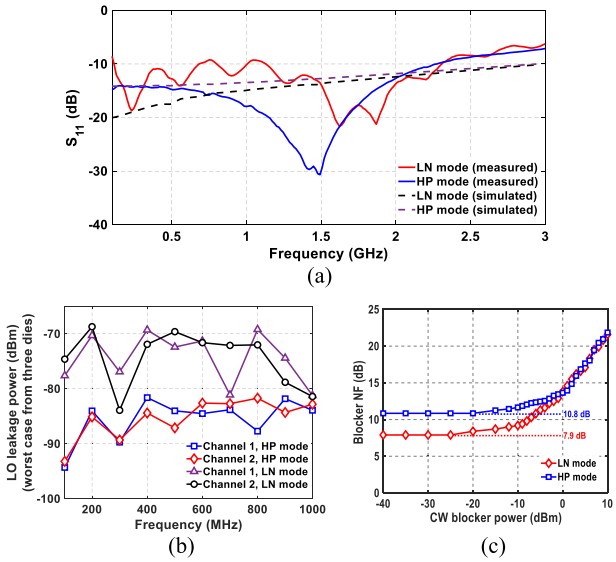

Fig. 23. Measured two-mode (a) S_{11}, (b) LO leakage at different LO frequencies, and (c) blocker NF in the presence of a CW blocker at $\Delta f = 60$ MHz for a 10-MHz RF BW filter with $f_{LO1} = 500$ MHz.

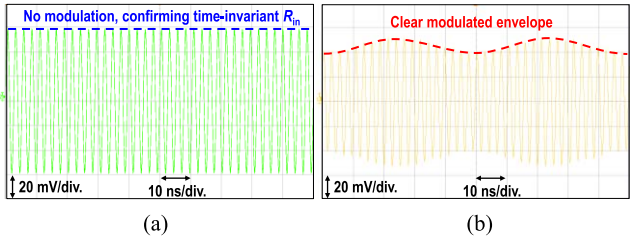

Fig. 24. Measured voltage waveform at the RF node of the receiver, $V_{RF}(t)$, when a sinusoidal signal at 380 MHz is injected to its input, in (a) HP mode and (b) LN mode.

linearity, S_{11}, and noise measurements did not vary appreciably between channels and configurations.

Since the signal processing is primarily done at RF in the proposed FA receiver, due to the presence of parasitics, the performance at higher carrier frequencies is in general worse than that at lower carrier frequencies. This is because the parasitics load the G_m cells and the virtual grounds are less well-behaved at higher LO. Metrics that depend on good virtual grounds would therefore suffer at higher carrier frequencies. It can be seen that for example, OOB IIP_3 degrades with higher LO frequencies. A few dB of NF degradation also appears at high LO frequencies, similar to the mixer-first ones [4]. Better layout and finer technology nodes would help reduce the parasitics and hence push the operational frequency higher.

As a final remark, a sinusoidal signal at 380 MHz was fed to the input of the receiver. Fig. 24 shows the voltage waveform at the RF node, $V_{RF}(t)$, of the receiver in the HP and LN modes, respectively, captured using an oscilloscope. Obviously, the LN mode shows clear modulation on the envelope of the waveform, while the HP mode has none. This helps confirm the achieved time-invariant R_{in} in the default HP mode.

Table I summarizes the performance of this work and compares it with the state-of-the-art single-channel receivers and NPFs, and multi-channel receivers. The implemented

TABLE I

PERFORMANCE SUMMARY AND COMPARISON WITH STATE-OF-THE-ART SINGLE- AND MULTI-CHANNEL RECEIVERS AND FILTERS

	Single-channel receivers/filters				Carrier-aggregation receivers			This work	
	[17] JSSC'18	[8] JSSC'19	[6] JSSC'19	[7] JSSC'20	[10] JSSC'15	[12] JSSC'18	[13] JSSC'21*	LN mode	HP mode
Architecture	TI-FA	*N*-path	*N*-path	*N*-path	Current-domain signal process.	Code-domain *N*-path	Multi-branch mod.-mixer-clock	Slice-based FA	
CMOS technology	65 nm	28 nm	65 nm	28 nm	65 nm	65 nm	65 nm	28 nm	
RF freq. (GHz)	0.1–1	0.1–2	0.8–1.1	0.2–2	0.5–3	0.5–1.4	0.3–1.3	0.1–1	
RF input	Differential	Differential	Differential	Single-ended	Differential	Differential	Differential	Single-ended	
BW (MHz)	2.5–40	13	30–50	18	1–30	2	10–66	5–20	
No. of channels	1				3	2	2	2	
Carrier spacing	N/A				<100	<700	200–600	30–900§	
A_{stop} (transition BW)	>58 (2.5× BW)	>47# dB (6× BW)	>17 (0.5× BW)	>27# (1.7× BW)	>30 (3× BW)	>28# (10× BW)	>60# (12× BW)	>44 (3.2× BW)	>51 (3.2× BW)
S_{11} (dB)	<–9	<–8#	<–7#	<–10#	<–10#	<–11#	<–6#	<–8.5	<–14
IB IIP_3 (dBm)	+8.2	+5#	+25	+1.5#	–28	–26	–6.9	+11.5	+13.4
OOB IIP_3 (dBm)	+24 (Δ*f*/BW = 6)	+44 (Δ*f*/BW = 12.3)	+24 (Δ*f*/BW = 1)	+33 (Δ*f*/BW = 4.4)	–4.8 (Δ*f*/BW = 4)	–15 (Δ*f*/BW = 10)	+16 (Δ*f*/BW = 12)	+25 (Δ*f*/BW = 8)	+35 (Δ*f*/BW = 8)
OOB IIP_2 (dBm)	+64	+90	+61	N/A	N/A	N/A	N/A	+71 (Δ*f*/BW = 8)	+82 (Δ*f*/BW = 8)
OOB B_{1dB} (dBm)	+12 (Δ*f*/BW = 6)	+13 (Δ*f*/BW = 12.3)	+9 (Δ*f*/BW = 1)	+12 (Δ*f*/BW = 4.4)	–1	–11.8	+4	+12.6 (Δ*f*/BW = 8)	+12.1 (Δ*f*/BW = 8)
LO leakage (dBm)	N/A	N/A	–45	N/A	N/A	N/A	N/A	<–68	<–81
Sideband rej. (dB)	N/A				N/A	35	>48	>43	>49
Supply voltage (V)	1.2/1	1.2/1	1	1.2	1.2/2.5	N/A	1.2	0.9	
Power (mW)	75–99	34–96	80–97	146.6–179	84/channel	18/channel	19.6/channel	16–27.5 /channel	21–31 /channel
NF (dB)	6.5–8.5	4.1–10.3	5.0–8.6	4.3–7.6	4.8	3.4–4.9	12.8–12.9	7.8–12.0	10.5–14.1
Gain (dB)	23	16	–4.2	13	50	38.5	53.2	12	10
Area (mm^2)	2.3	0.8	1.9	0.48	7.8†	0.31	1.8	1.3	

Estimated from reported data * High-linearity mode only † Including on-chip frequency synthesizer

§ For achieving a rejection of the other carrier by more than 40 dB. Otherwise, the spacing can be arbitrarily small till the two channels become adjacent.

prototype maintains the sharp filtering of single-channel FA, even in a dual-channel mode. The filter sharpness is close to that of [17] without using time-interleaving. Better S_{11} than [17] is also achieved. While the NF is worse than most of the other multi-channel receivers, it achieves an IB and OOB IIP_3 as high as +13 and +35 dBm, respectively, which are both close to 20 dB higher than prior multi-channel works. B_{1dB} of this work, which is better than +12 dBm, is at least 8 dB higher than the prior multi-channel receivers as well. The supply voltage is mere 0.9 V, which is the lowest among all. The overall performance is similar or even better than the single-channel ones. Note that the overall signal gain of this work is lower than prior art. Signal gain can be improved using additional baseband stages. The linearity of these additional stages is not critical due to the high rejection provided by the front-end. However, the relatively lower front-end gain means that baseband stages need to maintain a moderate noise performance in order not to degrade the overall NF. This would add to system power consumption but since the sampling rate is low, the additional power overhead is not expected to be high.

VII. CONCLUSION

In this article, we detailed a two-channel slice-based FA receiver front-end architecture. While maintaining its overall PTV operation to obtain sharp FA filtering, it presents a time-invariant input impedance, which is beneficial for both tolerance to RF-node reactance and multi-channel operation. All switches are moved into the feedback network, which greatly helps improve the linearity. With a 0.9-V supply, +35-dBm OOB IIP_3 and >+12-dBm B_{1dB} have been demonstrated. It also shows better than −81-dBm LO leakage power in its default HP mode.

ACKNOWLEDGMENT

The authors would like to thank Dinesh Alladi of Qualcomm Technologies, Inc. for valuable discussions. They also thank Rajasekhar Pullela and Pawan Tiwari of MaxLinear, Inc. for their help with the measurement. Sameed Hameed of Silvus Technologies, Inc., Jiyue Yang, Yan Zhang, Vinod Kurian Jacob, and Haris Suhail of UCLA are thanked for their assistance and help.

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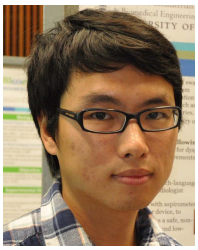

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