An FDD-based Full-Duplex Sub-THz Interconnect with Data-rate of 22.6 Gb/s and Energy-Efficiency of 1.58pJ/bit

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***Abstract*—A full-duplex sub-THz interconnect based on Frequency Division Duplex (FDD) scheme is proposed for high data-rate and bandwidth-density chip-to-chip communications. The system consists of a dual-band transmitter (TX), receiver (RX), and Si dielectric waveguide (DWG) channel that provides low in-band insertion loss (IL) and high isolation in the two adjacent frequency bands. A full-duplex measurement was set up with Pseudo Random Binary Sequence (PRBS) length of 2^{31}-1. With the Bit Error Rates (BER) < 1×10^{-12}, Channel 1 at 140 GHz and Channel 2 at 180 GHz achieve simultaneous On-Off Keying (OOK) modulated data rates of 12.3 Gb/s and 10.3 Gb/s, respectively. This full duplex interconnect system achieves the energy efficiency of 1.58 pJ/b and the record bandwidth density of 150.7 Gb/s/mm^2.**

I. Introduction

Sub-THz/THz interconnect demonstrates high potential to address the challenge of ever-increasing data rates for chip-to-chip communications by leveraging the advantages of both electrical and optical interconnects [1][2]. Multiplexing schemes are effective approaches to boost data rate and bandwidth density by employing multiple logical sub-channels to share a same physical link. Given the large single-mode waveguide bandwidth available in the sub-THz and THz regime, it is natural to adopt channelization schemes for high aggregate data-rate communications [3] while with tolerable dispersion effects. For instance, a plastic waveguide collaborating with Yagi-couplers allows two different frequency signals transmitted simultaneously [4]. An ortho-mode channel demonstrated in [5] exploits mode orthogonality for space division multiplexing. In this paper, an FDD-based full-duplex interconnect at sub-THz is demonstrated.

II. Design of Dual-band Sub-THz Interconnect

The architecture of the sub-THz interconnect system using CMOS chips and Si DWG is shown in Fig. 1 (a). The S-parameters and E-field distribution of E_{y11} mode in a Si DWG, cover a 3-dB bandwidth of 120-220 GHz with the minimum IL better than 3.5 dB, which is depicted in Fig. 1 (b). To fully utilize the waveguide bandwidth, two sub-channels, at 140 (CH.1) and 180 GHz (CH.2), are designed. These two carriers are generated by oscillators in the dual-band CMOS TX. Binary sequences are modulated as OOK signals, combined by diplexers, transmitted through the Si DWG, and recovered by the CMOS RX. All components are required to have a bandwidth at least twice of its data rate. To minimize interference, both sub-channels should have sufficient suppression in the other sub-channel band. The dual-band sub-THz channel, presented in Fig. 2 (a), consists of diplexer banks, Si DWG and microstrip line (MSL)-to-DWG transition. The diplexer in Fig. 2 (b) is composed of hair-pin resonator filters

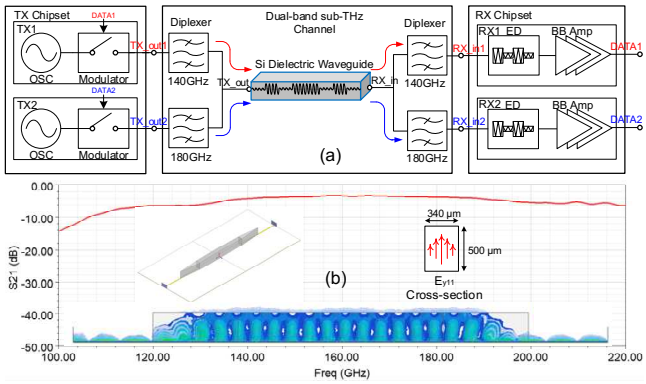

Fig. 1. (a) Dual-band sub-THz interconnect architecture; (b) simulated S-parameters and E field inside the Si DWG.

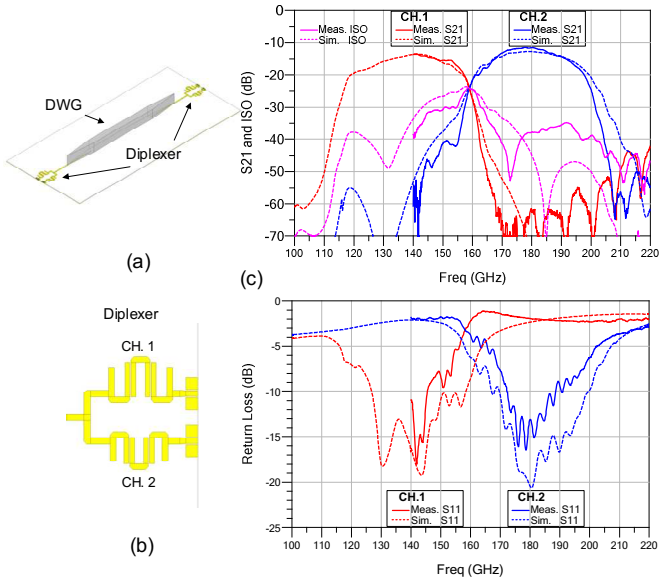

Fig. 2. Aarchitecture of (a) the dual-band sub-THz channel, (b) diplexer and (c) simulated and measured S-parameters of the dual-band sub-THz channel.

with the center frequencies of 140 and 180 GHz, respectively. All passive components are fabricated on a substrate of 20-μm bisbenzocyclobutene (BCB) ($\varepsilon_r = 2.9$, $\tan\delta = 0.03$ at 160 GHz). The S-parameters of the dual-band sub-THz channel, plotted in Fig 2 (c), was modelled in HFSS, and measured on-wafer with G-band (140 to 220 GHz) frequency extenders. The minimum measured IL is 13.2 dB for CH.1 and 11.7 dB for CH.2. Both bands have more than 20 GHz 3-dB bandwidth and 30 dB cross-band isolation. High out-of-band rejection reduces the noise on RX side and relaxes its dynamic range requirement.

Same as the dual-band channel, active TX and RX also consist of two banks working at the corresponding frequencies. The main blocks are shown in Fig 3. In the pursuit of high energy efficiency, power-hungry components, such as power

amplifier [6], doubler [7] and low noise amplifier at sub-THz, are avoided in the architecture. Therefore, the link budget must be carefully calibrated, because the output power of TX and sensitivity of RX are critical specifications to this system. TX consists of an oscillator as the carrier and a switch as the OOK modulator. Optimizing the load and transformer theoretically to maximize the output power and efficiency of oscillators can facilitate successful and efficient communications.

The non-coherent envelope detector (ED) in RX is insensitive to frequency, but the input balun must align with carrier's frequency to reduce RF reflection. The duplicated ED forms a pseudo-differential output to reject common-mode noise. The responsivity R_V, defined as second order derivative of the ratio between output voltage and input power of ED, highly determines the noise and sensitivity of a RX [8].

$$R_V = \frac{\partial^2(I_d R_d)}{\partial(v_{in}^2/re\{Z_{in}\})} = \frac{\partial^2 I_d}{\partial v_{in}^2} re\{Z_{in}\} R_d$$

where I_d is the drain current, v_{in} is the input voltage, $re\{Z_{in}\}$ is the real part input impedance and R_d is the load resistor of ED. The maximum R_V happens at the most nonlinear region of a transistor, thus, the bias is set close to V_T. After ED, baseband signals are magnified by amplifiers and buffers, then delivered to 50 ohms off-chip terminals for measurements.

III. Implement and Results

The sub-THz channel is fabricated in-house with micro-manufacturing process and assembled with a flip-chip bonder to form the dual-band sub-THz channel. TX and RX chips are implemented in a 65-nm CMOS process. The photos of CMOS chips, interconnect board and measurement setup are shown in Fig. 4. Bonding wires are employed to the signal chain for both DC and RF connections, but they are extremely lossy at high frequency. To minimize their effect, the bonding wires are kept as short as possible. The channel is fabricated on a 300-μm thickness wafer as the underneath spacer to minimize the package height difference and bonding wires length. Furthermore, bonding wires are included in the package design to evaluate and compensate their effects.

A full-duplex testbench is setup to measure the interconnect system. Bit-error rates (BER) measurement is performed by Anritsu MP2011B. The generated 2^{31}-1 PRBS pattern data is fed to the Tx, and BER and eye diagrams are measured at the RX outputs. CH.1 and CH.2 are tested in full-duplex configuration and the maximum date rates with error free are up to 12.3 Gb/s and 10.3 Gb/s, respectively. The measured BERs versus data rates together with the inset eye diagrams are plotted in Fig. 5. The power consumption of both sub-channels at the maximum error-free data rates are summarized in Table 1. The total power consumed by the proposed interconnect system is 35.8 mW and the energy-efficiency is 1.58 pJ/b.

Table 1. Power Consumption at the Maximum Error-free Data Rates.

	TX		RX		Total
	V (V)	I (mA)	V (V)	I (mA)	Power (mW)
CH.1	1	15.5	1	3.3	18.8
CH.2	1	13.8	1	3.2	17.0

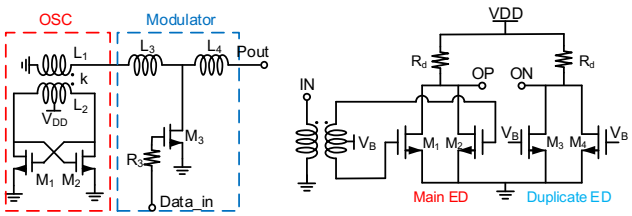

Fig. 3. Schematics of TX and envelop detector in RX.

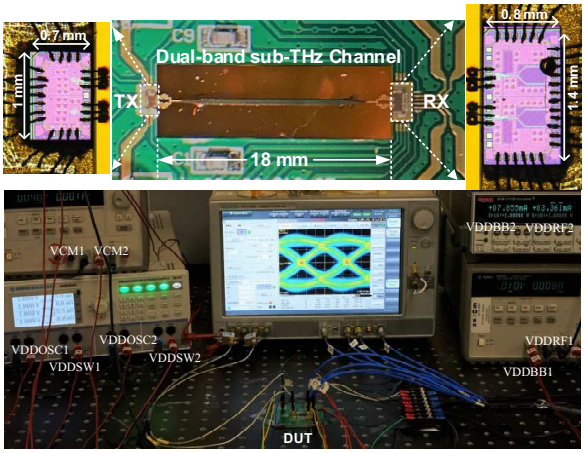

Fig. 4. The photos of TX and RX chips, system board, and full-duplex measurement setup.

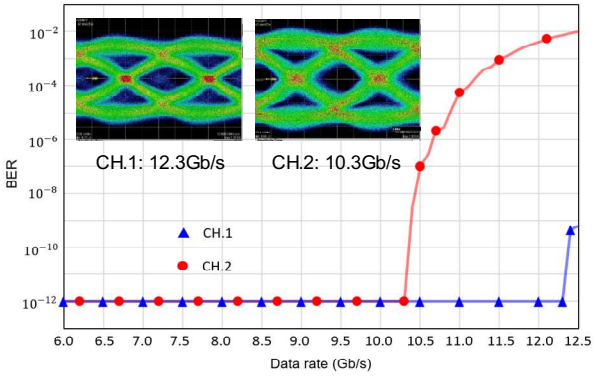

Fig. 5. BERs versus data rate of the interconnects with inset eye diagrams at PRBS 2^{31}-1 and BER < 1×10^{-12}.

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