## A Fully In-Package 4-Phase Fixed-Frequency DAB Hysteretic Controlled DC-DC Converter with Enhanced Efficiency, Load Regulation and Transient Response

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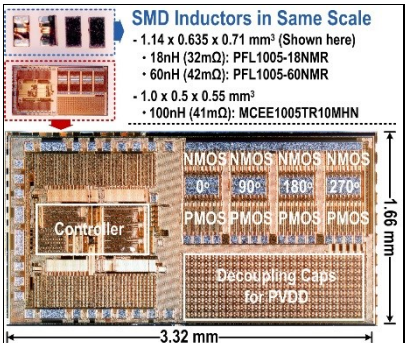
Multiphase DC-DC converters have been widely used to deliver more power more efficiently with smaller ripples and faster large-signal dynamic responses [1-5]. In terms of closed-loop voltage regulation, traditional linear PWM control has limited small-signal bandwidth, which is further compromised to ensure stability at different loading conditions with different PVT and LC variations. Non-linear control, such as hysteretic control, does not have small-signal bandwidth limitations nor stability concerns, thus can potentially achieve a faster dynamic performance. Among different topologies, current-mode hysteretic control has been adopted in 4-phase converters [2, 3]. To ensure proper operation at higher frequency, they require careful matching between the inductor current-sensing RC networks and the inductance and parasitic DC resistance (DCR) of the power inductors [2], or more complex RC sensing networks [3]. Also, the converters in [2-4] did not include current balancing, which could introduce unbalanced current due to mismatches in power transistors, control timing, and power inductors among different phases, and result in significant compromise in efficiency. To maintain optimum efficiency over a wide loading range, active-phase-count (APC) control has been introduced in [1, 2, 4]. In [4], APC is realized by a multi-bit ADC, which increases the design complexity and power consumption. Double-adaptive-bound (DAB) hysteretic control in [6] has demonstrated fast transient responses, however, it only works in single phase, and the operation is very sensitive to the delay of the comparator, the gate driver and other circuits in the control path, and the matching of the RC filters, especially at higher switching frequencies. Besides, due to the lack of a high-gain amplifier, output voltage DC accuracy is also compromised in hysteretic controlled switching converters, with a 40mV/1A load regulation in [2].

To address these limitations, this paper proposes a 4-phase DAB hysteretic controlled converter with digital DC calibration, current balancing, and APC management (Fig. 1). The DAB control achieves fixed-frequency operation and the digital calibration functions are all based on similar bidirectional-shift registers-controlled logics. This makes the converter easily extendable to adapt more phases with minimum design complexity overhead. Fig. 1 shows the system block diagram of the proposed converter. Two RC filters ($R_{DAB}C_{DAB}$, $R_SC_S$) are used for establishing the comparison boundary $V_{DAB}$ and $V_{FB}$ to regulate the output voltage. Instead of using well-matched RCs [6], $R_SC_S$ is chosen to be 4 times of $R_{DAB}C_{DAB}$ ($R_S$=$R_{DAB}$, $C_S$=4*$C_{DAB}$), with which the amplitude of $V_{DAB}$ is larger than $V_{FB}$ for a higher tolerance to circuit delays from $V_{CMP}$ to $V_X$ to work at higher frequency. In this work, matching of $R_SC_S$ to 4 $R_{DAB}C_{DAB}$ or with the L/DCR is not needed due to the existence of the digital calibrations, thus, the requirement of power inductors can be much more flexible.

The block diagram and operation principle of the digital DC output voltage ($V_O$) calibration is shown in Fig. 2. A dead-zone boundary between $V_{REFHDC}$ and $V_{REFLDC}$ is set for DC calibration. To achieve a wide range as well as a fine resolution, the bidirectional-shift-registers (BSRs) are designed including 8-bit fine, 8-bit medium and 8-bit coarse segments with carry in/out operations. When $V_O$ is beyond the dead-zone region, the medium and coarse BSRs shift the output codes to control the current sink array to adjust the slope of $V_{DAB}$ or $V_{FB}$ in all 4 phases globally. If $V_O$ is lower than $V_{REFLDC}$, $I_{FB}$ will be increased to discharge $V_{FB}$, if $V_O$ is larger than $V_{REFHDC}$, $I_{DAB}$ will be controlled to discharge $V_{DAB}$. The cross-point between $V_{DAB}$ and $V_{FB}$ changes accordingly when the slope of $V_{DAB}$ or $V_{FB}$ changes, resulting in an increase or decrease of duty cycle for accuracy calibration. When $V_O$ is calibrated into the dead-zone, the fine BSRs continue to further reduce the DC offset.

Current balancing (CB) digital calibration is also developed in this work (the left of Fig. 3). Four current sensors, with one in each phase, are designed to sense the high-side power PMOS current. By comparing the sensed voltage of Phase 90, 180 and 270 ($V_{SENPH90}$, $V_{SENPH180}$ and $V_{SENPH270}$, respectively) with the sensed voltage of Phase 0 ($V_{SENPH0}$), the BSRs operate to adjust the duty cycle of each phase locally to maintain the same amount of current as Phase 0. Take CB calibration for Phase 90 as an example. If $V_{SENPH90}$ is smaller than $V_{SENPH0}$, only $I_{CSE}$ increases to charge $V_{DABPH90}$ to increase the duty cycle of Phase 90 while $I_{CSK}$ remains 0. If $V_{SENPH90}$ is larger than $V_{SENPH0}$, only $I_{CSK}$ increases to discharge $V_{DABPH90}$ to reduce the duty cycle while $I_{CSE}$ remains 0.



Chip photo with 0402 miniature SMD inductors in the same scale.

APC management is also developed in this work (the right of Fig.3). If $V_{SENPH0}$ is smaller than $V_{REFHAPC}$, only Phase 0 is activated. If the load current increases such that $V_O$ drops below $V_{REFLDC}$, the burst-mode (BM) will be activated for the full 4-phase operation with 100% duty cycle to charge the power inductors with full thrust. The BM will be disabled when $V_O$ starts to recover, meaning that the inductor current has been increased larger than the load current. This is achieved by comparing $V_O$ with $V_{OLPF}$, a delayed version of $V_O$. In terms of heavy-to-light load change, when load current steps down to light load rapidly, the system will first turn off Phase 90 and Phase 270. If $V_{SENPH0}$ is still lower than $V_{REFHAPC}$, after a preset settling period, Phase 180 will also be turned off. To avoid significant output voltage fluctuations, the duty cycle of the corresponding phase(s) will be reduced gradually. When the sensed voltage is lower than $V_{REFLAPC}$, the corresponding phase(s) will be completely turned off.

The proposed converter has been fabricated in 180-nm CMOS and measured at 10MHz and 25MHz with 18-to-100-nH 0402 inductors for full in-package integration (chip & inductor photo above), converting 1.8V to 0.6V-1.5V. Fig. 4 shows the measured efficiency versus load currents at different voltages. A 93.9% peak efficiency is achieved with 100-nH 0402 inductors. Up to 12.2% efficiency improvement and better $V_X$ duty-cycle matching in measured waveforms are observed by enabling the CB calibration. Fig. 5 shows the measured load transient performance with fast current steps of 2.85A/2ns. The measured droop is 100mV with BM, which is 33.3% smaller than the 150 mV without BM. Fig. 5 also shows the steady-state DC $V_O$ accuracy comparison with and without the DC calibration. A significant improvement of 21.63% is observed with the calibration, with error remains within 2.5% in the full loading range with different voltages. This verified that the proposed DC calibration can effectively relax the accuracy and matching requirement of the RC current-sensing network in previous current-mode hysteretic designs, while remaining a load regulation comparable to designs with linear control. Fig. 6 shows the measured $V_X$ waveforms in fast load transients for APC demonstration, as well as the comparison table with recent multiphase non-linearly controlled switching converters. This work achieves higher efficiency using smaller-than-the-chip inductors with relaxed tolerances in L, matching and DCR, and decent transient responses with faster current steps.

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**References:**

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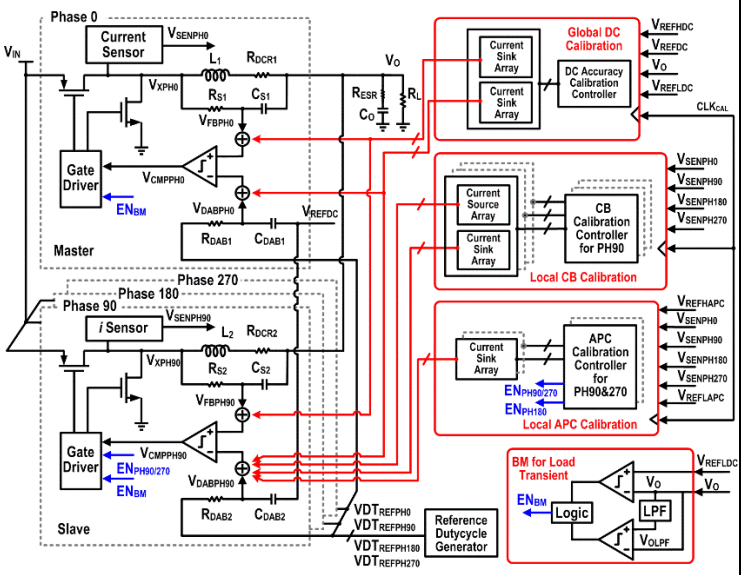



Fig. 1. System block diagram of the proposed converter.

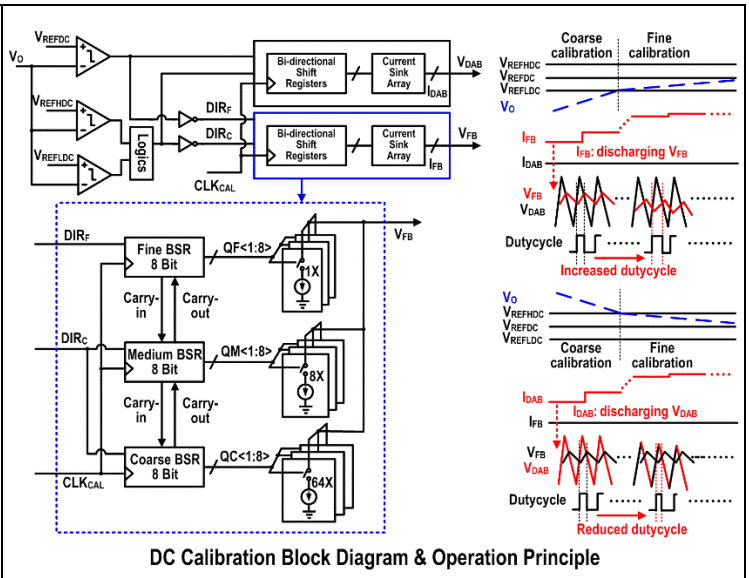



Fig. 2. Block diagram and operation principle of the proposed digital DC $V_O$ calibration.

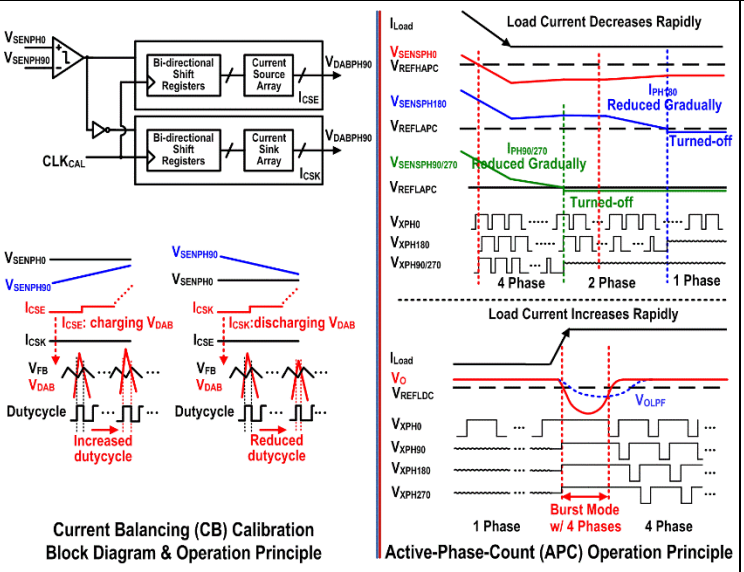



Fig. 3. Operation principle of the proposed digital CB calibration and APC management.

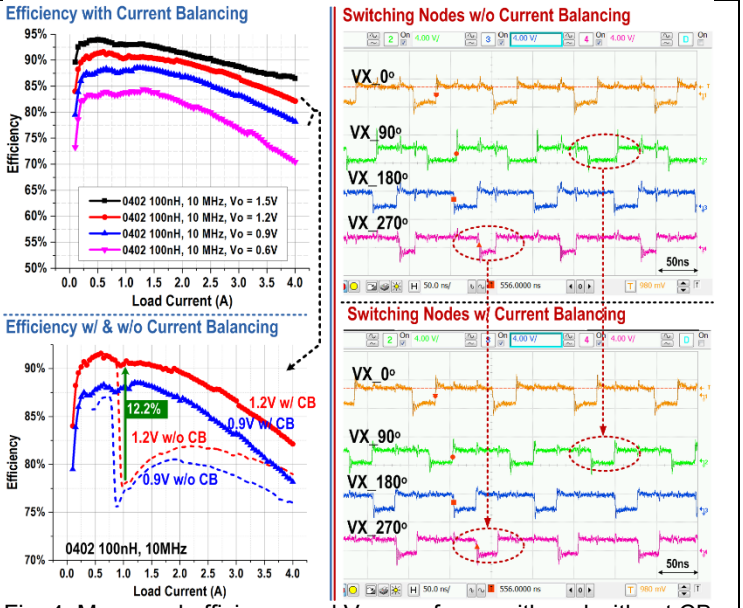



Fig. 4. Measured efficiency and $V_X$ waveforms with and without CB.

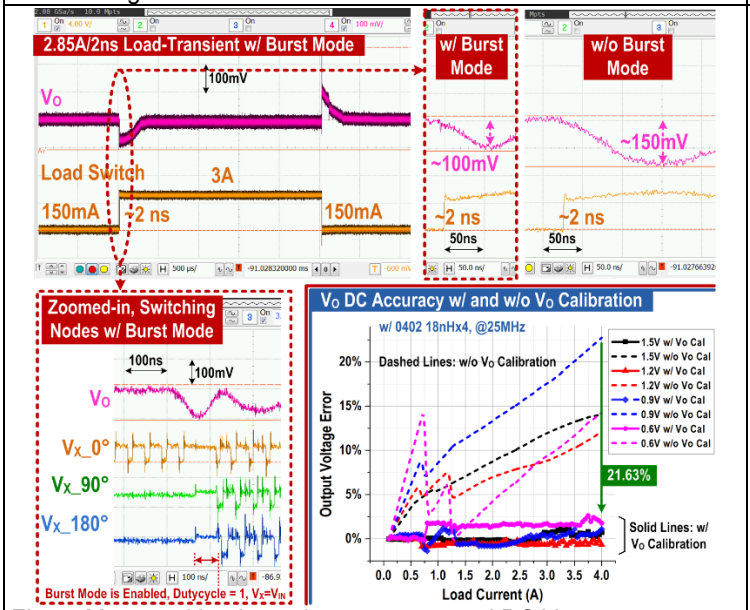
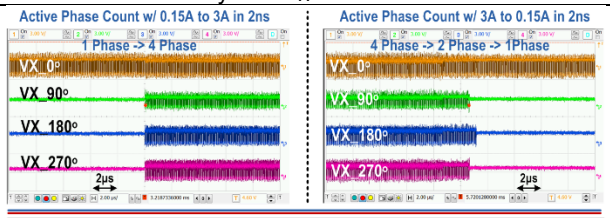



Fig. 5. Measured load transient response and DC $V_O$ accuracy.




| | ISSCC'14 [3] | ISSCC'14 [4] | ISSCC'17 [2] | ISSCC'19 [5] | This work | | |
|---|---|---|---|---|---|---|---|
| Technology | 180nm | 250nm | 350nm | 28nm | 180nm | | |
| Control | CM Hysteretic | CM Hysteretic | CM Hysteretic | Digital AOT | CM Hysteretic | | |
| # of Phase | 4 | 3 | 4 | 4 | 4 | | |
| Input Voltage | 3.3V | 2.8-5.5V | 3.3V | 1.2V | 1.8V | | |
| Output Voltage | 0.7-2.5V | 0.2-3.3V | 0.3-2.6V | 0.6-1V | 0.6-1.5V | | |
| Inductor | 78nH | 2.2µH | 200nH | 15nH | 18nH | 60nH | 100nH |
| Inductor Size | N.A. | N.A. | N.A. | N.A. | 0.51 mm³ x 4 | | 0.275 mm³ x 4 |
| Output Capacitor | 0.94µF | 66µF | 2.5µF | 0.2µF | 1.2µF | 1.2µF | 2.0µF |
| Switching Frequency | 40MHz | 500kHz | 25MHz | 75MHz | 25MHz | 25MHz | 10MHz |
| Peak Efficiency | 86.1% | 90.2% | 88.1% | 89% | 90.6% | 90.0% | 93.9% |
| RC & L/DCR Matching Requirement | High | High | High | No | Low | | |
| Active Phase Count | No | Yes | Yes | Yes | Yes | | |
| Current Balance | No | No | No | No | Yes | | |
| $V_O$ Droop (%) | 117.6mV (9.8%@1.2V) | 40.5mV (2.7%@1.5V) | 102.4mV (6.4%@0.9V) | 80mV (8.9% @ 0.9V) | 100mV* (8.3%@1.2V) | | |
| @Current Step (Current Slope) | @5A/5ns (1A/ns) | @8A/20µs (0.0004A/ns) | @4A/5ns (0.8A/ns) | @1A/10ns (0.1A/ns) | @2.85A/2ns* (1.425A/ns) | | |

* With 18-nH SMD Inductors.

Fig. 6. Measured $V_X$ with APC operation, and comparison table.