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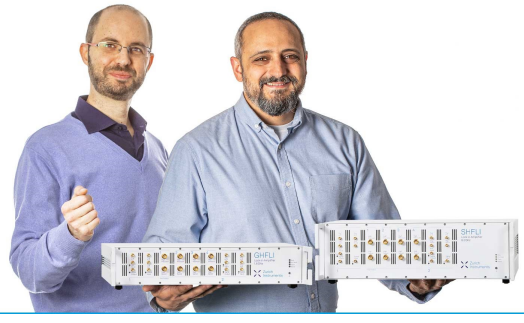

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ABSTRACT

We examine if the bundling of semiconducting carbon nanotubes (CNTs) can increase the transconductance and on-state current density of field effect transistors (FETs) made from arrays of aligned, polymer-wrapped CNTs. Arrays with packing density ranging from 20 to 50 bundles μm^{-1} are created via tangential flow interfacial self-assembly, and the transconductance and saturated on-state current density of FETs with either (i) strong ionic gel gates or (ii) weak 15 nm SiO_2 back gates are measured vs the degree of bundling. Both transconductance and on-state current significantly increase as median bundle height increases from 2 to 4 nm, but only when the strongly coupled ionic gel gate is used. Such devices tested at −0.6 V drain voltage achieve transconductance as high as 50 μS per bundle and 2 mS μm^{-1} and on-state current as high as 1.7 mA μm^{-1}. At low drain voltages, the off-current also increases with bundling, but on/off ratios of $\sim 10^5$ are still possible if the largest (95th percentile) bundles in an array are limited to ∼5 nm in size. Radio frequency devices with strong, wraparound dielectric gates may benefit from increased device performance by using moderately bundled as opposed to individualized CNTs in arrays.

Semiconducting carbon nanotubes (CNTs) are exceptional electronic materials that can potentially outperform Si and GaAs[1] in the channel of field effect transistors (FETs) in radio frequency (RF)[2,3] and logic[4] applications. RF FETs require high transconductance (g_m), low differential drain conductance, and low parasitic capacitance to achieve gain at high frequencies.[3] Logic devices require high on-state current density (I_D) to drive fast switching speeds.[4] To maximize g_m and I_D, CNTs need to be integrated into FETs in the form of tightly packed, aligned arrays to obtain a high density of conducting pathways in the channel.[5]

Generally, maintaining the isolation and individualization of CNTs in the channel is deemed important. If the CNTs are uniformly spaced and individualized, then it is possible to uniformly and fully gate them. Uniform gating improves the device-to-device uniformity of threshold voltage, V_T, while minimizing subthreshold swing. Full gating (i.e., a large gate-channel capacitance per CNT) is important for maximizing g_m and I_D and minimizing the off-state conductance per CNT. On the other hand, incorporating bundled CNTs (or in other words colinear aggregates of CNTs) in the channel provides an opportunity to increase the density of CNTs above and beyond what is possible using fully isolated CNTs, by locally extending the CNT array out-of-plane. Therefore, higher g_m and I_D could be possible, but there are disadvantages. For example, our prior work showed that bundling puts some CNTs within arrays in different local electrostatic environments than other CNTs, causing unwanted variations in V_T, with degraded subthreshold swing.[6,7] Our prior work also showed that despite the bundling, there was minimal improvement in the g_m or I_D per bundle compared to an isolated CNT. However, this prior work was conducted using a relatively weak, back gate comprised of 15 nm of SiO_2 (effective oxide thickness, EOT, of 15 nm).

Here, we investigate whether the bundling of CNTs can increase the g_m and I_D of FETs fabricated from arrays, when a stronger gate is used. Strong gates are potentially capable of modulating charge density in multiple CNTs per bundle, thereby leading to higher g_m and I_D. Researchers have described and created innovative gate insulator and electrode designs including top, double, and surround (all-around)

gate structures to increase the strength of the gate and reduce operating voltages in FETs.[8–10]

Here, ion gel gates are used (EOT <1.0 nm). Advantageously, the use of an ionic gate allows us to first characterize the transport properties of a CNT array FET using a back-gated geometry, then image the size, density, and conformation of CNTs in the channel, and, finally, remeasure the transport properties of the same array after the facile application of the ion gel. Ionic liquids and gels have been employed in the past as very high capacitance gates in both single CNT and array CNT FETs.[11–15] Though ion gel gates may not be suitable for many commercial applications because of their slow switching speeds,[16] recent thin layer conformal dielectric gates[8] with capacitance as high as 2.9 pF cm^{-1} per CNT have approached the high capacitance of ion gels,[17–19] estimated as between 2.5 and 6.3 pF cm^{-1} depending on frequency and voltage; therefore, the multi-CNT bundle gating characterized here may be achievable in dielectric gated devices that have commercial use. See Figs. S1 and S2 for capacitance estimates.

The FETs investigated here are made from poly[(9,9-dioctylfluorenyl-2,7-diyl)-alt-(6,6′-[2,2′-bipyridine])] (PFO-BPy) wrapped and sorted arc discharge semiconducting CNTs deposited using a recently published technique named Tangential Flow Interfacial Self-Assembly (TaFISA),[20] which produces uniform films of aligned arrays over large areas. To fabricate devices with a range of packing density and degrees of bundling, locations are chosen at the edges of the deposition region where transient effects at the beginning and end of the TaFISA process generate such array variation but still maintain a high degree of alignment.

The bundles studied here are distinct from the bundles of CNTs present in as-synthesized CNT powder in two ways. First, the CNTs in the bundles here are all (or predominantly all) semiconducting, whereas both semiconducting and metallic CNTs are present in as-synthesized CNT powder. Second, the polymer wrapper used is present on the surface of the CNTs during and following TaFISA, meaning that the bundles studied here are bundles of polymer wrapped CNTs (whereas the CNTs are bare and closely coupled in as-synthesized CNT powder). After deposition, the polymer wrapped CNTs are heat-treated at 400 °C in vacuum to remove the polymer sidechains;[1] however, the polymer back-bone remains, reducing CNT–CNT coupling.

The FETs are first constructed as back gate devices with the CNT array exposed to ambient [Fig. 1(a)]. The details of the fabrication process are included in the supplementary material [Figs. S3(a)–S3(f)]. Transfer and output curves are measured in this back gated condition first. The topography of the arrays is next characterized via atomic force microscopy (AFM) using a Bruker Icon with ScanAssist probe tips in the tapping mode. The number of CNTs or CNT-bundles that span the electrodes is counted manually. The heights of the CNTs and bundles are extracted by finding the peak heights in cross sections of the channel. Five cross sections of the channel are analyzed for each device. The median height of the CNTs or bundles in each cross section is calculated, and the median height of the CNTs in the FET is then determined by finding the median of those five results.

After AFM characterization, small ∼20 μm droplets of the ion gel, a mixture of 1-ethyl-3-methylimidazolium bis(trifluoromethylsulphonyl)imide ([EMIM][TFSI]) and polystyrene-b-poly(ethylene oxide)-b-polystyrene,[21] are applied using a needlelike probe tip near the gap between the side gate and the source and drain electrodes. When the probe tip is lifted, the gel droplet spreads to cover the CNT channel and contact the side gate [Figs. 1(b) and 1(c)]. This electrode geometry and ion gel droplet application enable direct probing of bare metal contact pads on all electrodes, with minimal contact between the gel and the source and drain electrodes and, therefore, minimal leakage current through the gel. Ion gel gates can be contacted from the top, side, or by using the back gate to form a hybrid oxide–ion gel capacitor.[22] In our case, we choose the stronger back hybrid gate [Fig. S3(f)]. Transfer curves and output curves of the encapsulated devices are collected over a few weeks, and the devices are stored in a nitrogen glovebox between measurements. Repeat measurement over this time shows the devices' transfer properties were stable.

Figures 1(e) and 1(f) show examples of topographic AFM images of two CNT channel arrays with similar packing density of 40–42 CNT-bundles μm^{-1} but different median heights and, therefore, different degrees of bundling. The packing density of all the devices measured ranges from 20 to 50 bundles μm^{-1}, and the median heights of

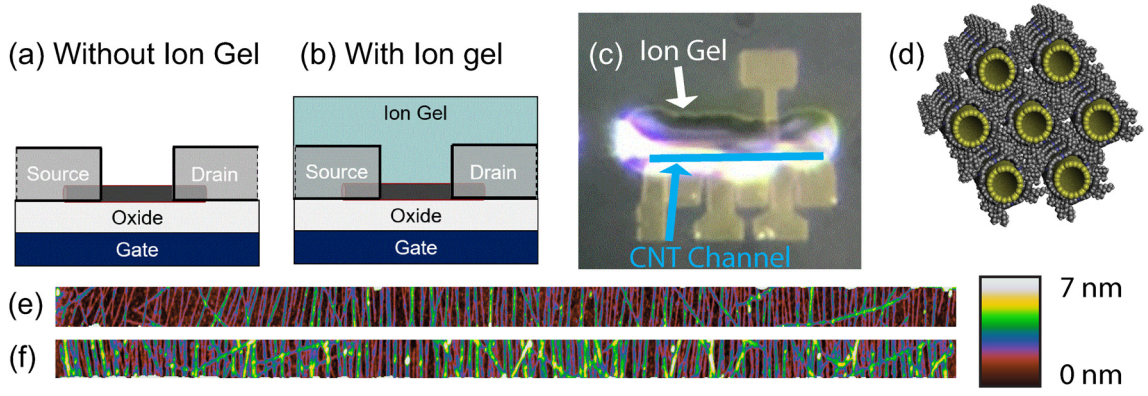

FIG. 1. Side view channel region of the FETs (a) before and (b) after application of the ion gel. (c) Optical image of ion gel applied to a set of devices; the ion gel and location of the CNT channel are marked. (d) A rendering of a large bundle of polymer wrapped CNTs before side chain removal. (e) and (f) AFM images of the channels of two devices with similar bundle packing densities of 40–42 bundles μm^{-1} and median bundle heights of 2.9 nm (e) and 3.5 nm (f). To the right of the AFM images is the height color scale ranging from 0 to 7 nm. The width of the two AFM images is 4 μm.

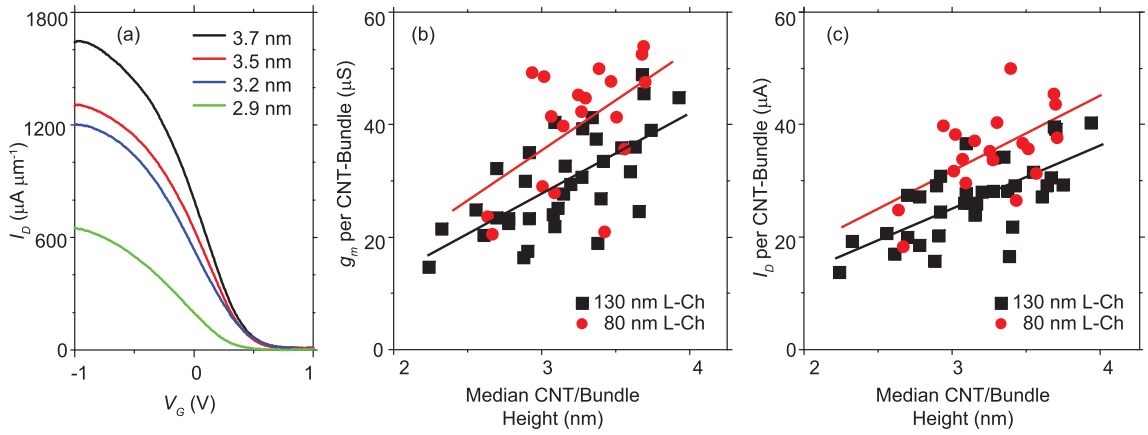

FIG. 2. (a) Transfer curves of ion gel gated devices. All have CNT-bundle packing density of 42–43 bundles μm^{-1} and 130 nm L_{Ch} but different median bundle heights. The g_m (b) and I_D (c) increase with bundle height at $V_D = -0.6$ V, indicating that more than one CNT per bundle is turned on by the gate. The red and black lines are least squares regression fits to the data. The p-values for the linear regression slopes are 6×10^{-6} and 5×10^{-6} for the g_m and I_D of the 130 nm L_{Ch} devices and 0.013 and 0.008 for the 80 nm L_{Ch} devices, respectively, indicating the slopes are significantly different from zero.

the bundles in each device range from 2.2 to 3.9 nm. Since the CNTs used in these devices have bare diameters of 1.2–1.7 nm and are at least partially polymer wrapped adding ~0.0–0.6 nm to each CNT (total diameter range of 1.2–2.3 nm), the median bundle heights of 2.2–3.9 nm indicate there is bundling in all devices.

The transfer curves of all measured FETs are presented in Fig. S4(a) ($L_{Ch} = 80$ nm; without ion gel), Fig. S4(b) ($L_{Ch} = 80$ nm; with ion gel), Fig. S4(c) ($L_{Ch} = 130$ nm; without ion gel), and Fig. S4(d) ($L_{Ch} = 130$ nm; with ion gel). A compilation of the g_m, I_D, subthreshold swing, V_T, and on–off ratio extracted from these measurements is provided in Tables S1 and S2 and Fig. S5, and an example of an output curve is shown in Fig. S6. Highlights of the most important trends noted in these data are further analyzed and discussed below.

Representative transfer curves are presented in Fig. 2(a), for ion gel gated FETs with four different median bundle heights ranging from 2.9 to 3.8 nm (but with similar bundle packing density of ~42–43 bundles μm^{-1}) at $V_D = -0.6$ V and $L_{Ch} = 130$ nm. The g_m per bundle almost doubles from 26 to 44 μS, and I_D per bundle increases from 24 to 37 μA, as the median bundle size increases from 2.9 to 3.8 nm. The same trends are also observed when the packing density is smaller (~25 bundles μm^{-1}) and for $L_{Ch} = 80$ nm.

The g_m per bundle of all devices vs median bundle height is plotted in Fig. 2(b), showing a positive correlation at both $L_{Ch} = 80$ and 130 nm. These data evidence that the ion gel gate is strong enough that multiple CNTs present in bundles are turning on at the same gate potential and contribute to g_m achieving values as high as 2.0 mS μm^{-1} and almost 50 μS per bundle [Figs. S5(f) and S5(g)]. Using the weaker back-gate without the ion gel, in contrast, shows no relationship between the degree of bundling and the transconductance (see Fig. S7), indicating that larger bundles have the same g_m as smaller bundles and individual CNTs. Thus, the back-gate is only able to effectively modulate the charge density in approximately one CNT per bundle. The back-gated g_m is also an order of magnitude lower than the ion gel g_m (as expected because of the smaller back gate-channel capacitance).

Since the ion gate is strong enough to turn on multiple CNTs in each bundle at the same time, it is reasonable to expect that the saturation current in larger bundles would be higher than in smaller bundles. To check this expectation, we plot I_D per bundle vs the median bundle height [Fig. 2(c)] and find that the on-current per bundle increases as the bundle size increases. This further supports our conclusion that multiple CNTs in bundles are contributing to the FETs' on-state transport characteristics.

Bundling also influences off-current. Figure 3 shows the off-current of the devices at a V_D of −0.1 V as a function of median bundle height. The FETs fall into two groups: (1) devices with relatively low off-currents that decrease with decreasing bundle size and (2) devices with high off-currents that are consistently high irrespective of bundle size. The trend seen in the former bundle height-correlated group likely reflects the presence of CNTs in the interiors of bundles that are screened by the exterior CNTs and, therefore, are only weakly affected by even the ion gate. Electrostatic models and accompanying experiments have shown that weakly gated semiconducting CNTs do

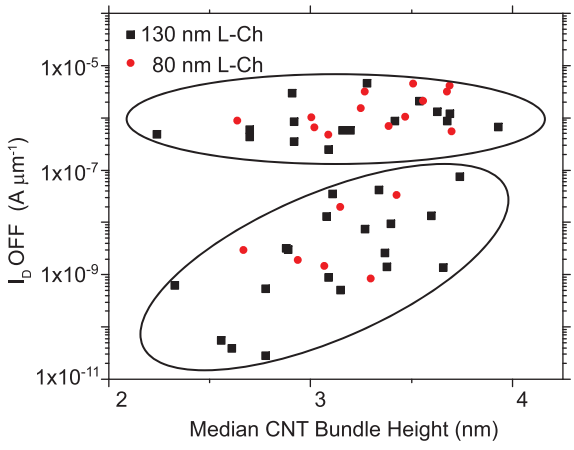

FIG. 3. Off-current for all ion gel devices colored by channel length at $V_D = -0.1$ V. The ellipses are guides for the eye indicating the two types of off-current behavior.

not turn strongly on or off,[7] and a single CNT within a bundle that is highly screened may have a high enough conductance to limit off-current in an array device. In this situation, the majority of the CNTs in the device channel will be strongly gated, and just a single or a few interior CNTs will be weakly gated. The g_m and I_D will be high since they are determined by the large number of strongly gated CNTs, but the subthreshold off-state current would be dominated by the single or few weakly gated CNTs that have relatively high off-currents. The number of such weakly gated CNTs would naturally increase with increasing bundle size, consistent with the observed data. On the other hand, the devices with high off-current that is not correlated with bundle height may be explained by different effects. These devices could have one or more metallic CNTs that limit the off-current. Alternatively, these devices could contain some configuration of semiconducting CNTs that does not turn off for some other reason such as bandgap narrowing due to bare CNT–CNT contact, in other words due to strong inter-CNT coupling[23,24] that may sporadically occur in regions that happen to have no or low polymer coverage. Plots of the off-current vs the 95th percentile in bundle height (Fig. S8) suggest that low off-currents ($<1\,\text{nA}\,\mu\text{m}^{-1}$ at $V_D = -0.1\,\text{V}$) are possible in the height-correlated regime, if the largest bundles in an array are smaller than ~5 nm, but not with larger bundles.

At $V_D = -0.6\,\text{V}$, all devices have similar off-currents, larger than at $-0.1\,\text{V}$. The increase in off-current with the magnitude of V_D is expected due to increased minority carrier current arising from band-to-band hopping at the abrupt source/channel interface because the gated portion of the channel extends all the way to the source and drain electrode edges.[25–28] RF devices do not require as low of off-current as logic devices; thus, with appropriate gate constructions, RF devices may benefit from moderate bundling through the improved g_m and I_D, despite elevated off-current. The output conductance (g_d) is an important parameter for RF performance and would need to be analyzed in future work (see Fig. S6 for more information).

Plotted in Fig. 4 is a champion device with a median bundle height of 3.1 nm, exceptional I_D of 1.3 mA μm^{-1} and g_m of 1590 mS μm^{-1} (41 μS per bundle) at $V_D = -0.6\,\text{V}$. When tested at $V_D = -0.1\,\text{V}$, this device also has an on/off ratio of 2×10^5.

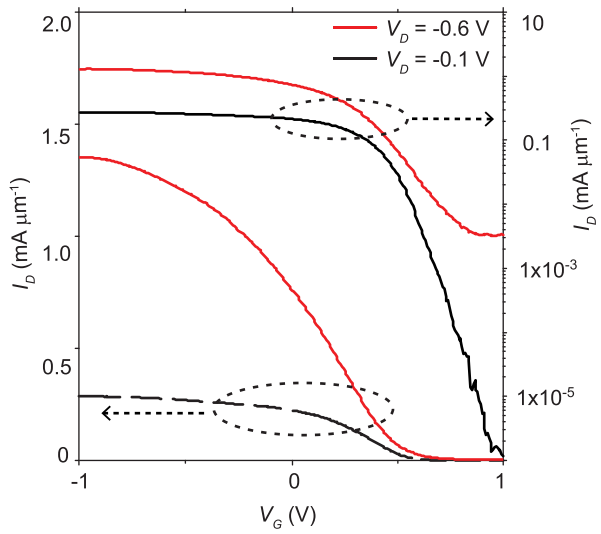

FIG. 4. Transfer curve of champion device at V_D of $-0.6\,\text{V}$ (red) and $-0.1\,\text{V}$ (black).

In summary, we have fabricated hybrid ion gel gated FETs from CNT arrays with various packing densities and with a range of bundle sizes and shown that g_m and I_D increase with bundle size. These effects most likely occur as multiple CNTs within the bundles are simultaneously turned on due to the high strength of the hybrid ion gel gate. At small V_D, larger bundles are also associated with higher off-currents, though some devices also have persistently high off-current that is not clearly associated with bundle size. These results are consistent across a range of packing densities from 20 to 50 bundles μm^{-1} and median bundle heights of 2.5 to 4.0 nm. An exceptional I_D of 1.3 mA μm^{-1} and g_m of 1590 mS μm^{-1} (41 μS per bundle) at $V_D = -0.6\,\text{V}$ are obtained. Some TFSI^- anion penetration into the interiors of CNT bundle structures may be viable in the on-state (negative gate bias), although it likely plays a minor role in this study for multiple reasons as discussed in the supplementary material. Most importantly, for the bundle diameter range explored here (2–4 nm), most of the CNTs are still on the surface of the bundles and, thus, already easily accessible to the ion gel.

Bundling may be useful in RF applications since it increases g_m without altering device dimensions when a strong gate is used, thereby limiting the parasitic capacitance that degrades RF performance. High capacitance top gate oxide structures using high-k dielectrics are approaching the strength of ion gel gates and may be strong enough to replicate the results reported here. Indeed, electrostatic models show that CNT-gate capacitance per bundle should increase with increasing bundle size when using thin (e.g., 3–5 nm) high-k (e.g., HfO_2) gate dielectrics in a similar fashion to ion gel gates (Fig. S1). In contrast, the CNT-gate capacitance per bundle is relatively constant as the bundle size is increased when using a relatively thick and weak 15 nm SiO_2 back gate (Fig. S2), explaining the invariance of g_m and I_D with bundle size observed experimentally in previous work[6] and here (Fig. S7) when using thick back gates. The increased off-current that is correlated with bundle size would be problematic for logic devices, but not for RF devices that are operated in the on-state. Allowing bundling may also enable more rapid commercialization of CNT arrays since it relaxes the requirement that each s-CNT is isolated, which can be difficult to achieve with perfect uniformity in high packing density arrays.

See the supplementary material for device capacitance estimates (Figs. S1 and S2), fabrication details [Figs. S3(a)–S3(f)], transfer curves for all FETs [Figs. S4(a)–S4(d)], FET performance metrics for 80 and 130 nm L_{Ch} [Tables S1 and S2, Figs. S5(a)–S5(i)], example output curves (Fig. S6), g_m per bundle vs median bundle height without ion gel (Fig. S7), off current vs 95th percentile bundle height (Fig. S8), and benchmarking charts and tables [Figs. S9(a)–S9(e), Tables S3 and S4].

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AUTHOR DECLARATIONS

Conflict of Interest

The authors have no conflicts to disclose.

Author Contributions

Sean Michael Foradori: Conceptualization (equal); Data curation (lead); Formal analysis (equal); Investigation (equal); Methodology (equal); Visualization (lead); Writing – original draft (lead); Writing – review and editing (equal). **Jonathan Dwyer:** Methodology (supporting); Resources (supporting). **Anjali Suresh:** Methodology (supporting); Resources (supporting). **Padma Gopalan:** Conceptualization (equal); Funding acquisition (supporting); Investigation (supporting); Resources (supporting); Supervision (supporting). **Michael Arnold:** Conceptualization (equal); Data curation (supporting); Formal analysis (equal); Funding acquisition (lead); Investigation (equal); Methodology (supporting); Project administration (lead); Resources (lead); Supervision (lead); Validation (lead); Visualization (supporting); Writing – original draft (supporting); Writing – review and editing (lead).

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