A 28-GHz Passive Outphasing Load Modulator in 40-nm GaN

Cameron Hill and James F. Buckwalter
University of California Santa Barbara, USA
cameron_hill@ucsb.edu

***Abstract*— This paper presents a passive tunable matching network for load-modulation of a power amplifier (PA). With a set of discrete RF switches, different real impedance transformations can be realized to optimize the loadline match of the PA for output power and/or efficiency. To handle high-power, a 40-nm GaN MMIC process was used to realize three RF switches that switch across a ring impedance network. The tunable matching network realizes 15, 50, or 80Ω depending on the switch state with insertion loss (IL) between 1.7 and 3.3 dB at a center frequency of 28 GHz. The GaN devices have a high breakdown point and therefore the network P_{1dB} exceeds 33 dBm. The bandwidth of the network exceeds 2.5 GHz.**

***Keywords*— RF Switch, GaN, Power Amplifier, Load Modulation, Millimeter-Wave**

I. Introduction

Emerging 5G wireless networks achieve high data rates through the use of orthogonal frequency division multiplexing (OFDM) waveforms which have high peak-to-average power ratios and require high PA efficiency at up to 10 dB back-off from the peak transmit power [1]. Load modulation improves backoff efficiency of PAs by exploiting the relationship between load impedance, efficiency, and output power. Often load modulation is accomplished by leveraging the interaction between two PAs as in Doherty and outphasing architectures [2], [3]. However, these designs are difficult at millimeter-wave (mm-wave) frequencies due to sensitive combining networks and added cost and complexity of multiple amplifiers.

Alternatively, dynamic load modulation (DLM) uses switches to change the output tuning elements of the power amplifier to optimize efficiency for the desired output power [4]. Ideally, the DLM network would only change the real value of the load impedance for optimum tuning. However, most approaches require a large bank of switched capacitors or varactors to change the load capacitance and therefore cannot access large areas of the smith chart. [5], [6]. Scaling the DLM to mm-wave bands is also difficult due to the large parasitic capacitance and resistance associated with the switch or varactor components. Additionally, large banks of switches are generally only feasible in highly scaled CMOS processes, placing limits on the power handling for the network at the output of the PA.

To get the best of both outphasing and DLM, this paper proposes a passive outphasing load modulator (POLM) from 28 GHz fabricated in a 40nm GaN process that allows the load impedance to be tuned between 20 and 80 ohms with minimal imaginary load variation. The network switches across a transmission line ring where only one switch is required for each state, enabling low loss and allows for practical device layout at high frequency. The GaN process also allows for high linearity and power handling to provide minimal distortion in transmitting. Section II will discuss the theory and circuit design of the network while Section III will present the measurement results.

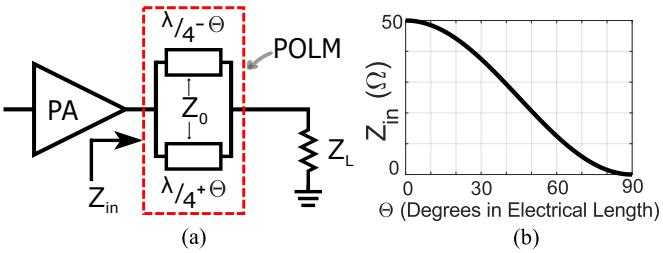

Fig. 1. Ideal circuit schematic for (a) real-impedance load modulation network, and (b) the input impedance vs. variation in transmission line length

II. Circuit Design

Similar to phase mismatching used in outphasing networks [7], the POLM network proposed is shown in Fig. 1 (a). A transmission line loop of characteristic impedance, Z_0 and total circumference of $\lambda/2$ is placed between the load Z_L and the PA as a matching network [8]. If the length of each segment of the loop is adjusted by $\pm\Theta$ relative to $\lambda/4$, then the input impedance can calculated be from

$$Z_{in} = \frac{Z_0^2(\cos(2\Theta)+1)^2}{16Z_L\cos^2(\Theta)} \tag{1}$$

and is plotted in Fig. 1 (b) for the case of $Z_0 = 100\Omega$ and $Z_L = 50\Omega$. Eq. 1 demonstrates that ideal load modulation is possible, i.e., only a real impedance from zero to $Z_0^2/(4Z_L)$ is presented to the PA.

Constructing a network with continuously tunable transmission line lengths becomes a major design challenge. Because it is difficult to get large phase variation without large loss in transmission lines, a switched network accesses different points in the loop to adjust the impedance seen by the PA. A circuit schematic for the proposed impedance tuning network is shown in Fig. 2.

Because the maximum real input impedance is bounded by $Z_0^2/(4Z_L)$, it is desirable for Z_0 to be as large as possible to allow for a large input impedance variation. In order to increase the possible range of Z_{in}, artificial transmission lines are used, where the shunt capacitance is distributed, but a stripline coil is used to increase inductance per unit length. By doing this, Z_0 can be raised to 100Ω to produce a suitable impedance tuning range and each loop of the artificial transmission line produces a phase shift of 15 degrees at 28 GHz.

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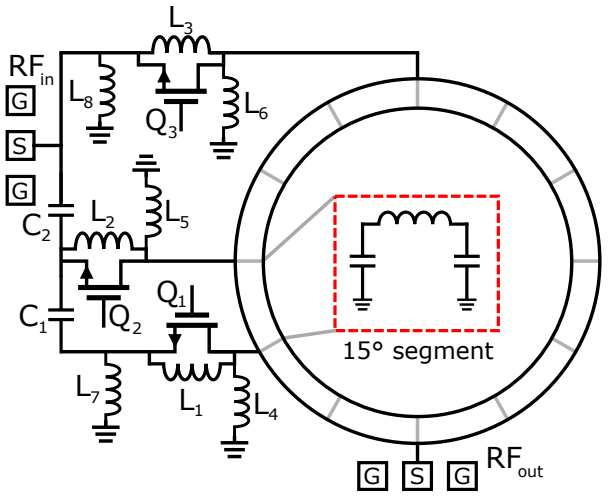

Fig. 2. Circuit schematic of load modulation loop highlighting pseudo-artificial transmission line loop, and switch tuning elements.

Table 1. Values of Passive Components

Comp.	L_1	L_2	L_3	L_4	L_5	L_6	L_7	L_8
Val. (pH)	280	1000	730	300	300	350	260	320

Switches Q_2 and Q_3 are 300um wide devices for states 2 and 3 while Q_1 is a 600um device for state 1 since the input impedance seen when Q_1 is on is significantly lower. To eliminate feed through and improve the isolation of each switch, resonating inductors L_1, L_2 and L_3 are added to their respective switches. Adding the devices to the loop adds significant capacitive loading at each location and inductors L_4, L_5, and L_6 are used to combat this. The values of the inductors are given in Table 1. While these inductors prevent undesired loading of the loop, they also limit the bandwidth of the network, especially in state 3 which would normally have the widest bandwidth, but is also most sensitive to shunt parasitics.

A combination of switch losses and parasitics on the input lines cause the impedance at the input to drift above the simulated values of 12, 26, and 48 Ω each of the loop inputs. Adding L_8 allows the input parasitic of Q_3 to be minimized while the combination of C_1 and C_2 cancels the inductance associated with the length of the input network to create a close to ideal simulated impedance of 15Ω. As a result, additional impedance separation is created between the three states, and utilizing C_2 and L_7 moves the impedance seen for states 2 and 3 to 45 and 75 Ω respectively.

III. Measurement Results

The S-parameters were measured using a 67-GHz vector network analyser and the input and output pads were de-embedded using on-chip SOLT calibration elements. The probing setup is shown in Fig. 3. A comparison of the measured and simulated Z_{in} is shown in 4 for states 1, 2 and 3. The measured values for Z_{in} are 13.5, 40, and 80 Ω.

The mismatch between the simulated and measured parameters is a result of modeling errors leading to the resonant networks being tuned closer to 29-GHz while the loop network is tuned to 28-GHz. This shift in the center frequency can be seen in the log-scale measurements shown in Fig. 5. This discrepancy leads to slightly more insertion loss (IL) than simulated. The measured IL is 1.7, 2.4, and 3.3 dB for each of the three load states, compared to simulated losses of 1.4, 1.6, and 1.9 dB in states 1, 2 and 3, respectively. In the limiting state 3, the 1 dB Bandwidth extends from 26.7-29.4 GHz

The measured ratio of the lowest to highest real impedance presented by the network corresponds to a back-off power of 7.7dB. In the worst case of state 3 the losses correspond to a

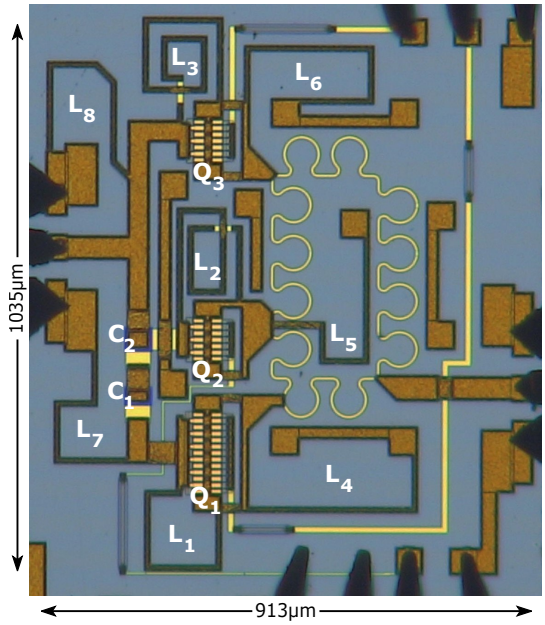

Fig. 3. Chip photograph for the load modulation network in the 40nm GaN process with discrete elements highlighted to match Fig. 2

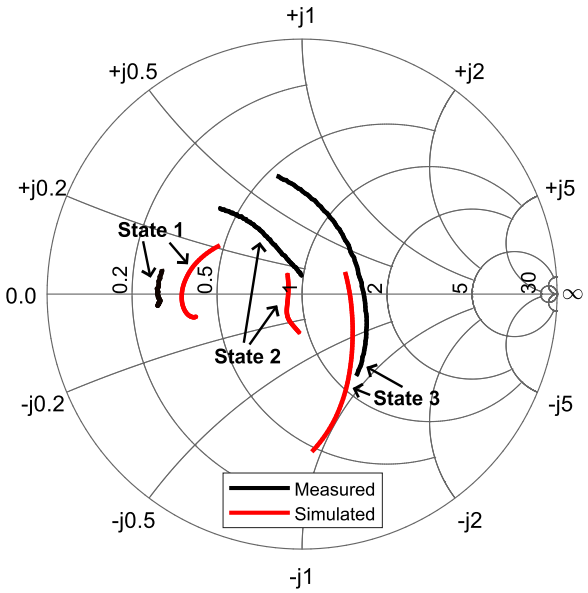

Fig. 4. Measured versus simulated S11 for the three states of the network on a Smith chart

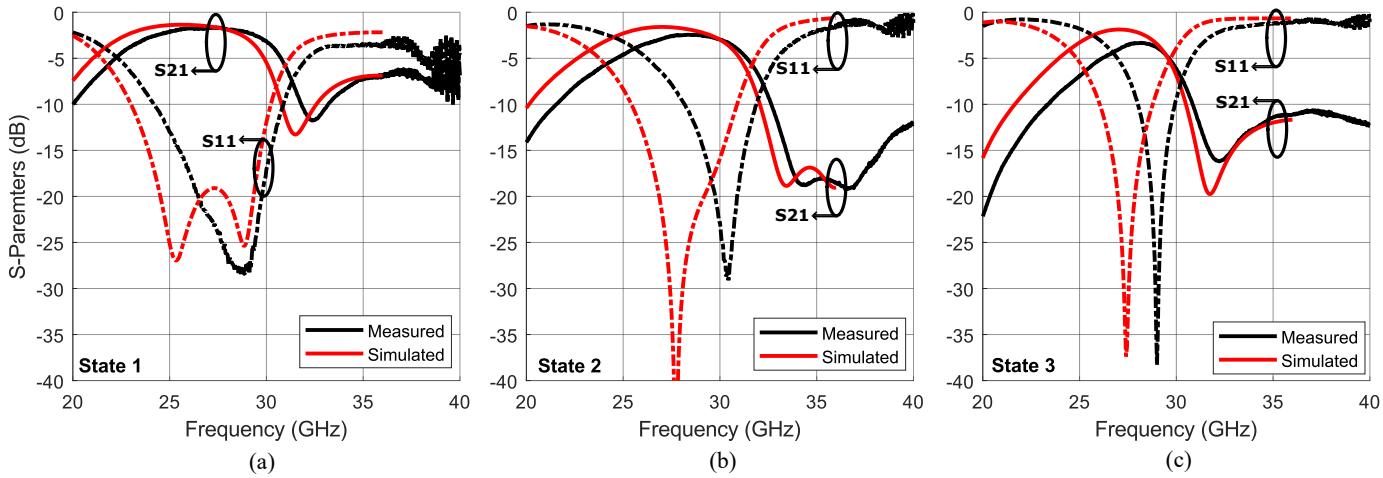

Fig. 5. Magnitude of measured and simulated S21 and S11 for (a) state 1, (b) state 2, and (c) state 3

theoretical back-off efficiency of 37% compared to just 22% for an ideal class B - a comparison that is plotted in Fig 6.

For a post-PA network, the linearity in each state is important. To measure linearity, a Norsat block up-converter with a saturated power of 44 dBm was used to drive the test-bench. The input power was measured with a 20dB coupler and Keysight N1913A power meter while the output was measured on a 67 GHz network analyser. To account for calibration mismatch between source and receiver, the data was smoothed and the loss was normalized to match the low power S-parameters measured previously in a 50Ω environment. After de-embedding cable and probe losses, the insertion loss versus the input power to the network is presented in Fig. 7 with a limiting P1dB of 33 dBm in state 2. The maximum IIP3 measurable on this testbench was 36 dBm of which the linearity of the POLM exceeded.

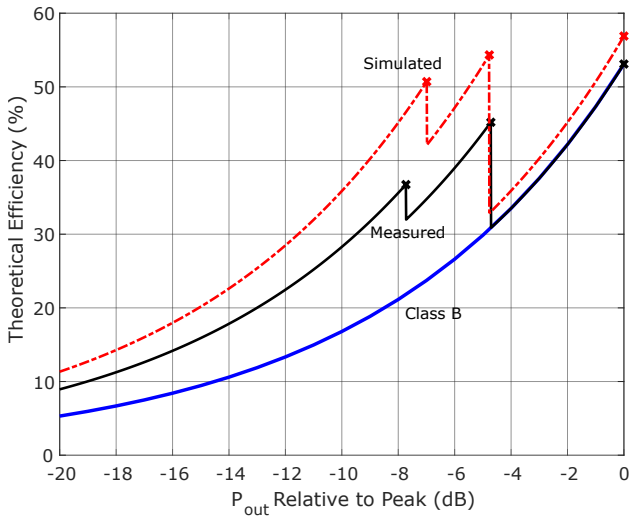

Fig. 6. Potential efficiency improvement for measured versus simulated load modulation networks compared to ideal class B back-off efficiency

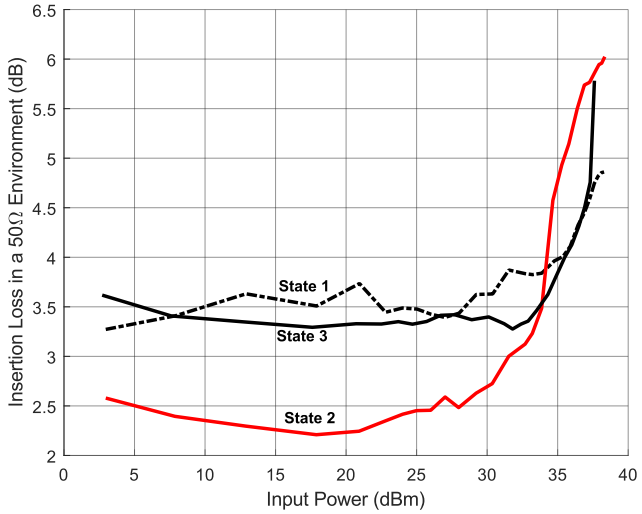

Fig. 7. Insertion loss versus input power for each of the three states measured in a 50 ohm probe environment. Insertion loss appears high because some power is reflected in states 1 and 3 which is accounted for in the x-axis

IV. Conclusion

This work presents a POLM to improve the efficiency of power amplifiers at 28 GHz designed in a 40nm GaN process. The reported switched ring structure allows the impedance to be tuned between 15 and 80 Ω and exhibits a maximum loss of 3.3 dB which is sufficient to offset back-off efficiency degradation in traditional amplifiers. Power handling of the network is greater than two watts due to the high breakdown voltage of the GaN devices.

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