

Reconfigurable Millimeter-wave Power Amplifiers in GaN and SOI using Passive Load Modulation

Rohit R. Karnaty, Shu-Ming Chang, James F. Buckwalter
University of California, Santa Barbara, USA

Abstract—5G applications in millimeter-wave bands have challenging requirements for power amplifiers (PAs) in handsets, picocells, and even basestations, and GaN in basestations. We propose passive outphasing load modulation (POLM) as a generalizable tuning approach that can be applied to various device technologies. Load modulation for high average efficiency as well as static tuning in the presence of load variation is described. The application of POLM to CMOS SOI and GaN PAs at 28 GHz is discussed and verified through measurements of different classes of operation and broadband waveforms.

Keywords—millimeter-wave, power amplifier, load modulation, efficiency, GaN, SOI CMOS

I. INTRODUCTION

Efficiency is an important consideration in millimeter-wave power amplifiers (PAs). As every element in a transmit phased array has a PA, the thermal load of the PA and circuit area are both severely constrained, particularly when scaling above 28 GHz. Technologies that offer excellent output power and efficiency in millimeter-wave bands include SOI CMOS, which natively allows the integration of an entire beamformer, and GaN HEMTs which require a separate MMIC for the PA at each beamformer element. The transmit architecture of a digital beamformer is illustrated in Fig. 1 where an array of power amplifiers (PAs) is driven from a beamformer array. A CMOS SOI technology has been shown to be capable of a peak 25 dBm at 28 GHz [1]–[2]. GaN HEMTs are capable of producing power exceeding 30 dBm [3]. At lower frequency bands, separate silicon and III-V die can be assembled at the limit of cost. At higher frequency bands, the physical dimensions of the array limit the feasibility of a millimeter-wave array that is enabled by silicon and III-V PAs. As more power per element might be provided through CMOS SOI [2] and GaN HEMT [3], the heat generated by these PAs must remain relatively constant, demanding circuit techniques that maximize high efficiency over a range of output powers.

Conventional load modulation approaches are based on a pair of PAs that co-operate under medium and high-power regimes. Outphasing amplifiers operate under constant envelope with a differential phase between the pair of amplifiers [4]. On the other hand, a Doherty amplifier uses a 90° phase shift between PAs that are amplitude modulated to impose a change on the load seen by the main PA [5].

More recently, the load-modulated balanced amplifier (LMBA) shown in Fig. 2 has been demonstrated with tunability at the isolated port for efficiency and matching [6]. While the main and auxiliary PAs are isolated at the peak power and 6-dB backoff power, the tunability has recently been demonstrated

for wideband behavior using a negative capacitance based on non-Foster networks [7].

However, there is no fundamental reason why two PAs are required for load modulation. Moreover, the use of two PAs requires more circuit area and introduces gain variation between the two PAs that demands digital predistortion to compensate. Another approach would use a single high-efficiency PA with tunable load network to solve several problems; not only can it be used to achieve higher efficiency under output backoff (OBO) power but reconfigure the output matching network for antenna VSWR variation [8].

In Section II, we will describe a general approach to passive outphasing load modulation [9]. In Section III, we demonstrate how this approach is applied to SOI CMOS and GaN HEMT device technologies. Section IV describes implementation of the high-efficiency PAs and losses in the POLM circuit.

II. PASSIVE OUTPHASING LOAD MODULATION

The passive outphasing load network illustrated in Fig. 2 is conceptualized as a pair of transmission lines with characteristic impedance, Z_1 and Z_2 , and a differential phase length relative to the total phase around the loop. In other words, the differential phase is $2\Delta = \theta_1 - \theta_2$ and the loop phase is $2\Sigma = \theta_1 + \theta_2$, where θ_2 is the differential phase.

Under the condition that the characteristic impedance of the two arcs are $Z_1 = Z_2 = Z_o$, the input impedance is

$$Z_{in} = \frac{R_L \cos^2 \Delta}{\cos^2 \Sigma + \frac{4R_L^2}{Z_o^2} \sin^2 \Sigma} + j \frac{Z_o}{2} \cot \Sigma \left[\frac{\cos^2 \Delta}{\cos^2 \Sigma + \frac{4R_L^2}{Z_o^2} \sin^2 \Sigma} - 1 \right] \quad (1)$$

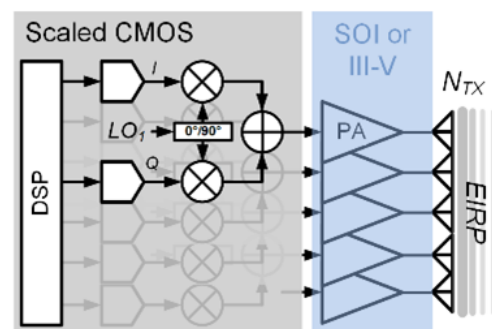


Fig. 1. Block diagram for a millimeter-wave digital beamformer

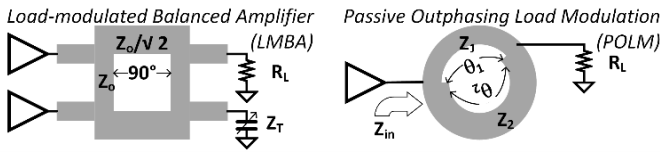


Fig. 2. Millimeter-wave approaches for load modulation in PAs

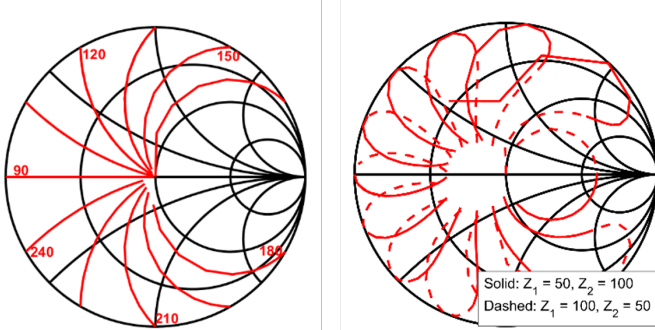


Fig. 3. Load impedance variation for POLM. In the left curve, the variation in $\Sigma\theta$ is plotted as separate trajectories where the $\Delta\theta$ is swept from 0 to 90 degrees and $Z_1 = Z_2 = 100$ Ohms. On the right plot, the trajectories are plotted under the asymmetric choice for characteristic impedance.

The resulting input impedance is plotted in Fig. 3 for different choices of Σ and Δ . First, we consider the input impedance resulting when the characteristic impedance of both arms is equal to 100 Ω . The choice of Σ ranges from 90° to 270° in 15° increments on the left side of Fig. 3 and each curve corresponds to varying Δ from 0° to 90° . For the choice of $\Sigma=90^\circ$, the input impedance changes along the real axis at ranges from 50 Ω when $\Delta=0^\circ$ to 0 Ω when $\Delta=90^\circ$.

On the right plot in Fig. 3, the input impedance sweep is performed under the asymmetric condition on Z_1 and Z_2 as labelled. Notably, the asymmetric choice of characteristic impedance bends the impedance as a function of Δ curves relative to the symmetric solution in Fig. 3.

A technology-specific POLM implementation would fix the total loop phase (Σ) but would allow the differential phase would be varied (Δ). In theory, this would require a switch network to tap different locations around the loop.

III. GAN AND CMOS SOI LOAD MODULATION

To understand the viability of POLM applied to a millimeter-wave PA, we consider two candidate circuit technologies: 45-nm CMOS SOI and 150-nm GaN HEMTs. For the CMOS SOI, we consider a 4-stack FET PA approach at 28 GHz to achieve the peak output power of 24.5 dBm. In Fig. 4, we plot the power added efficiency (PAE) curves to determine the peak PAE at maximum power and 3-dB OBO from the loadpull simulation. The peak power demonstrates more than 24 dBm with an efficiency of 51%. At 3-dB OBO, the efficiency is 46.7% and at 6-dB OBO it is about 32%. The load impedance trajectory between these power levels requires reactive load variation that is illustrated in the Smith chart accompanying Fig. 4. The red curve indicates a

Pin(dBm)	$Z_L(\Omega)$	PAE(%)	Pout(dBm)
8	$43+j90$	46.7	21.7
13	$41+j38$	51.4	24.5

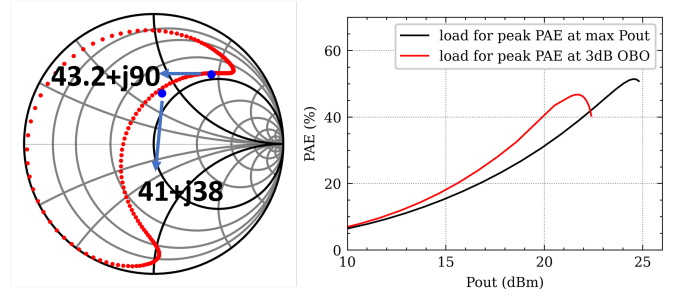


Fig. 4. Load modulation for a CMOS SOI 4-stack differential PA illustrating the change in load impedance for high efficiency

Pin(dBm)	$Z_L(\Omega)$	PAE(%)	Pout(dBm)
24	$3.6+j41.5$	33.7	28
26	$8+j41.5$	34.5	31.5

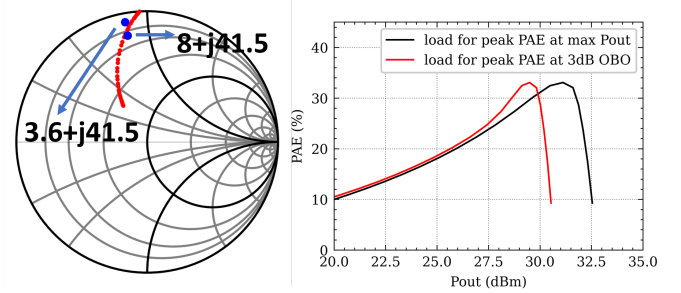


Fig. 5. Load modulation for a GaN HEMT single device illustrating the load impedance variation

specific implementation of the asymmetric load modulation with constant total loop length as discussed previously.

A 150-nm GaN HEMT technology targets an output power of 31.5 dBm using a single common source transistor in Fig. 5 [10]. Whereas the reactive load in the SOI CMOS PA changes significantly, the reactive part of the desired load impedance of the GaN HEMT does not change under the OBO power condition. Therefore, the GaN HEMT is attractive for symmetric load modulation with a resistive loadline variation.

IV. DEMONSTRATION OF A GAN-BASED POLM

Since the POLM can be external to the chip and realized as a separate component between the PA and the antenna, we consider the implementation of the POLM on a GaN substrate to determine the losses of the ring at 28 GHz. A test structure is illustrated in Fig. 6 to measure the losses of the POLM with two different differential states. The ring has been designed with $\Sigma = 90^\circ$, where state 1 corresponds to $\Delta = 0^\circ$ and state 2 corresponds to $\Delta = 56^\circ$.

Fig. 6 shows the measurements of the two states. As predicted, the input impedance at the two different states corresponds with Z_{IN} of $12.3 + j8$ in state 1 and $3 + j11$ in state 2 at 28 GHz. The insertion loss of the POLM is 0.15

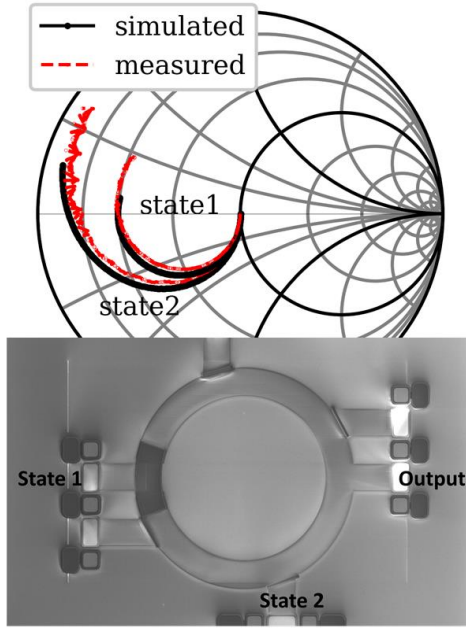


Fig. 6. GaN POLM comparison of simulation and measured input reflection for the 2 states from 10 MHz to 30 GHz with inset microphotograph

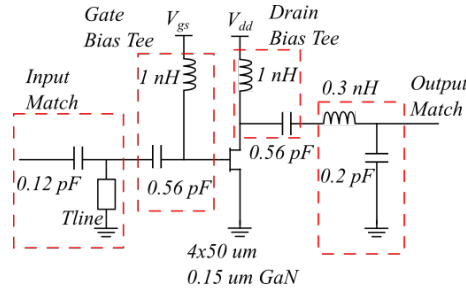


Fig. 7. Schematic of a 28-GHz, class-AB GaN PA

dB in state 1 and 0.4 dB in state 2. Higher insertion losses may result if switches are required to connect to the ring along different outphasing arcs.

The schematic of a 0.15um GaN, 28 GHz PA is shown in Fig. 7 and is capable of watt-level output power with high efficiency. The measured large-signal performance of the class-B GaN PA is illustrated in Fig. 8 for different drain voltages. While the drain efficiency reaches 46% at an output power of 27 dBm, the class-B operation was measured under 20-V and 25-V drain supply conditions. The measured gain and PAE are plotted in Fig. 8. The peak gain is 6 dB for a 25-dBm output power under the 20-V supply. At peak power, the supply can be increased to 25 V to improve the gain by 2 dB and extend the output power to more than 28 dBm at the same efficiency. Hence, the supply voltage can be varied to achieve peak PAE at OBO power conditions.

Fig. 9 shows the layout of the GaN PA core along with POLM on a common substrate. Here, we replace the traditional matching network with the passive ring structure. A cascode topology is introduced to achieve increase the maximum output

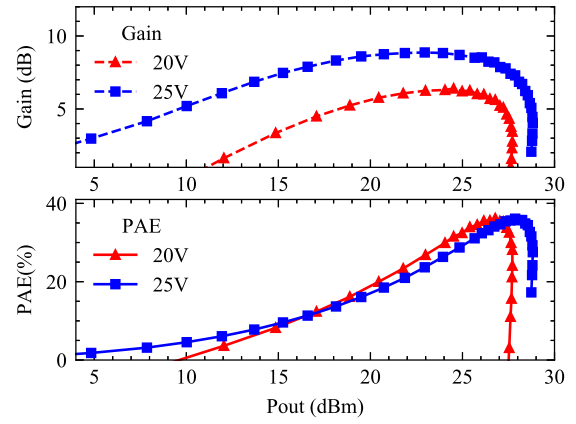


Fig. 8. Comparison of Gain and PAE for $V_{ds} = 20V$ and $V_{ds} = 25V$ (class B).

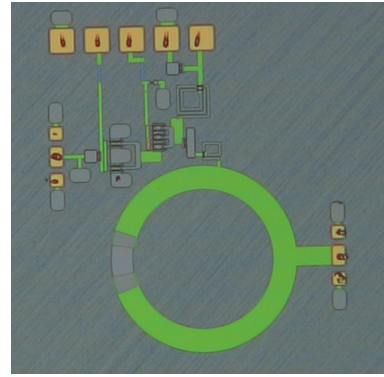


Fig. 9. Microphotograph of the GaN PA core with POLM

power (greater than 30 dBm) and PAE of around 24%. In Fig. 10 the PAE is plotted as a function the output power (Pout). We find excellent agreement between simulation and measurement. At OBO of 10dB, the PAE drops by a factor of 1/2 to 10%.

V. CONCLUSION

This paper discusses opportunities for passive outphasing load modulation for reconfiguration of a millimeter-wave PA to achieve high average efficiency and tunable matching

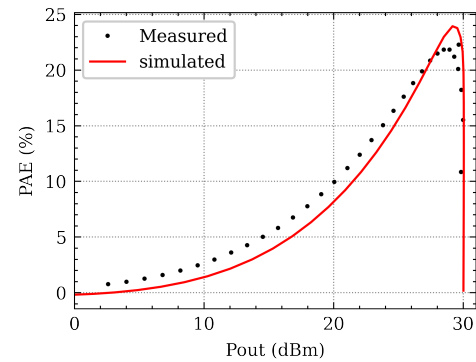


Fig. 10. PAE of the GaN PA as a function of the output power

impedance. We present symmetric and asymmetric load networks and discussed the application to CMOS SOI and GaN device technologies. A prototype GaN POLM was demonstrated to offer a matching impedance variation from 3 to 12 Ohms with insertion loss from 0.15 to 0.4 dB. We also show the implementation of a complete PA design with the POLM integrated with a PAE of 24% at 30 dBm of output power.

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