Analysis of the Sub-μA Fully Integrated NMOS LDO for Backscattering System

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***Abstract*—A fully integrated NMOS low-dropout (LDO) voltage regulator with the ultra-low quiescent current tailored to RF backscattering systems is analyzed. A folded-cascode amplifier is used as the error amplifier implementation to obtain good performance in terms of the loop stability, line regulation, load regulation and power supply rejection ratio (PSRR). The NMOS LDO regulator is simulated in the 180 nm CMOS technology with a 6 nA quiescent current. The line and load regulations are respectively 0.003 mV/V and 8 mV/mA with only 1 pF load capacitor and maximum 10 μA load current. The PSRR is -67 dB at the low frequencies and -22 dB at 1 MHz.**

***Index Terms*—NMOS LDO, backscattering system, folded-cascode, low quiescent current, small load current**

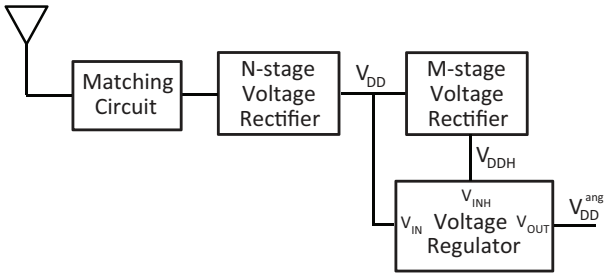

Fig. 1. Conventional block diagram of RF energy harvesting circuit in the sensory system-on-chip designs.

I. Introduction

RF backscattering, a form of wireless transmission based on modulated reflection of external RF signal, has become a promising low-power communication paradigm that enables a realization of passive Internet of Thing(IoT) devices that cover a wide range of applications [1]. Since the source of the RF signal is external, such transmission does not require an 'active' radio transceiver, allowing devices to function in an extremely low power range (under 10 μW). In this power range, the devices operate autonomously from the energy harvested from the external RF signal itself without need for on-board battery [2].

Since the harvested power is scarce and intermittent, a high performance linear voltage regulator is required to produce a stable supply voltage for the analog circuitry. Most of the state-of-the-art low power LDO designs are designed for the mA-level load currents [3]–[8], which is overly high for the RF backscattering systems. We investigate the design of the low power LDO regulators that are tailored to the operating conditions of the RF energy harvesting system-on-chip designs.

There are two types of linear voltage regulators depending on the chosen type of the pass transistor, NMOS and PMOS regulators. The conventionally used topology with PMOS pass transistor due to the low-frequency output pole leads to the complex frequency compensation. Thus, it generally needs a large external capacitor or compensation circuit that occupies a large area for closed loop stability [9]–[12]. The topology with NMOS pass transistor has been used less frequently mostly due to the required boosting of the supply voltage of the error amplifier in order to keep the regulator operating in the low-dropout voltage region. This called for an additional dc-dc converter like a charge pump. However, NMOS topology has many advantages like low output impedance, frequency response, load regulation and small chip area. A fully integrated LDO in 65 nm technology, consuming 970 pA quiescent current, has been previously proposed, demonstrating the advantages of using NMOS pass transistor architecture [13]. We further analyze how this architecture can be tailored to RF energy harvesting devices and explore the limits in the performance of such LDO implementation.

In Section II, the analysis of the fully integrated NMOS LDO regulator, with emphasis on the loop stability and PSRR, is presented. Simulation results are shown in Section III, with the conclusions outlined in Section IV.

II. Integrated NMOS LDO Regulator

In the system-on-chip designs which are powered through the harvested energy, the higher supply voltage than nominal is available due to the additional requirements in the system design. In RF energy harvesting systems, the higher supply voltage is required for powering of control logic and protection diodes and is generated through additional stage(s) in a voltage multiplier [14]. The conventional block diagram of the energy harvesting circuit including the voltage regulator is shown in Figure 1. This eliminates the need for additional voltage boosting circuit in the design of linear voltage regulator with NMOS as pass transistor.

Due to the ultra-low power operation of RF energy harvested system, with the power budgets on the order from few nWs to 10 μW [15], the key constraint in the design of the linear voltage regulator is the quiescent current. The power

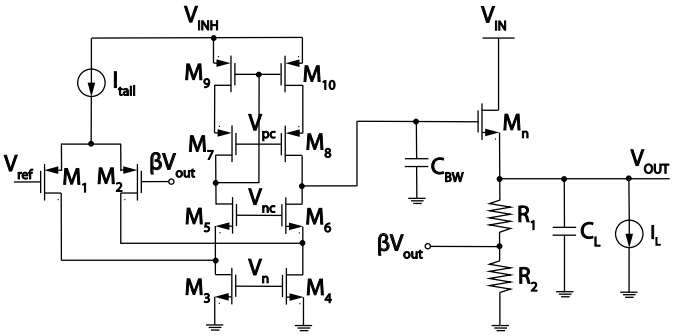

Fig. 2. Schematic of the sub-μA fully integrated NMOS LDO voltage regulator.

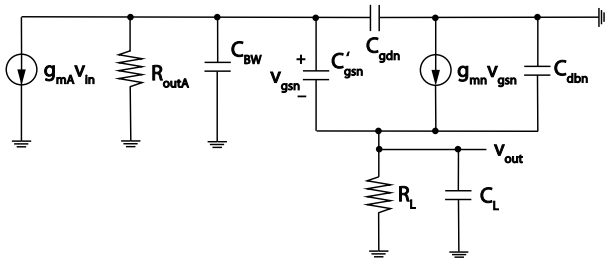

Fig. 3. Small signal model of NMOS LDO regulator.

budget also sets the limit on the load current of regulator that typically ranges from nAs to 10s μA. This is in contrast to the conventional voltage regulators that operate with load currents up to mA range. The RF energy available to harvesting device could be intermittent. These devices conventionally include an energy storage device and the energy supply is shifted from RF signal to the storage capacitor depending on the incident RF energy level. This leads to rapid changes in the input voltage of the regulator and the line regulation is important factor in design of the voltage regulators in these types of devices. This favors the regulators with NMOS pass transistor as NMOS pass transistor behaves as cascode transistor between input and output voltage of regulator [16].

The sub-μA fully integrated NMOS LDO voltage regulator is implemented in the low-cost 180 nm CMOS process, which makes available transistors with nominal voltage supply of 1.8 V. Transistor level regulator design is depicted in Figure 2. The EA is implemented as a folded-cascode amplifier, comprising transistors M_1 to M_{10}. M_n is the NMOS pass transistor. The reference voltage V_{ref} is generated by a bandgap reference, which delivers 600 mV. Feedback resistors R_1 and R_2, implemented as diode connected NMOS transistors, contribute 1.5 nA to the quiescent current. The bias voltages V_n, V_{nc} and V_{pc} are realized by a bias generation circuit. The size of NMOS pass transistor is $W/L = 80\mu m/500nm$ and the transistor is operating in weak inversion region under maximum 10 μA load current, while maintaining a good line and load regulation.

A. Loop Stability

In the design of the error amplifier(EA) in LDO regulator with NMOS pass transistor, the voltage gain and the output voltage range are the most critical constraints. The high voltage gain is required in order to achieve the high loop gain and to improve the PSRR. The output voltage range determines the voltage difference between the supply voltage of the pass transistor and the error amplifier. The differential folded-cascode operational amplifier is chosen as it provides a large low-frequency gain and enables control of the dominant pole of the LDO loop by the variable capacitor, C_{BW}, at the output. In NMOS pass transistor LDO, the domininant pole is at the output of the amplifier and this architecture does not require use of external capacitor at the LDO output. In terms of the output voltage range, compared to the two-stage amplifier implementation, the folded-cascode leads to the increased the supply voltage. The non-dominant pole of EA occurs at the drains of M_1 and M_2 and it is higher than the pole at the output of the LDO.

A simplified small signal model of the NMOS LDO regulator used for the frequency analysis of the open-loop gain is shown in Figure 3. Based on the shown model, the dominant pole w_{p1}, second pole w_{p2} and zero w_z of the LDO open-loop are

$$\begin{aligned} w_{p1} &= \frac{1}{R_{outA}(C_{BW}+C_{gdn})} \\ w_{p2} &= \frac{g_{mn}(C_{BW}+C_{gdn})}{(C_{BW}+C'_{gsn}+C_{gdn})C_L+(C_{BW}+C_{gdn})C'_{gsn}} \\ w_z &= \frac{g_{mn}}{C'_{gsn}}, \end{aligned} \quad (1)$$

where R_{outA} is the output resistance of the error amplifier; g_{mn}, C_{gsn}, C_{gbn} are C_{gdn} are the transconductance, gate-source, gate-bulk and gate-drain capacitance of pass transistor M_n respectively and $C'_{gs} = C_{gs} + C_{gb}$. C_{BW} is the capacitor at the output of the amplifier and C_L is the load capacitor at the output of LDO. Assuming that C_{BW} and C_L are much higher than the transistor capacitances

$$\begin{aligned} w_{p1} &= \frac{1}{R_{outA}C_{BW}} \\ w_{p2} &= \frac{g_{mn}}{C_L} = \frac{\kappa I_L}{U_T C_L}, \end{aligned} \quad (2)$$

where U_T is the thermal voltage. From (2), the dominant pole of the open-loop is controlled by C_{BW} while the second pole is controlled by the loading current and capacitance. This is expected for the architecture with NMOS pass transistor, as NMOS pass transistor provides small output impedance. From the equation for the second pole, we can conclude that no external capacitance is required for improved stability. The stability condition determines the minimum load current as decreasing the load current leads to the lower values of the second pole.

B. Power Supply Rejection Ratio

PSRR is one of the most important specifications in the design of the voltage regulators for the RF energy harvesting

$$
\begin{aligned}
T_1(s) &= \frac{C'_{gs}C_{db8}R_nR_ps^2 + g_{mn}R_nR_pC_{db8}s + g_{mn}\left(R_n+R_p\right)}{C_LC_{BW}R_nR_ps^2 + C_{BW}R_nR_pg_{mn}s + \beta g_{mA}g_{mn}R_nR_p} \\
T_2(s) &= \frac{C_{BW}C_{dbn}R_{outA}r_{on}s^2 + \left(C_{BW}+g_{mn}r_{on}C_{dbn}\right)R_{outA}s + 1}{C_LC_{BW}R_{outA}r_{on}s^2 + C_{BW}R_{outA}g_{mn}r_{on}s + R_{outA}\beta g_{mA}g_{mn}r_{on}}
\end{aligned} \tag{3}
$$

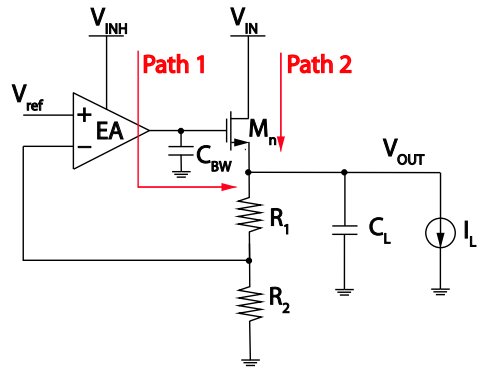

Fig. 4. Two noise paths for analysis of PSRR of NMOS LDO regulator.

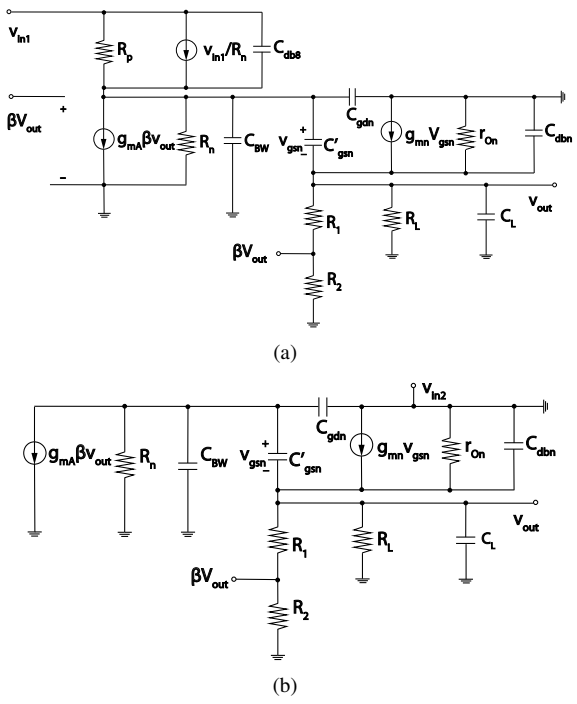

Fig. 5. (a) Small signal model of Path 1, (b) Small signal model of Path 2 for the computation of PSRR.

devices. Figure 4 illustrates the two noise paths from V_{in} through the supply voltage of the error amplifier (Path 1) and pass transistor M_n (Path 2) to the output of the LDO.

The small signal models for PSRR computation for both paths are shown in Figure 5. In the simplified small signal model for PSRR of EA [17], R_n and R_p are the resistances looking up and down into the drain of M_8 and M_6,

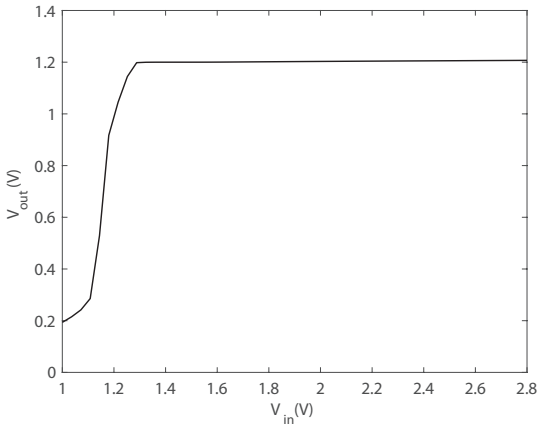

Fig. 6. Output voltage of the LDO regulator as a function of input voltage.

respectively. C_{db8}, between V_{inH} and output of EA, is the junction capacitance of drain to substrate of M_8. C_{dbn} is the junction capacitance of drain to substrate of M_n. The following simplified equations for PSRR transfer functions of the both small signal models can be derived as (3). The overall PSRR transfer function presents the addition of the transfer function for these two paths.

III. Simulation Results

The fully integrated NMOS LDO voltage regulator is designed in 180 nm CMOS technology and simulated in Cadence simulation environment. Output voltage of the regulator, V_{out}, is set at 1.2 V and the regulator is designed to operate with the input voltage V_{in} of 1.4 V, thus the nominal dropout voltage is 200 mV. The simulated I_Q is 6 nA. We first show the dependence of the output voltage on the input voltage of the regulator in Figure 6, with the dropout voltage as low as 100 mV. For all values of the input voltage, the voltage V_{inH} is 400 mV higher than V_{in}.

The open-loop gain is shown in Figure 7 for the minimum and maximum value of the load current, I_L, 5 nA and 10 μA, as well as for the two different values of the loading capacitor, which represents the capacitance of the circuit supplied by the regulator. We can notice that the dominant pole does not depend on the loading conditions. The second pole reaches the lowest value, as predicted by (2), for the minimum loading current and the larger value of the loading capacitance.

Figure 8 shows that the line regulation of the LDO for the 200 mV step in the input voltage is 0.003 mV/V. Figure 9 depicts the output voltage when the loading current I_L, with the rise and fall time of 50 ns, is changed between 5 nA and

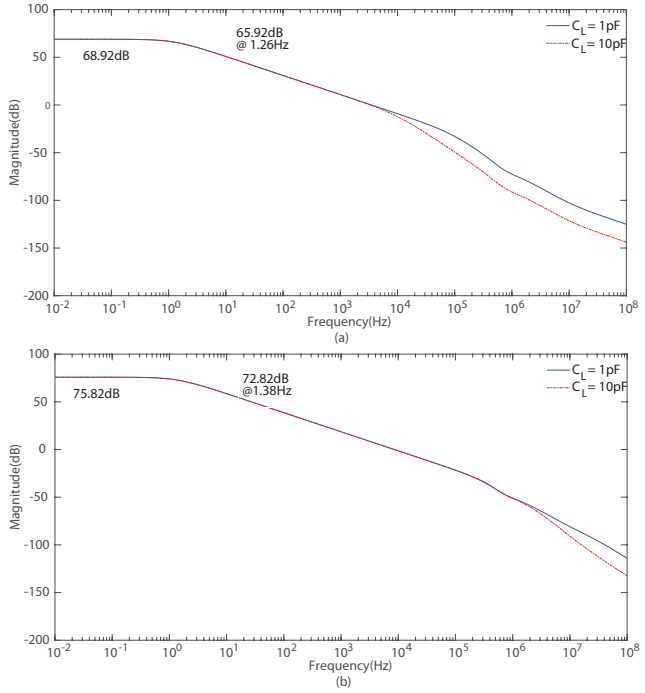

Fig. 7. Open-loop gain for (a) I_L = 5 nA and (b) I_L = 10 μA for the value of capacitance C_{BW} equal to 0.5pF.

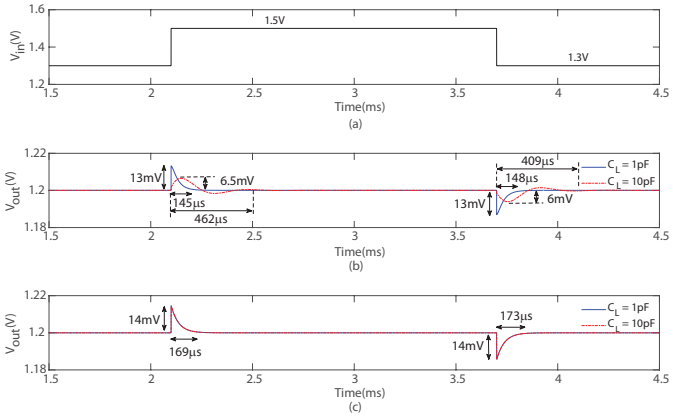

Fig. 8. Line regulation for the change of input voltage from 1.3 V to 1.5 V for the loading current (b) I_L = 5 nA and (c) I_L = 10 μA.

10 μA. The load regulation is 8 mV/mA. The rise and fall time with 1% precision are 189 μs (313 mV undershoot) and 189 μs (197 mV overshoot) when I_L changes from 5 nA to 10 μA and then to 5 nA, respectively.

Fig. 10(a) shows the comparison of the derived PSRR transfer function (3) and the simulation result. PSRR is set by the gain of the amplifier at low frequencies and equals -67 dB, while it is -34.9 dB at 1 kHz and -22 dB at 1 MHz, as shown in Figure 10(b). For moderate frequencies, the PSRR will be the same as in Path 2 after the corner frequency $f_c = f_{p1} g_{mn} r_{on}$, which is 128 Hz in the design. Path 2 is the critical path for PSRR after lower frequency range. From (3), since the second zero f_{zb} is far more higher than the first zero f_{za}, they can

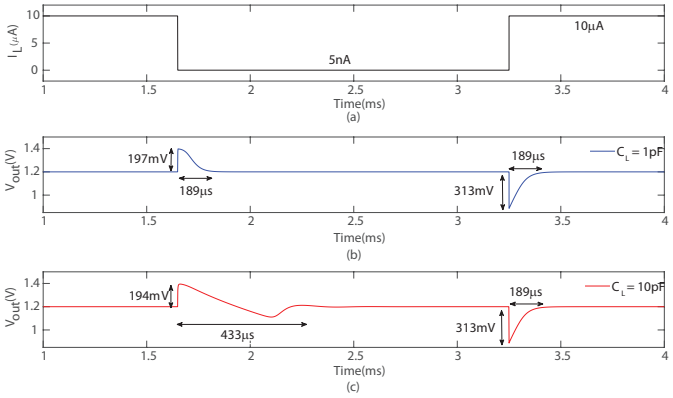

Fig. 9. Load regulation for the change of the loading current from 5 nA to 10 μA.

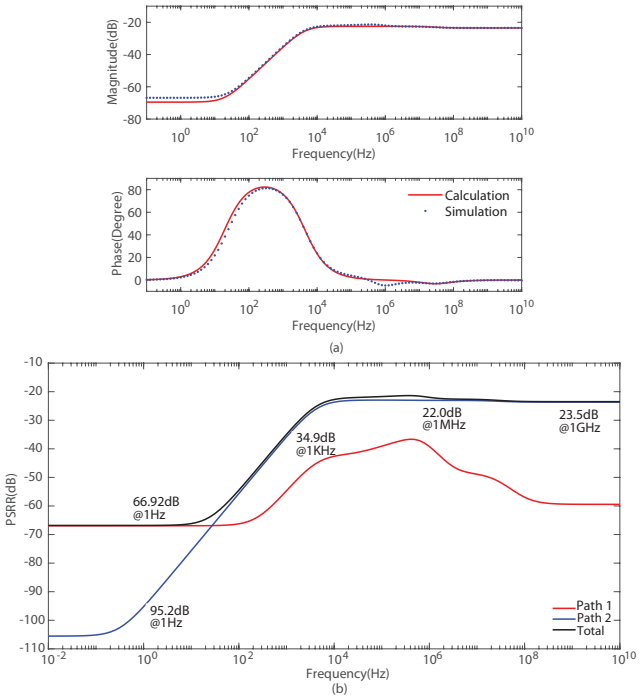

Fig. 10. (a) PSRR magnitude and phase comparison between the calculation and simulation of the total paths, (b) Simulated PSRR of Path 1, Path 2 and overall transfer function.

be expressed as following

$$f_{za} = \frac{1}{2\pi(C_{BW} + g_{mn} r_{on} C_{db}) R_{outA}} \tag{4}$$

$$f_{zb} = \frac{1}{2\pi}\left(\frac{1}{C_{dbn} r_{on}} + \frac{g_{mn}}{C_{BW}}\right) \tag{5}$$

The two poles f_{pa} and f_{pb} are:

$$f_{pa} = \frac{C_{BW} g_{mn} - \sqrt{C_{BW} g_{mn}(C_{BW} g_{mn} - 4 C_L \beta g_{mA})}}{4\pi C_{BW} C_L} \tag{6}$$

$$f_{pb} = \frac{C_{BW} g_{mn} + \sqrt{C_{BW} g_{mn}(C_{BW} g_{mn} - 4 C_L \beta g_{mA})}}{4\pi C_{BW} C_L} \tag{7}$$

TABLE I
PERFORMANCE COMPARISON

	[3]	[4]	[5]	[6]	[7]	[8]	This Work
Year	2016	2016	2018	2018	2020	2020	2021
CMOS Technology(nm)	180	180	65	180	55	40	180
V_{in}(V)	1.4	1.4	1	1.2	0.8	1.1	1.4
V_{out}(V)	1.2	1.2	0.8	1	0.6	0.9	1.2
V_{DO}(mV)	200	200	200	200	200	200	200
I_{load}(mA)	100	50	10	10	10	100	0.01
Load Capacitor(pF)	100	4.7×10^5	10	100	10^6	100	1
Quiescent Current(nA)	61	900	30	407	16	20	6
Line Regulation(mV/V)	0.6	7.25	N/A	0.283	0.5	4.8	0.003
Load Regualtion(mV/mA)	0.27	0.14	1.58	0.077	1.05	0.0379	8
Settling Time(μs)	N/A	0.4	0.1	1.56	N/A	0.354	189.86
PSRR(dB)	-26@1MHz	-42@1MHz	-24@1MHz	-37.7@1MHz	-42.7@50kHz	-32.12@1MHz	-22@1MHz
FOM(ps)	0.001189	4	0.00159	286.65*	11.4	680.36*	4.82

* FOM is recalculated based on the equation in [9]

From (4), (5), (6) and (7), C_{BW} and C_L are important parameters to adjust PSRR once the design of EA and NMOS pass transistor is done. f_{za}, f_{zb} and f_{pa} increase with the decreasing of C_{BW}, while f_{pb} declines; f_{pa} increases, and f_{pb} reduces with decreasing of C_L. However, f_{za} and f_{zb} are constant. Hence, in order to obtain a better PSRR, a larger C_{BW} can be used to turn PSRR flat earlier at low frequencies rather than continuing to rise. Further, a larger C_L can be used to move the second zero higher and the second pole lower, which leads PSRR to drop lower at high frequencies.

The comparison with the state-of-the-art designs is shown in Table I. The LDO in this work has an equivalent 1 pF load capacitor. With the 10 μA maximum load current and 6 nA low quiescent current, the LDO still achieves an acceptable transient performance. Based on the figure of merit(FOM) proposed in [9]

$$FOM = C_L I_Q \Delta V / \Delta I^2 \tag{8}$$

the proposed integrated NMOS LDO shows a competitive FOM with respect to other reported state-of-art designs.

IV. CONCLUSION

A fully integrated NMOS LDO with 6 nA ultra-low quiescent current for RF energy harvesting devices is analyzed and designed. The design will be fabricated in the 180 nm technology to verify the simulation results and to address the performance of LDO under different matching and temperature conditions.

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