1.81 kHz Relaxation Oscillator With Forward Bias Comparator and Leakage Current Compensation Based Techniques

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***Abstract*—We propose a 1.81 kHz on-chip relaxation oscillator implemented in 0.18 μm CMOS technology without trimming. The first order temperature coefficient (TC) is compensated by leakage current. The stability is further enhanced by a forward bias comparator that suppresses offset variation. The oscillator consumes 11.69 nW from a 0.8 V power supply and the TC is 49.3 ppm/°C for a temperature range from -20°C to 80°C . The simulated line sensitivity is 1.8% with voltage supply ranging from 0.5 V to 2.0 V.**

***Index Terms*—Internet-of-things, low power, temperature compensation, line sensitivity, relaxation oscillator**

I. Introduction

For granular and long-term environmental monitoring using wireless sensor networks [1] or activity monitoring using RF tags [2], the sensory systems have to operate powered by the harvested energy [3]. The biomedical implants have the similar power requirements [4]. Common to these devices is that they are conventionally implemented as an ultra-low power system-on-chip (SoC) that relies on a portable and stable timer or clock generator.

In a typical wireless sensor node, crystal oscillator with frequency in kHz range provides both high accuracy and low power with power consumption on the order of nWs [5]. However, the external component results in a larger board area and higher cost, motivating the requirement for a fully-integrated clock source. Compared with ring oscillator (RO) [6], relaxation oscillator has better temperature and supply voltage stability and is a promising candidate to realize a low-cost and low-power on-chip clock signal.

The conventional design of the on-chip relaxation oscillator integrates a voltage reference and a comparator. The application limits on the TC and line sensitivity of the oscillator pose stringent requirements on the implementation of resistors and capacitors, the delay and offset voltage of comparator and logic circuit delay. In the most circuit implementations, the composite resistors are generally employed to realize a resistance with zero TC to remove frequency variation from the timing resistor. The metal-insulator-metal (MIM) capacitor is used for temperature tolerance and the variance is negligible.

In the relaxation oscillator design with the frequency in the kHz range, the delay and offset voltage (V_{os}) of comparator are typically the main sources of the frequency uncertainty. The propagation delay due to limited comparator bandwidth is a parameter strongly dependent on the temperature and the supply voltage. Due to the low supply voltage in SoC design (0.6 V to 1.1 V) in 0.18 μm CMOS process, all circuits operate in subthreshold or near-threshold region. The propagation delay increases as the temperature drops. Offset of the comparator causes frequency instability. The offset voltage component that stems from the process variations results in a frequency shift, while the temperature dependence of the offset voltage leads to a residual temperature coefficient of the oscillator. The process variations can be removed by a one-time calibration, but the temperature variance pertains. Additionally, the variations in the supply voltage and the aging effects impact the offset voltage.

A range of different architectures, as well as comparator designs have been proposed in the literature to address these issues. An integrated error feedback that includes extra two capacitors and an op-amp is employed to cancel the comparator delay variation caused by temperature [7]. Two integrator-comparator technique measures and cancels the comparator delay by an opposite-phase replica comparator [8]. Different approaches have been utilized for removing the nonidealities of the comparator with the cost of extra power consumption. The comparator designed with constant-g_m biasing, two matched capacitors and switched RC scheme in order to achieve constant comparator delay operates with higher voltage headroom [9]. With the increased design complexity, the comparator delay can be removed with two digital compensation loops [10].

We present a 1.81 kHz relaxation oscillator design with a TC of 49.3 ppm/°C tailored for a low power Internet-of-things (IoT) device. The proportional-to-absolute-temperature (PTAT) comparator delay is counteracted by a nonzero starting voltage for timing capacitor via a leakage current. A novel forward bias comparator reduces the frequency variance by stabilizing the input voltage offset with near zero power consumption.

The paper is organized as follows. Section II contains the circuit implementation. Section III presents the simulation results followed by the conclusion in Section IV.

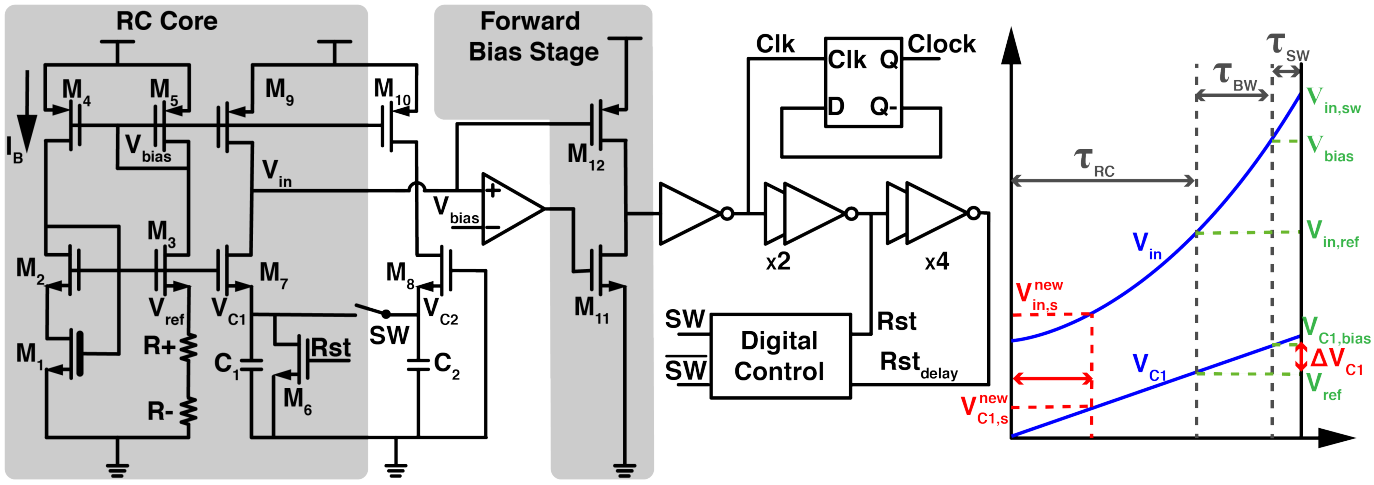


Fig. 1. Architecture of the proposed oscillator and the model of oscillator period due to limited bandwidth and offset of the common gate amplifier.

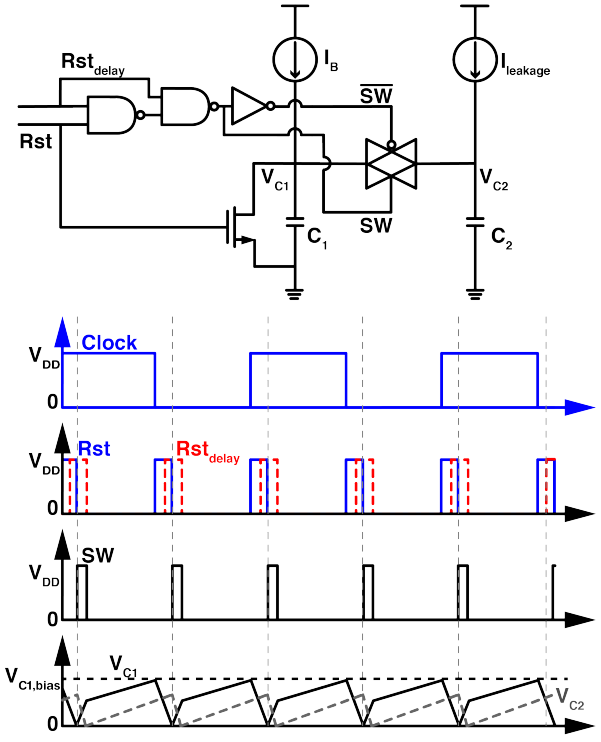


Fig. 2. Logic circuitry and timing waveform.

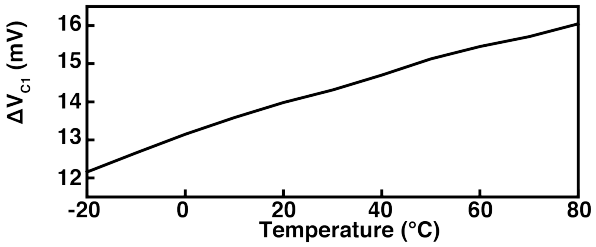


Fig. 3. Simulated drifted ΔV_{C1} with temperature variation from -20 °C to 80 °C.

II. Circuit Implementation

A. System Overview

Fig. 1 shows the system diagram of the proposed oscillator that contains a CTAT bias current I_B supplied by a reference voltage generator, a time constant RC core, a forward bias comparator and a leakage current based compensation (LCBC) block.

The oscillator clock period is determined by the time constant RC core, which comprises resistors R_+ and R_- and the time defining MIM capacitor C_1. C_1 is charged by the replica bias current I_B and triggers the output of the comparator when capacitor voltage V_{C1} exceeds the reference voltage V_{ref}. The following inverter chain outputs the clock signal through a D flip-flop and generates the sufficiently long reset pulse for switch M_6 to discharge the C_1 immediately and avoids a residual charge on C_1. During the charging and reset phase, the compensation capacitor C_2 is charged to a voltage that increases with temperature and is used to reduce the TC of oscillator. At the end of reset phase, a simple digital circuitry opens switch SW and connects C_1 and C_2 to transfer the charge from C_2 to C_1. A nonzero starting point $V_{C1,s}^{new}$ is provided for C_1.

The period T_{osc} of the relaxation oscillator is expressed as

$$T_{osc} = \tau_{RC} + \tau_{BW} + \tau_{sw} \tag{1}$$

This is graphically illustrated in Fig. 1, where $\tau_{RC} = \frac{V_{ref}C_1}{I_B}$ is the time determined by the capacitor charging and discharging period. Taking into account the limited bandwidth of the common gate transistor M_7, V_{in} does not follow the ramp input V_{C1} and τ_{BW} is the additional time for V_{in} to exceed V_{bias}. τ_{sw} is the remaining time resulting from the input offset of the comparator. The additional part of T_{osc} comes from the digital and reset circuit which has a little impact on the overall temperature stability. The detailed design will be addressed in the following sections.

B. Reference Generation

The bias current generator is the most crucial building block for the RC oscillator that defines the overall temperature behavior. The beta-multiplier circuit is commonly used to generate PTAT current source, with additional 34% power consumption from feedback amplifier [11].

A voltage reference that composes NMOS transistors with the different gate-oxide thicknesses [12] is utilized, and the structure is shown in the Fig. 1. Transistor M_2 is a nominal 1.8 V NMOS transistor, whereas the transistor M_1 has a thick gate oxide. The reference voltage V_B, that depends on the threshold voltage difference and size ratio, is insensitive to supply voltage, has good linearity of temperature and is given as

$$V_B \approx (V_{TH,M_2} - V_{TH,M_1}) + \eta V_T ln(\frac{t_{OX,M_2} W_{M1}/L_{M1}}{t_{OX,M_1} W_{M2}/L_{M2}}) \quad (2)$$

where the first term has a negative TC and the second term has a positive TC. By properly sizing the transistors, a CTAT reference voltage V_B is implementated. The bias current source I_B is realized by V_B through resistors. A 9.95 $M\Omega$ P-type poly resistor without salicide R_- with a negative first-order TC and a 5.12 $M\Omega$ N-type poly resistor with salicide R_+ with a positive first-order TC are combined to achieve a low TC resistor that is used to reduce TC of I_B. Although I_B and V_{ref} are CTAT, the first-order TC of τ_{RC} can be removed.

C. Leakage Current Based Compensation Circuit (LCBC)

The finite bandwidth of M_7 introduces a temperature dependent time constant τ_{BW} into the oscillator period, and is given as [11]

$$\tau_{BW} = (1 - e^{-\frac{T_{osc}}{\tau_{M7}}})\tau_{M7} \quad (3)$$

As shown in the model in Fig. 1, V_{C1} further increases from V_{ref} to $V_{C1,bias}$, where ΔV_{C1} can be expressed as

$$\Delta V_{C1} = \tau_{BW} I_B / C_1. \quad (4)$$

τ_{BW} depends on the output resistance and load capacitance at the drain of M_7 and exhibits a PTAT dependence on temperature. I_B is a CTAT bias current and when multiplied by the PTAT τ_{BW} results in a CTAT ΔV_{C1}, as shown in Fig.3.

We propose a method to compensate τ_{BW} with a PTAT leakage current source as illustrated in Fig. 2. The gate of transistor M_8 is connected to ground, and the transistor's drain current I_D, as transistor operates in weak inversion, is given as

$$I_D = \frac{W}{L I_0 exp(\frac{V_{GS}-V_{TH}}{\eta V_T})[1 - exp(-\frac{-V_{DS}}{V_T})]} (5)$$

where $I_0 = \mu C_{ox} \cdot V_T^2 \cdot (\eta - 1)$, μ is the carrier mobility, C_{ox} is the gate-oxide capacitance, V_T is the thermal voltage, V_{TH} is the threshold voltage of the NMOS transistor, and η is the subthreshold slope factor. M_{10} operates in cutoff region in order to keep $V_{DS,M8}$ much larger than V_T and the transistor M_8 in saturation.

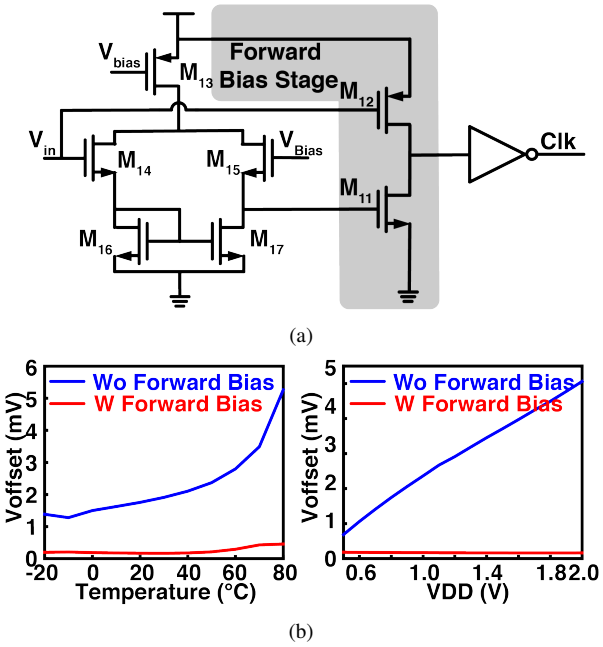


Fig. 4. (a) Proposed forward bias comparator, (b) Simulated results of the offset voltage versus temperature and supply voltage.

Fig. 2 shows the schematic of LCBC and related timing waveforms. The LCBC is composed of a storage capacitor C_2, a pass transistor and digital control circuit.

Consider one-clock operation of LCBC as an example. When the V_{in} reaches $V_{in,sw}$, the $Clock$ signal changes. Two inverters are used to generate a long enough reset signal. V_{C1} is discharged immediately, whereas V_{C2} keeps charging during the reset phase. When the falling edge of Rst is sensed, SW is pulled up. The pulse length depends on the time delay between Rst and Rst_{delay} and is 465 ns at 25 °C. Subsequently, C_1 is connected to C_2. C_2 is discharged to $V_{C1,s}^{new}$ and V_{C1} rapidly rises to non-zero starting point for the next charging phase. The $V_{C1,s}^{new}$ depends on the ratio of C_1 and C_2, that is

$$V_{C1,s}^{new} = \frac{C_2}{C_1 + C_2} \cdot \tau_{BW} I_{leakage} / C_2 \quad (6)$$

The $V_{C1,s}^{new}$ is designed to cancel the first-order temperature dependence of ΔV_{C1}.

D. Forward Bias Comparator

The input offset voltage $V_{os} = V_{sw} - V_{bias}$ of comparator varies $\pm 37\%$ for temperature increasing from -20 °C to 80 °C and leads to τ_{sw} variation. In order to realize a constant T_{osc}, comparator is improved with implementation of forward bias technique.

In a conventional scheme, an inverter follows the comparator and the switching voltage is written as

$$V_{SW,inv} \approx \frac{1}{2}[V_{DD} - nV_T ln(\frac{K_N}{K_P}) - |V_{th,p}| + V_{th,n}] \quad (7)$$

$V_{SW,inv}$ depends on the supply voltage, NMOS threshold voltage $V_{th,n}$ and PMOS threshold voltage $V_{th,p}$. Simulation

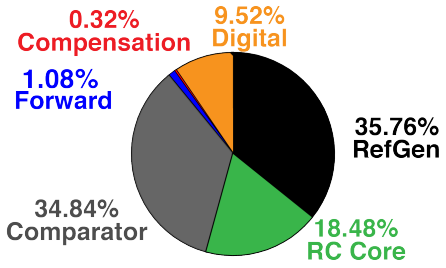


Fig. 5. Power distribution in the proposed relaxation oscillator.

results show that $V_{SW,inv}$ has a PTAT dependence. A condition for the inverter to reach the switching threshold is given by

$$G_m S_{Vin} T_{sw}^2 = C_{inv} V_{SW,inv}$$
$$V_{os} = \frac{C_{inv} \Delta V_{SW,inv}}{G_m T_{sw}} \quad (8)$$

where G_m is the transconductance of comparator, S_{Vin} is the slope of input voltage and C_{inv} is the input capacitance of inverter. V_{osc} exhibits a PTAT dependence and supply voltage sensitivity caused by $\Delta V_{SW,inv}$, as shown in Fig. 4(b).

A forward bias technique is adopted in Fig. 4(a) to suppress the τ_{sw} variation. The gate of top PMOS M_{12} is connected with V_{in} rather than the output of comparator. When V_{C1} approaches $V_{C1,bias}$, M_{12} turns off first and activates the later inverter before turning on M_{11}. As the temperature increases, the leading time between M_{12} and M_{11} keeps and relaxes the V_{os} variation.

As illustrated in Fig. 4(a), the offset voltage rapidly increases with the temperature without using the forward bias stage. In contrast, when employing the forward bias, the drifting offset voltage can be mitigated at around 200 μV by dynamically adjusting the switching point of the M_{11} and M_{12}. 200 times Monte Carlo simulations were conducted to check the V_{os} variation under different temperature and supply voltage. In summary, the forward bias technique improves the V_{os} 20 times compared to the conventional comparator with additional 3% of power consumption.

III. Simulation Results

The proposed relaxation oscillator is designed and implemented in 180 nm CMOS process. Operating at 0.8 V, the output frequency is 1.81 kHz with 11.57 nW power consumption at room temperature (25 °C). 35.76% of power is consumed by the reference generator and 34.84% is consumed by the comparator. The forward bias and leakage compensation circuits consume less than 1.5% power of the whole design.

Fig. 6 shows the simulated digital control signal and voltage of capacitors at 80°C. C_1 is fully discharged to ground from 50 mV, 1 μs after Rst signal is pulled up and stays at 0 V for 6 μs until the reset phase is done. A delay reset signal Rst_{delay} forms compensation SW control signal to provide a non-zero starting voltage for V_{C1}. At the end of compensation

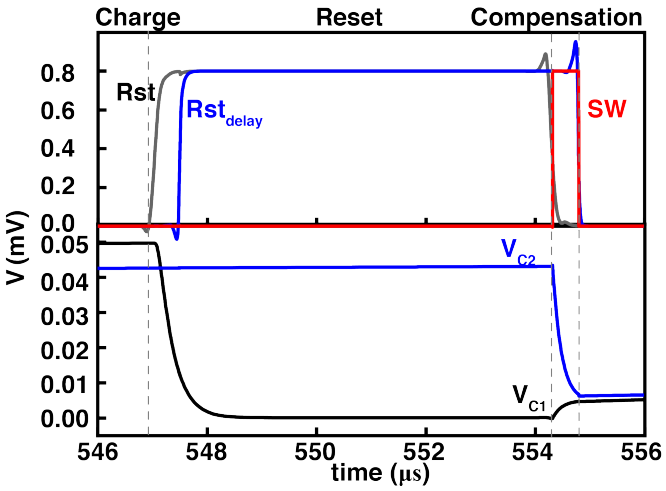
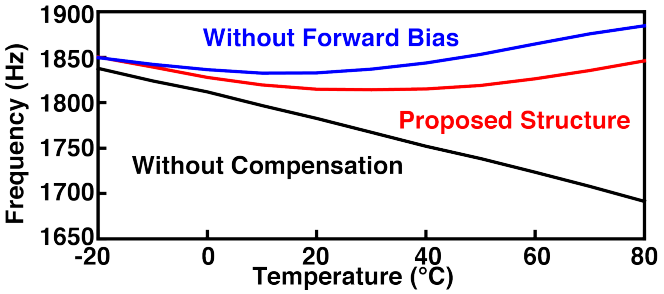
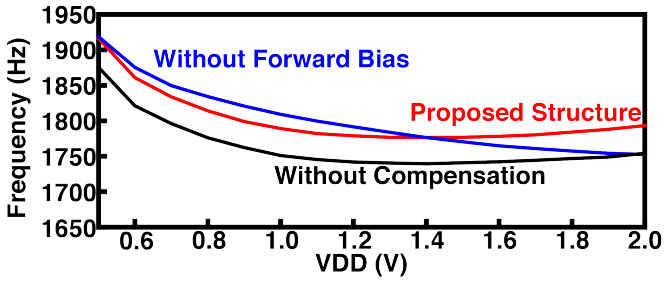


Fig. 6. Simulated waveforms for proposed oscillator at 80 °C .



(a)



(b)

Fig. 7. (a) Simulated frequency of oscillator versus the temperature at 0.8V. (b) Simulated frequency of oscillator versus the supply voltage at 25^0C.

phase, V_{C1} and V_{C2} are both balanced at around 6 mV. Then a replicated clock cycle runs.

A. Temperature Variation

The simulated frequency stability against temperature is shown in Fig.7(a) for the proposed relaxation oscillator without compensation and without forward bias circuits in temperature range from -20°C to 80°C. Respectively, the temperature coefficients are shown as ± 49.3 $ppm/°C$, ± 208.2 $ppm/°C$ and ± 70.0 $ppm/°C$. The improvement is achieved with 1.40% additional power. The residual frequency shifting comes from the digital control circuitry and current

TABLE I
SUMMARY AND COMPARISON WITH LITERATURE

	Year	Tech (nm)	Frequency (kHz)	Power (nW)	Supply (V)	Temperature Coefficient (ppm/°C)	Line Sensitivity (%/V)	FOM (nW/kHz)	Result
Paidimarri, JSSC [9]	2016	65	18.5	130	1	20 @-40 $\sim$ 90	5	7.02	Measured
Yao, ISNE [13]	2019	180	29.59	253.27	1	450 @-20 $\sim$ 80		8.55	Simulated
Asano, ISCAS [14]	2017	65	32.5	271	1.1	138 @-40 $\sim$ 80	1.39 @1.1 $\sim$ 1.3	8.33	Simulated
Ma, ISCAS [15]	2017	65	64.2	8960	1.2	14.69 @-20 $\sim$ 120	0.188 @1.2 $\sim$ 2.3	139.56	Simulated
Zheng, TCAS-II [16]	2018	180	364	1360	1.2	70 @-20 $\sim$ 90		3.74	Measured
Sun, ASICON [17]	2019	180	190	2400	1.8	197 @0 $\sim$ 125	0.84 @1.7 $\sim$ 1.9	12.63	Simulated
Chiang, TCAS-II [12]	2014	180	28	40	1.2	95.5 @-20 $\sim$ 80	1.48 @1.0 $\sim$ 2.0	1.42	Measured
Denier, TCAS-I [18]	2010	350	3.3	11	1	>1000 @-20 $\sim$ 80	3.5 @1.0 $\sim$ 4.0	3.36	Measured
Dai, CICC [19]	2015	180	122	14.4	0.6	327 @-20 $\sim$ 100	6 @0.6 $\sim$ 1.8	0.12	Measured
Jiang, JSSC [11]	2018	180 (SOI)	1.22	1.44	0.4	94 @-20 $\sim$ 70		1.18	Measured
This work	2021	180	1.81	11.57	0.8	49.3 @-20 $\sim$ 80	1.8 @ 0.5 $\sim$ 2.0	6.36	Simulated

reference, which usually contributes second order temperature effects.

B. Line Sensitivity

The measured frequency variation against the supply voltage is plotted in Fig. 7(b). The proposed design indicates a 1.8% frequency variation as the supply changes from 0.5 V to 2 V. In the conventional relaxation oscillator, the low line sensitivity is realized with bandgap voltage reference, which adds extra power consumption and higher supply headroom. The forward bias technique improve the line sensitivity 22% with 125 pW power.

C. Performance Comparison

TableI summarizes the performance of our proposed structure and compares it with the state-of-the-art kHz-range relaxation oscillator designs. The figure of merit energy per cycle is defined as

$$FOM = \frac{P}{f_{osc}} \tag{9}$$

where P is the power consumption and f_{osc} is the oscillation frequency. A lower energy per cycle signifies higher power efficiency. The FOM value is 6.36 nW/kHz. The proposed design demonstrates the comparable efficiency without trimming and external components. The proposed oscillator provides a good trade-off between temperature coefficient, line sensitivity and power consumption.

IV. CONCLUSION

1.81 kHz relaxation oscillator is designed in 180 nm CMOS process without the off-chip components and trimming. 49.3 ppm/°C temperature stability is realized by leakage current compensation. Forward bias technique further improves the line sensitivity and temperature dependence of comparator offset. Simulation results validate the proposed relaxation oscillator and indicate a promising fully integrated clock source for IoT SoCs.

ACKNOWLEDGMENT

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