Internal-Distributed CDM ESD Protection

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Abstract

CDM ESD protection is a major ESD protection design challenge for advanced ICs, often suffering from random design failures. It was recently reported that the traditional pad-based CDM ESD protection method is fundamentally faulty, contributing to design uncertainties in CDM ESD testing and field failures. This paper reports a novel internally distributed CDM ESD protection method to overcome this major design challenge, which was validated using an internal-CDM-protected oscillator IC implemented in a foundry 45nm SPO CMOS technology. (Keywords: ESD, CDM, SOI, VFTLP, distributed)

I. Introduction

On-chip ESD protection is required for all ICs. Constant advances have been made to ESD protection solutions and design techniques [1-3]. For decades, conventional pad-based ESD protection schemes have been used for almost all ESD protection designs, which work effectively to protect ICs against the external-oriented "from-external-to-internal" types of ESD events, such as HBM, MM and IEC ESD test models [1]. Nevertheless, the classic pad-based ESD protection method does not seem to be effective for CDM ESD protection, which has been notoriously uncertain and unreliable in ESD testing and features random ESD field failures, making CDM ESD protection design extremely challenging today for complex ICs in advanced technologies [4-6]. Recently, we reported that the classic pad-based CDM ESD protection method is theoretically wrong, which is the root cause to the CDM ESD protection design uncertainties that has been haunting the IC industry [6].

Fig. 1 illustrates the classic pad-based CDM ESD protection scheme, where ESD devices between pads serve to shunt the ESD pulses to ground and clamp the pad voltage to a safely low level for ESD protection. It works nicely for external-oriented ESD events because the incident ESD transients can be blocked at the pad from getting into the IC core. Unfortunately, this pad-based ESD protection method may not work for CDM ESD protection that is internal-oriented "from-internal-to-external" ESD event in nature. For CDM ESD events, static charges are introduced to ICs during the entire lifetime, and are accumulated locally and distributed randomly inside the IC cores. Theoretically, even if an ESD protection device at pad functions nicely during an CDM ESD event, when the static charges stored inside an IC core flow outward and discharge through the pad-based ESD device, possible internal CDM ESD failures may still occur along the internal charge-flowing path as depicted in Fig. 1 [6]. Fig. 2 illustrates another CDM ESD failure example where substantial charges are stored locally around a large MOSFET and some internal charges will inevitably run through the S/D junction or the gate in the path, resulting in CDM ESD failures regardless of the pad-based ESD protection. Moreover, the widely used field-induction CDM (FICDM) testing method cannot simulate the random distribution nature of CDM charge storage inside an IC die and hence may cause various CDM ESD testing errors [6]. In summary, it is believed that the widely used pad-based CDM ESD protection method is fundamentally faulty, which may be the reason to the random CDM ESD failure problem that the industry has been struggling with for decades. It is therefore imperative to explore revolutionary new on-chip CDM ESD protection techniques. This paper reports the first internally distributed CDM ESD protection concept, which is demonstrated in an oscillator IC designed and fabricated in a 45nm SOI CMOS process.

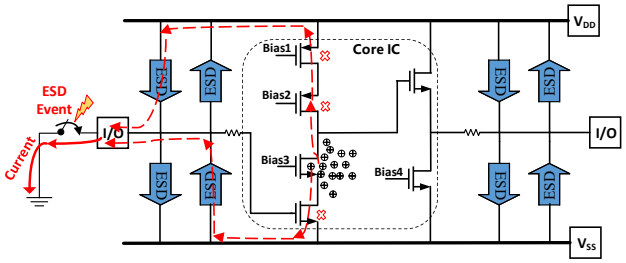

Fig. 1 Illustration of pad-based CDM ESD proteciotn scheme where internally stored charges may cause internal CDM ESD failures (marked x) when flowing from internal to external to discharge through an ESD device at the pad.

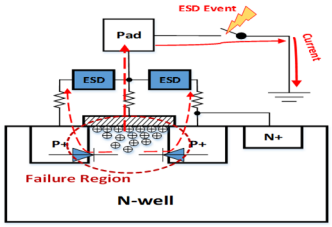

Fig. 2 An examplary case shows possible CDM ESD failure using a pad-based CDM ESD protection design.

II. Internally Distributed CDM ESD Protection

Understanding the fact that charges can be introduced to an IC anytime and are stored inside the IC randomly and

in a distributed manner, we devised a new non-pad-based internally distributed CDM ESD protection technique [7]. As depicted conceptually in Fig. 3, an IC die can be smartly partitioned, according to circuit functions, layout floor plan and device properties and sizes, to reflect the nature of internal charge distribution, and a net of smaller ESD devices will be designed and embedded inside the IC die at selected internal nodes per the smart portioning according to the internal/local CDM charge distribution. Therefore, as static charges are generated and accumulated internally and locally, and when reaching to a given local potential threshold, the internal/local ESD device will be triggered and the static charges will be discharged locally without flowing through the die to a pad for ESD discharging. Therefore, the new internally distributed ESD protection mesh can provide adequate whole-chip CDM ESD protection, smartly handling the "from-internal-to-external" CDM ESD discharge events without relying on any pad-based ESD protection structure.

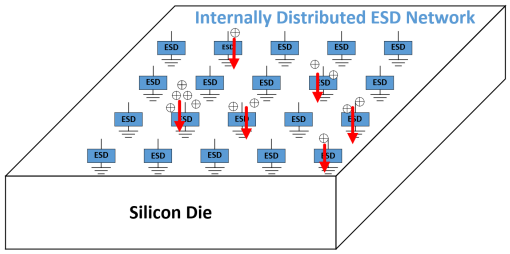

Fig. 3 Illustration of a new internally distributed CDM ESD protection method for ICs [7].

The new internally distributed CDM ESD protection technique was first verified by chip level simulation using a CDM-protected oscillator IC designed in foundry 45nm SOI technology. Fig. 4 shows the schematic for the 3-stage oscillator IC where six large MOSFET devices (NM1, NM2, NM3, PM7, PM8 and PM9) are considered

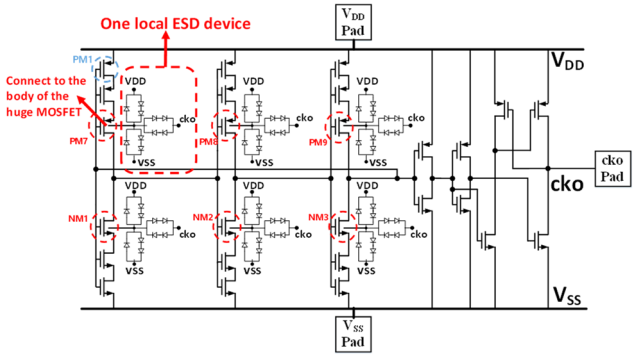

Fig. 4 A 3-stage oscillator IC designed in 45nm SOI where the large MOSFETs (NM1, NM2, NM3, PM7, PM8 & PM9) likely store the static charges internally. An internally distributed CDM ESD network is designed and connected to these large MOSFETs locally.

the main storage bins for the static charges internally. Per the smart partitioning rule, internal/local ESD protection structures will be placed at the circuit nodes associated with these large MOSFETs, which are anti-parallel ESD diodes comprising the internally distributed CDM ESD protection network. For comparison, Fig. 5 shows the traditional pad-based CDM ESD protection for the same oscillator IC using same ESD diodes. The CDM ESD design target is 500V CDM (failure current I_{t2}~10A), which requires the ESD diode being 360μm wide for the pad-based ESD design. For the new internally distributed CDM ESD protection design, the internal ESD diode features a smaller size of 60μm in width since the total charges are distributed among the six storage bins for CDM ESD events.

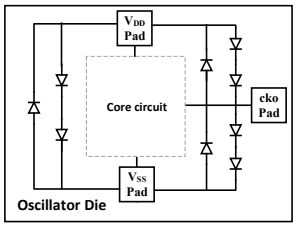

Fig. 5 Classic pad-based CDM ESD protection for the same oscillator IC as a comparison with that in Fig. 4.

SPICE circuit simulation was conducted for the two CDM ESD protected oscillator IC splits using a new pseudo-distributed field-induction CDM (FICDM) circuit model and simulation that we developed recently [6]. For both IC splits, i.e., using the traditional pad-based CDM ESD protection and the new internally distributed CDM ESD protection, the IC dies are charged by field induction and then discharges into the ground through the CDM ESD protection devices. The CDM ESD failure criterion used

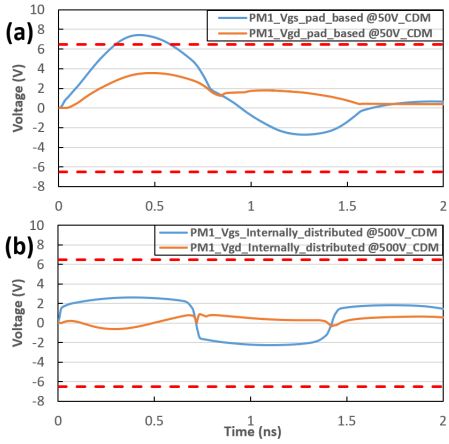

Fig. 6 Exemplary transient voltage analysis for V_{GS} and V_{GD} of PM1 of the IC under CDM ESD zapping: (a) CDM ESD failure occurs at 50V CDM zapping for the IC using classic pad-based CDM ESD protection, and (b) CDM ESD passed 500V CDM zapping for the IC using the internally distributed CDM ESD proteciotn method.

is the gate voltage breakdown ($|V_{GS}|$ or $|V_{GD}|$) of any MOSFET, which is BV_{OX}~6.5V in the 45nm SOI process. Fig. 6 presents the transient CDM discharging voltage waveforms by SPICE for an exemplar MOSFET PM1 for the two IC splits, which shows that CDM ESD failure occurs at ~50V for IC using classic pad-based CDM ESD protection, while the IC using the new internally distributed CDM ESD protection method passed 500V CDM zapping without any gate breakdown failure. This chip-level CDM ESD circuit simulation proves that the new internally distributed CDM ESD protection method is effective.

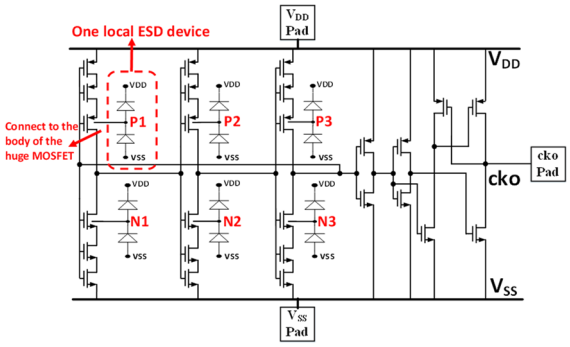

Fig. 7 Schematic for an oscillator demo IC using internally distributted CDM ESD protection.

III. Experiment Demo

A simplified oscillator IC, as depicted in Fig. 7, was designed and fabricated in a foundry 45nm SOI CMOS using the new internally distributed CDM ESD protection as a demo example. The internally distributed CDM ESD protection net consists of simple ESD diodes that are placed at the internal circuit nodes associated with the six large MOSFETs (P_1, P_2, P_3, N_1, N_2 and N_3). The small ESD didoes were designed (60μm in width) to handle CDM ESD current I_{t2}~2A. Fig. 8 shows the die photo for the CDM ESD protection IC fabricated and the measured output waveform of the IC confirming the oscillation function. Due to lack of commercial CDM ESD zapping tester in our lab, we chose to conduct VFTLP test for the fabricated IC dies. During VFTLP testing, the GS probe was applied directly to the internal circuit nodes where the

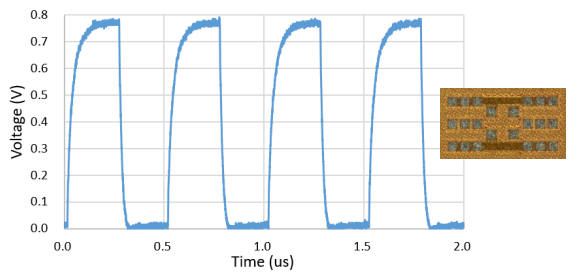

Fig. 8 Measured output waveform of the oscillator IC fabricated in 45nm SOI. Inset is a die photo.

internally distributed CDM ESD protection diodes are connected. Therefore, VFTLP testing can effectively and adequately characterize if the internal CDM ESD devices can respond to the ultrafast CDM pulse and protect CDM ESD protection internally and locally as expected. Fig. 9 presents exemplar CDM ESD discharge I-V curves at various internal circuit nodes stressed by VFTLP pulse routines, which clearly shows that the internal CDM ESD didoes can provide CDM ESD discharging in VFTLP test,

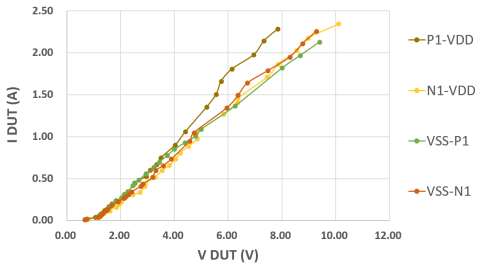

Fig. 9 Measured ESD discharge I-V curves for the IC with internally distributed CDM ESD protection by applying VFTLP pulses at internal nodes.

at least to the CDM level of I_{t2}~2A. The demo circuit, while simple, readily validated that the new internally distributed CDM ESD protection method works in Si, which will be further improved in our on-going designs.

IV. Conclusion

This paper reports the first novel internally distributed CDM ESD protection technique, which can replace the faulty pad-based CDM ESD protection method. Validated by using a simple 3-stage oscillator IC designed and fabricated in a foundry 45nm SOI CMOS, the new internally distributed CDM ESD method can provide true CDM ESD protection for advanced ICs, resolving the major CDM ESD protection problem of decades.

References

[1] A. Wang, *On-chip ESD protection for integrated circuits*, Kluwer, Boston, 2002, ISBN: 0-7923-7647-1.

[2] A. Wang, et al, "A review on RF ESD protection design", *IEEE TED,* pp. 1304-1311, July 2005.

[3] H. Feng, et al, "A mixed-mode ESD protection circuit simulation-design methodology", *IEEE JSSC*, pp. 995-1006, June 2003.

[4] C. Shaalini, et al, "Failure analysis on 14 nm FinFET devices with ESD CDM failure", *Microelectronics Reliability* 88 (2018): 321-333.

[5] H. Wang, et al, "Chip-level CDM circuit modeling and simulation for ESD protection design in 28nm CMOS", *Proc. IEEE ICSICT*, 2018.

[6] M. Di, et al, "Pad-based CDM ESD protection methods are faulty", *IEEE J-EDS,* October 2020.

[7] A. Wang, "Internally distributed CDM ESD protection", *U.S. Patent App. #62936355*, 2019.