ESD Protection Designs: Topical Overview and Perspective

Zijin Pan, Cheng Li, Weiquan Hao, Xunyu Li and Albert Wang, Fellow, IEEE

***Abstract*—Electrostatic discharge (ESD) protection remains a major challenge to integrated circuits (ICs), particularly for complex chips implemented at advanced technology nodes. Over decades, substantial advances have been made to on-chip ESD protection. This paper, instead of reviewing various specific ESD protection structures reported, provides an overview of selected key topics on practical ESD protection designs, focusing on new ESD protection concepts and design methodologies, as well as an outlook to future ESD protection designs.**

***Index Terms*—ESD, TLP, co-design, CDM, gNEMS, overhead.**

I. Introduction

On-chip ESD protection became an IC design reliability concern not long after the birth of Si CMOS IC technology in 1963. Over the past six decades or so, significant efforts have been devoted to understanding ESD failures and developing ESD protection solutions, leading to continuous advances in on-chip ESD protection designs. Many books provide comprehensive discussions on various ESD protection topics, from ESD fundamentals [1, 2] to advanced design topics [3, 4]. Over years, numerous specific ESD protection solutions have been reported covering various IC technologies at different nodes, for example, diode-string [5], diode-triggered SCR structure (DTSCR) [6], multi-directional SCR ESD protection structures [7, 8], ESD in SOI [9], ESD in FinFET [10], ESD for GaAs HBT [11], ESD in carbon nanotubes [12], ESD in Si nanowire FETs [13], ESD for GaN HEMT [14], and ESD for SiC MESFET [15], to name a few. While ESD protection may vary in performance and design practices, the following ESD protection design principles have been widely accepted: First, an ESD protection structure functions like an accurately-controlled rugged switch as depicted in Fig. 1 [4]. Second, ESD protection design is IC-specific, i.e., no universal one-for-all ESD protection solution. Third, the ESD-Critical Parameters must be carefully designed, as depicted in Fig. 2, in terms of the ESD discharging I-V characteristics featured by triggering (voltage V_{t1}, current I_{t1}, response time t_1), holding (voltage V_h, current I_h), discharging resistance (R_{ON}), and thermal breakdown (voltage V_{t2}, current I_{t2}), etc. [16, 17]. For example, the holding current and voltage of SCR ESD devices are important parameters related to possible latch-up. Fourth, ESD discharging I-V curve of any ESD device must be confined within an ESD Design Window, which unfortunately suffers from the ESD Design Window Shrinking effect as IC technologies advance [18, 19]. Fifth, on-chip ESD protection is a full-chip circuit design task, not about individual ESD protection device only. Sixth, the ESD Design Overhead effect, including inevitable ESD-induced parasitic capacitance (C_{ESD}), leakage (I_{leak}), noises and noise coupling, as well as ESD device sizes and ESD layout difficulty [20, 21], can not only seriously affect chip performance, but also make IC physical design extremely involving. To this end, much efforts have been given to understanding the negative impacts of ESD parasitic effects on high-data-date, high-frequency and broadband ICs. Therefore, careful ESD design optimization is always required to minimize any ESD-induced parasitic effects. Accurate ESD characterization hence becomes essential for high-speed and RF ICs, including S-parameter, C_{ESD} and noise figure (NF) measurements, as well as overall evaluation using certain ESD design Figure-of-Merit (FoM, a.k.a., F-factor) [22]. This paper is not intent to review all state-of-the-art specific ESD structures reported; instead, it provides a topical overview of critical new ESD protection concepts and design methodologies. The paper is organized as follows: After a brief on ESD protection basics in the Introduction, Section II discusses ESD-RFIC co-design method, Section III covers CAD techniques for ESD protection designs, Section IV presents some non-traditional ESD protection concepts, Section V describes new charged device model (CDM) ESD protection design method, Section VI depicts a few disruptive ESD protection concepts, Section VII gives a brief future ESD protection perspective, and a summary concludes the paper.

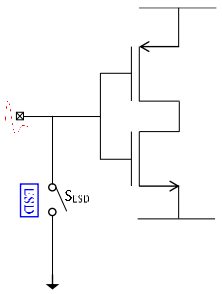


Fig. 1 Ideally, ESD protection acts as a controlled switch.

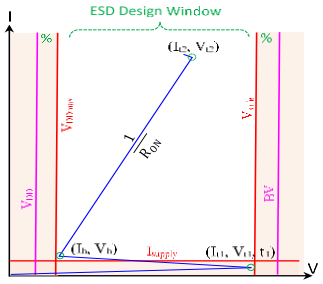


Fig. 2 ESD discharging I-V curve must fit into the ESD Design Window, with a margin.

II. ESD-RFIC co-Design

Nowadays, a major challenge is to design adequate ESD protection for high-speed, high-frequency ICs, which can be benefited from an ESD-IC (often, referred to as ESD-RFIC) co-design method. As said, ESD-induced parasitic effects, being C_{ESD} or noises, are inevitable and increasingly unacceptable to high-throughput, high-frequency and broadband ICs [20, 23].

Li (cli043@ucr.edu), Chen, F. Zhang, H Wang, Di, Pan and A. Wang (aw@ece.ucr.edu) are with University of California, Riverside, USA.

While efforts have been made to minimize unwanted ESD parasitic effects, for some chips implemented in certain IC technologies, ESD protection cannot be used at the ultrahigh-speed pads because the ESD structure will seriously degrade IC performance, e.g., an I/O circuit of >20Gbps cannot afford an ESD device with C_{ESD} ~ a few 10s fF [24]. Therefore, an ESD-RFIC co-design technique, suitable for any high-speed IC too, was developed to address such a design challenge [20]. Alternatively, a disruptive above-IC ESD protection concept was proposed that will be discussed in Section VI. The ESD-RFIC co-design method is practical, and conceptually simple: since the ESD parasitic effects are unavoidable, then, they ought to be included in core IC design to strike a design balance. ESD-RFIC co-design follows three steps as depicted in Fig. 3: First, one needs to select suitable ESD protection structures that must be optimized by CAD simulation to minimize the C_{ESD} and noises. Second, the optimized ESD structures will be fabricated and then characterized, i.e., measuring S-parameter and NF. Third, co-design can be conducted in two sub-steps. As usual, an RF IC is first designed with proper I/O impedance matching (Z-matching). Next, the measured ESD parasitic parameters are included in RF IC simulation, which for sure will cause IC Specs degradation. Careful tuning of I/O Z-matching will then be performed to recover the ESD-induced circuit degradation. To avoid the tediousness and inaccuracy of extracting C_{ESD}, the measured S-parameter file can be directly inserted into a simulator. The following two examples validated the ESD-RFIC co-design technique. Fig. 4 shows a low noise amplifier (LNA) fabricated in a 180nm RF CMOS featuring 5GHz center frequency and power dissipation of 11.5mW. The LNA has an input Z-matching tank of C1, L1, L3, L4 and L5, and has 5KV human body model (HBM) ESD protection at input [25]. There are four design splits: LNA without ESD, LNA with ggNMOS ESD (serious impact), LNA with diode ESD (optimized), and LNA with diode ESD and co-design (recovery). The measurement results show that LNA gain S21 (b), input reflection S11 (c) and NF (d) are all seriously affected by traditional ggNMOS ESD protection device (beyond repairable). These LNA Specs are also affected by the optimized diode ESD device, which was then recovered by ESD-LNA co-design. Fig. 5 depicts a series-shunt SP10T RF antenna switch designed for a 4G global phone and fabricated in 180nm SOI CMOS [26]. The SP10T switch supports quad-band GSM and multi-band WCDMA (a). Since GSM transmitter has to handle output power up to 35dBm, i.e., 30.5V, multiple FETs (6, 8, 12) must be stacked in the series and shunt branches. Unfortunately, the uneven voltage drop (V_{ds}) across each FET in a stack will cause circuit degradation, which can be alleviated by a feed-forward capacitor (FFC) technique, e.g., Cf1 and Cf2 in (b). This SP10T features 9KV ESD protection using anti-parallel diode ESD protection, which

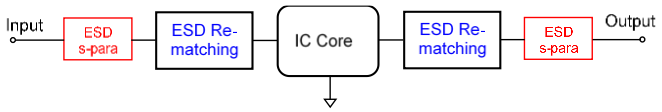


Fig. 3 Illustration of ESD-RFIC co-design method.

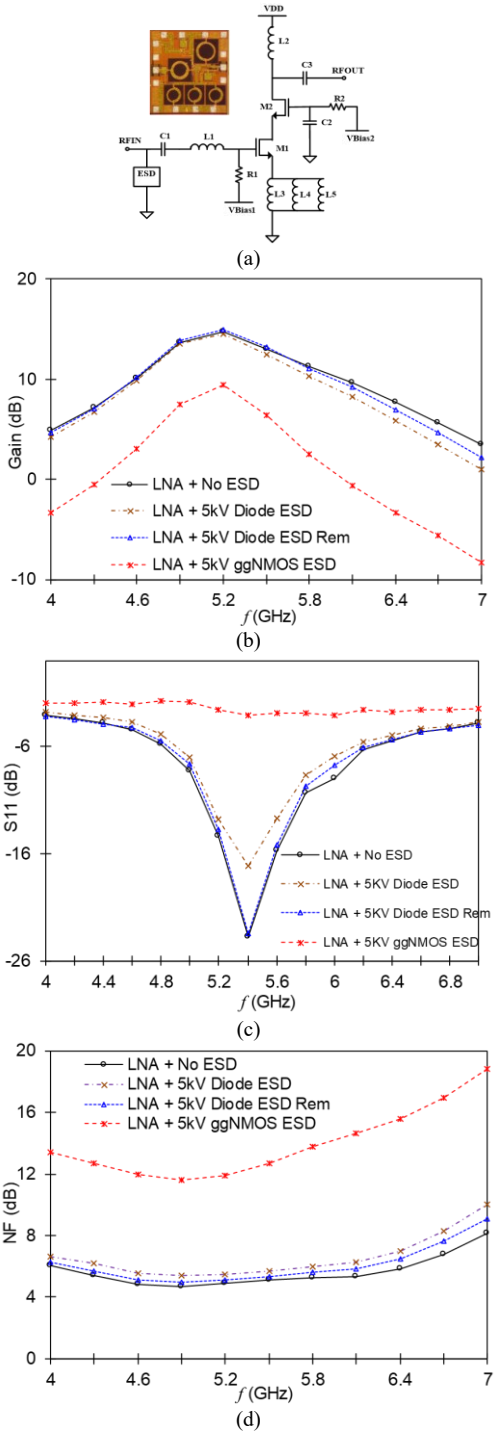


Fig. 4 Impact of ESD protection on LNA Specs measured: (a) schematic and die photo, (b) gain S21, (c) input reflection S11, and (d) NF.
Rem = Z-rematching by ESD co-design.

was optimized for minimum C_{ESD} that however still affected SP10T circuit performance. Measurement of V_{ds} (c) shows that the uneven V_{ds} across an 8-FET stack was smoothed by FFC for SP10T without ESD protection. However, it was observed that the ESD protection corrupted the FFC remedy, which fortunately was fully recovered after ESD-SP10T co-design. Transmission line pulse (TLP) testing for insertion loss (IL) in (d) confirms 9KV ESD protection for the SP10T IC. The two design examples clearly show that even optimized ESD

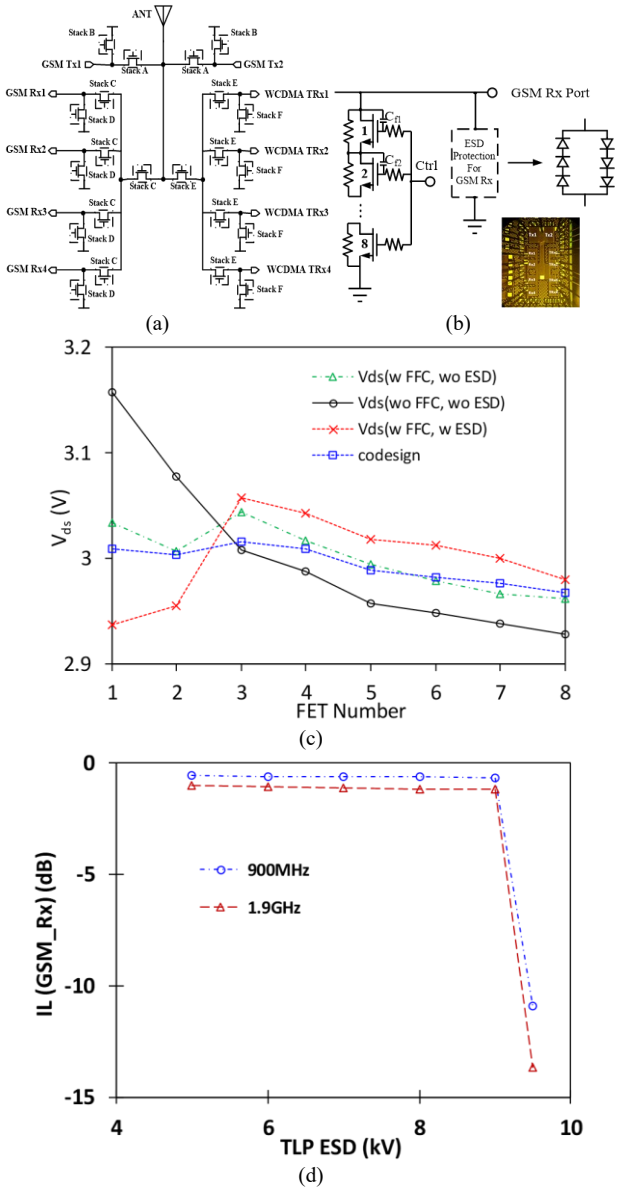


Fig. 5 SP10T + 9KV ESD protection by ESD co-design: (a) switch topology, (b) an 8-FET stack with anti-parallel diode ESD protection and die photo, (c) measured V_{ds} for each FET in one FET stack, and (d) measured IL confirms 9KV HBM ESD protection.

protection can seriously affect RF IC performance, which can be recovered by careful ESD-RFIC co-design.

III. CAD for ESD Protection Design

In fact, CAD methods are essential to ESD-IC co-design, and practically, for all on-chip ESD protection requiring design optimization, predication and verification. This section discusses CAD simulation techniques and procedures for practical ESD protection designs.

A. TCAD for ESD Protection Designs

Simulation is essential to IC designs. Since on-chip ESD protection design is a part of circuit design, it is natural for IC designers to run circuit-level ESD design simulation. Circuit-level ESD simulation has been studied for long [27]. Yet, lack of adequate compact modeling for ESD protection structures remains a major barrier for full-chip ESD protection simulation using circuit simulators, e.g., SPICE. This is because ESD discharge involves complex multiple-coupling effects (materials, process, device, circuit, layout, 3D, electro-thermal, transient), which could not be accurately described in normal SPICE device models yet, e.g., ESD-induced hot spots and thermal boundary conditions (internal, 3D, transient, roaming), 3D ESD discharging routing (layout effect), etc. Accordingly, TCAD-based 3D mixed-mode ESD simulation design method has been developed to address the ESD complexity without being hindered by unavailability and inaccuracy of ESD device

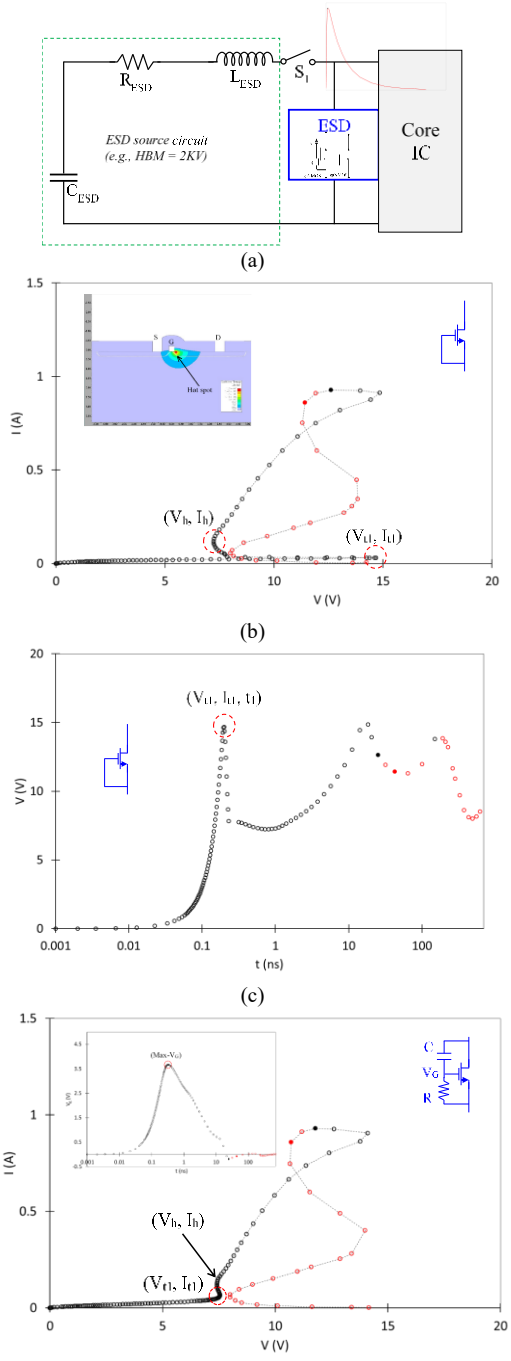


Fig. 6 Design comparison of ggNMOS and gcNMOS ESD structures by TCAD: (a) simulation schematics, (b) ggNMOS ESD discharging I-V curve (Inset: hot spot), (c) ggNMOS ESD discharging in t-domain, and (d) gcNMOS ESD discharging I-V characteristics (Inset: V_G behavior).

compact modeling [17, 28, 29]. In principle, TCAD covers both device and circuit simulation in a 3D fashion where ESD discharging is simulated by solving device physics equations across the device mesh structure with the ESD device terminal characteristics being internally auto-coupled to the core circuit for circuit-level simulation (SPICE) using normal compact device models for regular circuit components. This way, TCAD simulation can reveal the ESD discharging details (i.e., ESD-critical parameters: V_{t1}, I_{t1}, t_1, V_h, I_h, R_{ON}, V_{t2}, I_{t2}, etc.) in the context of the IC circuit, hence facilitates ESD design optimization and prediction at chip level, hence avoiding trial-and-error. As an example, Fig. 6 depicts a TCAD simulation study of ggNMOS *versus* gcNMOS ESD protection structures [30]. TCAD ESD simulation allows to use any standard ESD pulse generator circuitry to produce a certified ESD waveform (per industrial ESD test models) to stress an IC, as shown in (a). The simulated ESD discharge I-V curves (b & c) for ggNMOS reveal the ESD-critical parameters including the critical t-domain behavior (c). It found that the triggering voltage (V_{t1} ~ 14.7V) is high for ggNMOS, not suitable for low-voltage ICs. A gcNMOS ESD structure was proposed using RC-to-gate coupling to reduce ESD triggering to V_{t1} ~ 7.5, as shown in (d). TCAD ESD simulation can provide rich design details. For example, Inset in (d) shows the transient gate voltage in gcNMOS, helping to avoid direct gate breakdown due to gate-coupling by properly selecting R&C values. Inset in (b) reveals the ESD-induced transient hot spot related to ESD thermal failure. Such details in TCAD ESD simulation supports ESD-technology co-development that is an emerging topic in advanced IC technology development. To address the 3D layout effects on ESD protection designs, 3D TCAD simulation is needed [28, 31]. Fig. 7 presents a design example of using 3D TCAD to investigate 3D (layout) ESD discharging behaviors for P^+NW ESD diodes in CMOS where the four design splits share the same in-Si diode structure, but featuring different

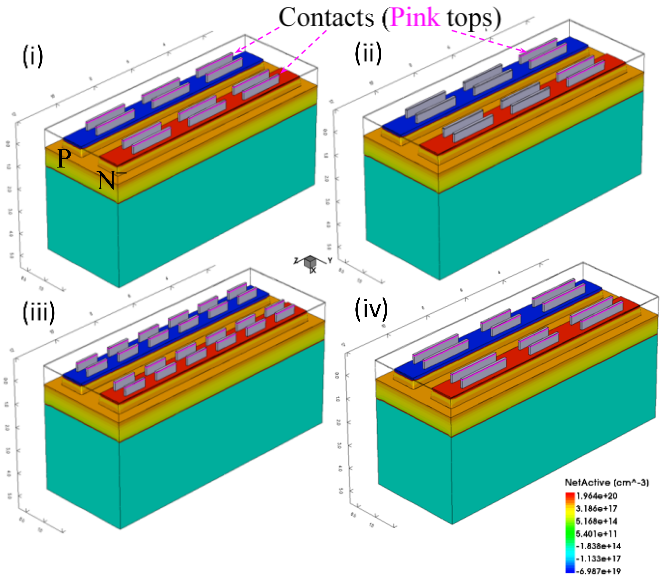


Fig. 7 Comparison study of layout design on P^+NW ESD diodes by 3D TCAD ESD simulation with four splits with same Si structure, but different metal/contact layout to reflect the variation in ESD discharging paths. Pink line on top of metal (Gray) indicates valid ESD conduction and the contacts were designed differently to reflect 3D ESD discharging crowding effect.

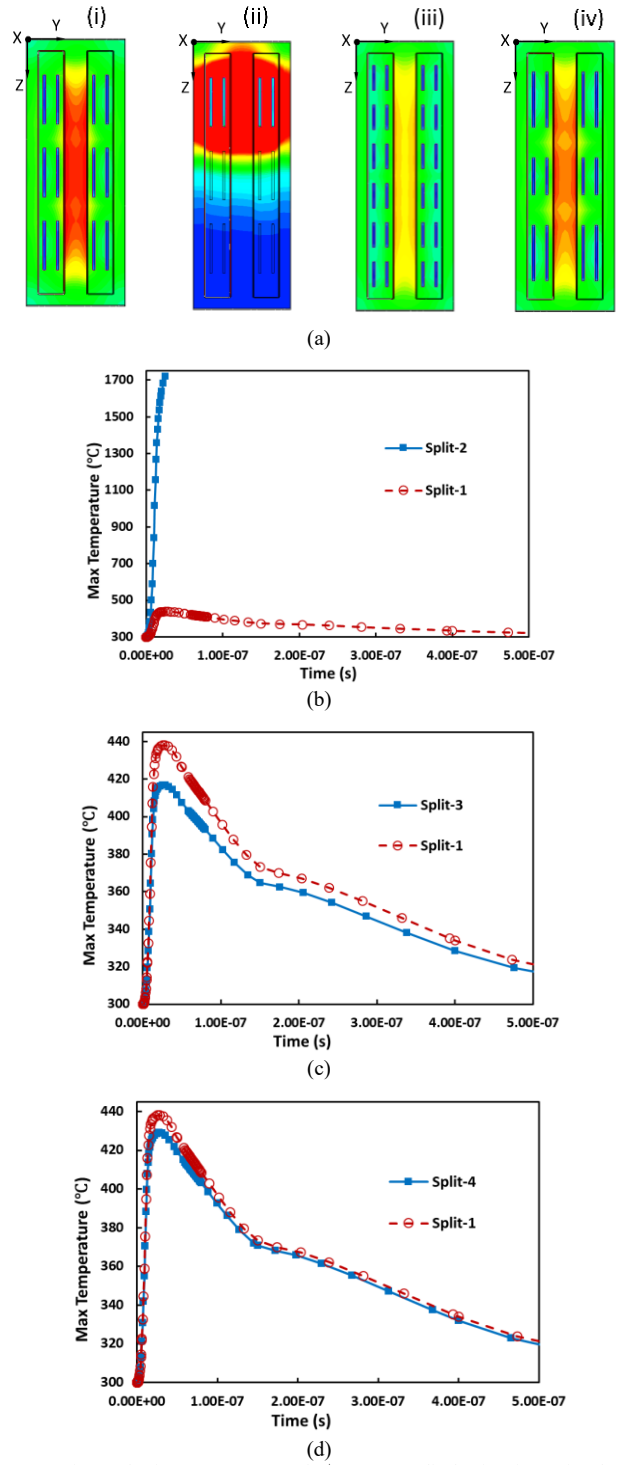


Fig. 8 Maximum lattice temperature of P^+NW ESD diodes in Fig. 6 simulated by 3D TCAD transient ESD simulation reveals 3D impacts of four layout designs on ESD discharging conduction routes and heating: (a) T_{max} maps for 4 layout splits, and (b), (c) and (d) T_{max} comparison of splits (ii, iii and iv) with the base line layout (i).

metal/contact layout designs in the backend used, which were used to study the 3D layout-related ESD conduction routing that can result in local current crowding and hot spots [31]. Fig. 8 shows the simulated ESD-induced maximum lattice temperature (T_{max}) across the ESD diodes, including T_{max}-map and split comparison, which clearly reveal the layout effect on 3D ESD discharging. It is noteworthy that, due to computing

power, it is wise to limit "full-chip" ESD simulation to I/O circuit block with ESD devices in TCAD ESD simulation. It is also important to know that calibration is vitally critical to TCAD mixed-mode ESD simulation and that it is wise to focus on the "trend" revealed in TCAD simulation in ESD designs. Further, readers are reminded that, while TCAD can be very useful to simulating ESD discharge functions, accurate TCAD ESD simulation can be very involving that requires designers to thoroughly understand device physics and numerical simulation algorithms in order to properly selecting the embedded device physics models and simulation boundary conditions. In addition, all ESD-critical parameters can be studied in details by 3D TCAD ESD simulation, which however is still very time/computing consuming.

B. ECAD for ESD Protection Designs

It is well known that TCAD is not popular among circuit designers due to device physics and process details involved, as well as computing limitation, making TCAD unsuitable for simulating large chips. Since ESD protection is for ICs, it is obviously desirable of being able to run full-chip ESD circuit simulation using ECAD tools (e.g., SPICE). Though accurate ESD device compact modeling is still a technical barrier as discussed earlier, ESD circuit simulation using SPICE is possible if behavioral models are available for ESD devices. Circuit-level ESD simulation by ECAD has three steps: First, carefully designed ESD protection structures are fabricated and measured for their ESD discharging I-V characteristics, providing all ESD-critical parameters. Second, behavioral models are developed for the ESD devices measured, which are certainly 100%-ly accurate for the ESD structures fabricated, and an ESD device library (Pcell) is then built up accordingly. Third, in circuit design, an IC designer can select a suitable ESD device from the ESD library to construct a complete ESD-protected IC core circuit, which can then be simulated for its full-chip ESD discharging behaviors (i.e., ESD functions) using SPICE and the behavioral model. Fig. 9 presents one exemplar IC designed and fabricated in a foundry 28nm CMOS. The IC core is a simple buffer circuit with full-chip 2KV ESD protection (a) including an active power clamp, PU-ESD (Input to V_{DD}) STI P^+NW ESD diode and PD-ESD (Input to V_{SS}) N^+PW, with its die photo shown in (b) [32]. TLP testing shows the ESD-critical parameters for PU-ESD (forward I_{t2} ~ 2.3A, reverse V_{t1} ~ -7.98V), PD-ESD (I_{t2} ~ 1.8A) and power clamp. The 28nm CMOS features V_{DD} = 0.9V, BV_{GS} ~ 8.52V and BV_{DS} ~ 7.01V, which establishes the ESD Design Window. In SPICE ESD simulation, it is critical to include the metal interconnects resistance since even a small bus resistance is significant under lager ESD transients. The TLP-measured bus resistance are R_1 ~ 1Ω, R_2 ~ 1Ω, R_3 ~ 1.15Ω, R_4 ~ 0.6Ω, R_{bus1} ~ 1.5Ω and R_{bus2} ~ 0.3Ω. A case of 2KV HBM ESD zapping to Input pad with respect to V_{DD} (ND mode) is simulated by SPICE to reveal the full-chip ESD discharging details. (c) shows the transient voltages at all circuit nodes, and (d) gives the branch discharging currents and terminal voltages of concerned internal transistors under 2KV ESD zapping, which can be analyzed to check ESD device triggering and ESD discharging paths. The designed ESD discharging path under ND mode B-to-A (negative) zapping is Route-ADEFGB through the power clamp and forward PD-ESD that is confirmed by checking the transient node voltage drops. However, simulation discovered that an unexpected side ESD discharging path of Route-ACD was also triggered ($V_{CB} > V_{t1}$ ~ 7.98V for PU-ESD), which fortunately only conducts a small current of ~40mA, but could be a weak point as shown in the thermal image (b). The terminal voltages for internal transistors (MP1 and MN1) are lower than the breakdown voltages (d). Overall, full-chip ESD circuit simulation using SPICE provides circuit-level ESD discharging details (i.e., ESD function), confirms chip-level ESD protection, reveals design weakness and suggests how to improve a design. In summary, ECAD allows full-chip ESD protection circuit simulation, but one can only use pre-tested ESD devices with behavioral models.

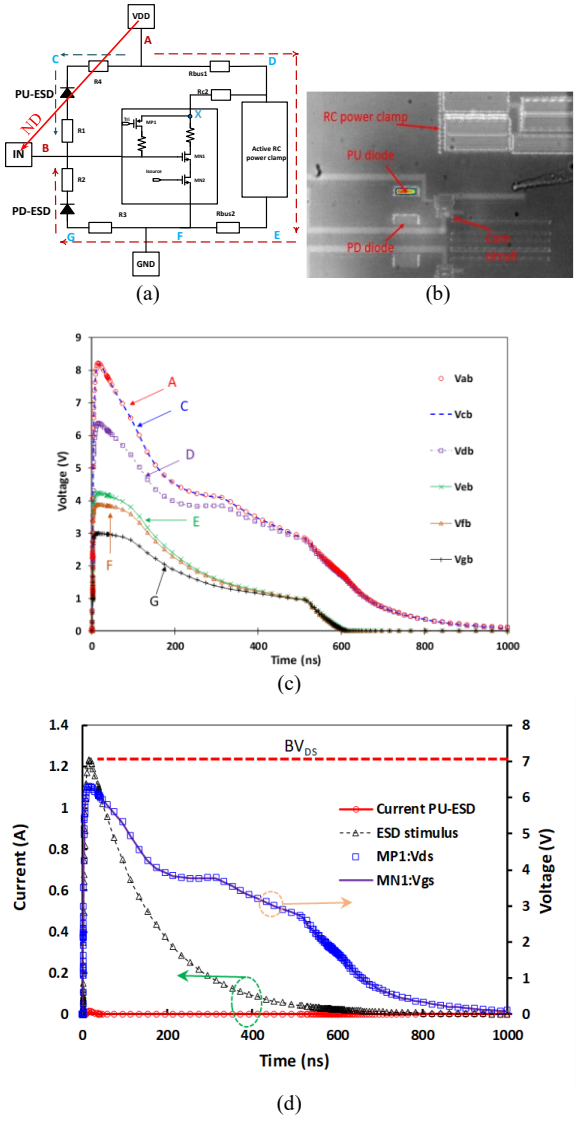


Fig. 9 SPICE simulation of full-chip ESD protection for a buffer+ESD chip under 2KV HBM ESD stressing: (a) circuit schematic, (b) EMMI image, (c) node voltages with respect to node-B under B (negative)-to-A (ND mode) ESD zapping, and (d) branch current and transistor terminal voltages.

C. CAD for ESD Protection Design Verification

Full-chip ESD protection circuit design verification must be conducted at physical layout level, just like in normal IC designs, which cannot be achieved using neither TCAD nor ECAD ESD simulation. Fig. 10a illustrates the common IC design flow, staring from setting circuit Specs and selecting circuit topology and schematics, then conducting pre-simulation, next building circuit layout, followed by performing layout design verification (i.e., DRC, LVS, ERC, xRC, etc.), and finally conducting post-simulation. If physical design verification is satisfactory, one can then sign-off the tapeout and send the GDSII data to a foundry for fabrication and expect to achieve 1st Si design success. Unfortunately, practical ESD protection circuit design still follows an incomplete design flow as depicted in Fig. 10b where the key physical design verification steps are mostly missing. This is unacceptable for ESD protection design for complex chips at advanced technology nodes. In fact, ESD layout design is vitally critical to any chip-level ESD protection designs due to unavoidable 3D and parasitic effects. In real-world IC design practices, one does not tapeout a design without confirming it working on a computer screen, though working on a screen may not guarantee functioning in Si. For full-chip ESD protection designs, simple DRC and LVS checking, often following relaxed ESD design rules, does not have much value to chip-level ESD physical design verification, because such an over-simplified "checking" method is not ESD-function-based and misses most parasitic ESD behaviors at chip level [4]. To address this challenge, a new ESD CAD technique was developed, which contains the following key functions: to extract all ESD devices designed (intentional) and ESD-like devices (parasitic) from the layout GDSII data file, to extract all ESD-critical parameters for any ESD-like devices extracted, to construct an intermediate full-chip ESD circuit netlist (all possible ESD-like devices included) and to create the final ESD circuit netlist ("functional" ESD devices) by removing any extracted ESD-like devices that may be redundant, to extract all possible ESD discharge paths between any two pads and to estimate the equivalent ESD-critical parameters for these ESD conduction paths, then to conduct full-chip ESD circuit simulation and zapping simulation to verify the ESD physical design [33, 34]. Extracting all possible parasitic ESD-like devices within an IC is critical since early ESD failure often occurs at such ESD weak points, even if individual ESD devices are designed well. Since ESD device layout is often irregular and involves interconnection, not simple Manhattan style, a subgraph isomorphism technique was proposed to extract any arbitrary ESD-like devices on a chip [33]. A Smart Parametric Checking method was developed to check all ESD functions, not just layout spacing (DRC) and circuit connection (LVS), at chip level in order to realize the desired full-chip ESD circuit physical design verification [35]. In a design example shown in Fig. 11a, all intentional ESD devices designed (LVSCR and diode at input 1 & 2, ggNMOS and ggPMOS at output, and SCR as a power clamp) and possible parasitic ESD-like devices (e.g., an SCR structure within the guard ring of the output buffer block) were extracted. Their ESD-critical parameters were also extracted. It is important to know that, the ESD-critical parameters for an ESD device must be extracted in both conduction polarities (i.e., between anode/A and cathode/K, Fig. 11b), in order to achieve accurate full-chip ESD physical design verification, because ESD stressing (and ESD testing routines) may occurs to any pads on a chip in any directions. Fig. 12 illustrates the extracted ESD-like devices flagged on the layout where it shows that two fingers are correctly identified for the ggPMOS ESD structure at the output pad. Fig. 13 depicts the new ESD CAD flow realized in a new ESD CAD tool developed using the new ESD CAD technique, which essentially follows the same IC CAD design flow [4]. The new ESD CAD tool (named SmartESD) has the following critical functions: take and analyze the ESD design GDSII data file, perform simple ESD checking (ESD-flavored DRC, LVS, xRC), extract all ESD-like devices (intentional and parasitic) and their ESD-critical parameters, extract all possible ESD discharge paths and their equivalent ESD-critical parameters, generate an ESD netlist (including metal bus resistance), and conduct ESD circuit simulation (post-simulation using ESD device behavior models) to verify the full-chip ESD protection physical design based on ESD discharge functions (not just

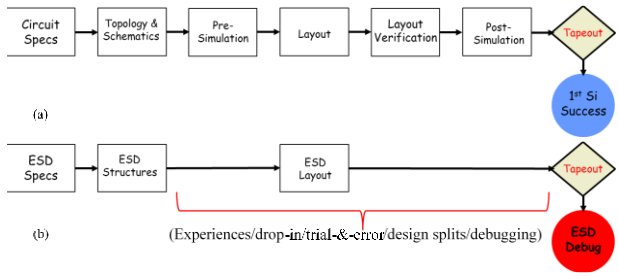


Fig. 10 Common flow comparison: IC core design *versus* ESD protection design (missing critical steps for 1st-Si design success).

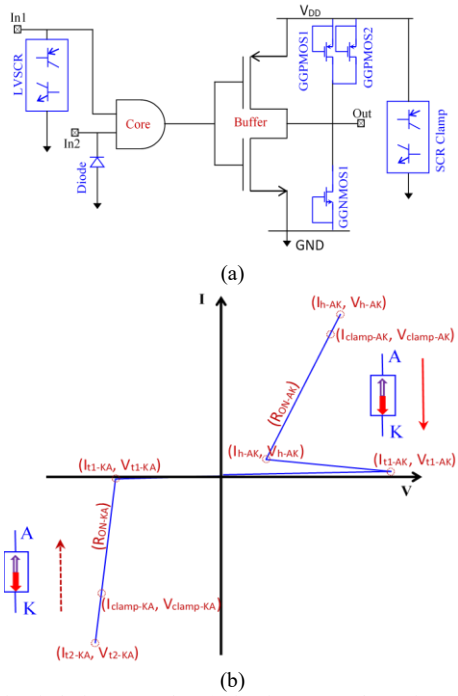


Fig. 11 ESD circuit design example: (a) circuit + ESD schematics, and (b) ESD-critical parameters must be extracted in both directions (i.e., A⇒K and K⇒A discharging).

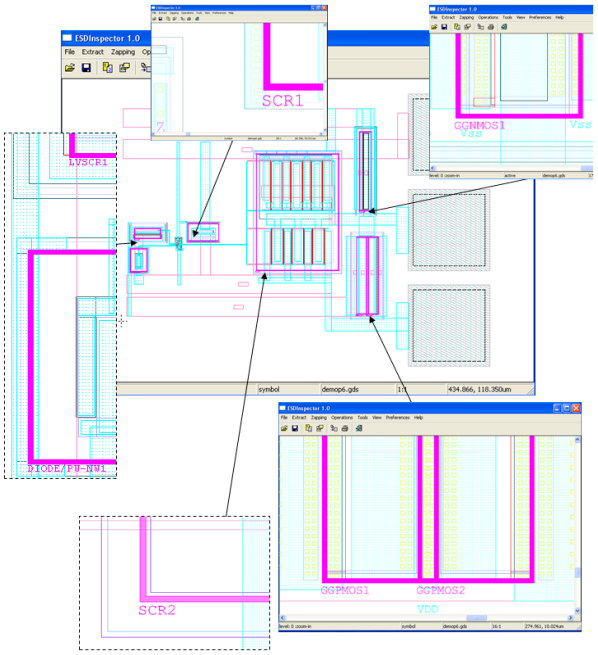


Fig. 12 CAD-extracted intentional ESD devices (designed for I/O and power clamp) and parasitic ESD-like devices (SCR2) for the ESD circuit in Fig. 11.

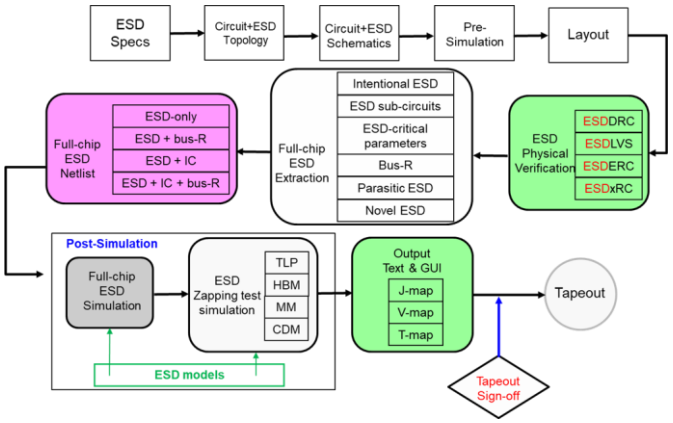
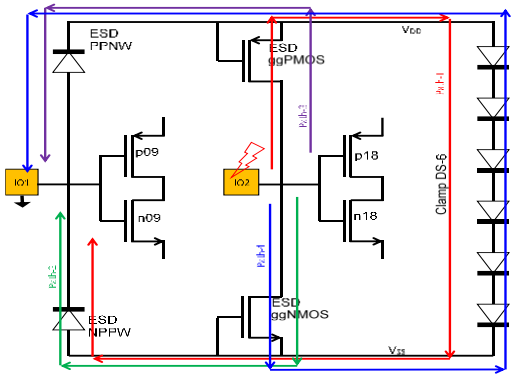
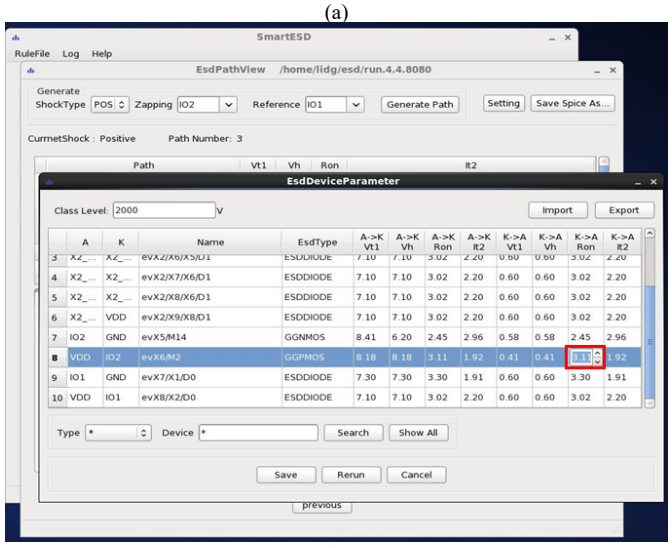


Fig. 13 SmartESD has all key features needed to conduct ESD-function-based full-chip ESD physical design verification. The graphical interface includes ESD discharge current density map (J-map), node voltage map (V-map) and temperature map (T-map for ESD-induced heating) for the whole chip.

layout spacing and connection). Uniquely, with the ESD circuit netlist extracted, SmartESD allows an IC designer to comprehensively simulate the extremely complex full-chip ESD zapping test routines (think about how many possible ESD zapping pad-pad combinations for a chip with hundreds of pads!) in the design phase, not waiting until the Si is out. Fig. 14 depicts one design example where SmartESD can extract all ESD-like devices, generate the ESD netlist, extract all possible ESD discharging paths (e.g., 4 paths under a specific positive IO2-to-IO1 ESD zapping case) and their equivalent ESD-critical parameters. Next, the "actual" ESD discharging path (Red) was identified based on its triggering voltage (i.e., lowest V_{t1}). It is worth noting that, when comparing V_{t1} values for the extracted ESD conduction paths, both ESD stressing polarities and metal bus resistance must be included for accuracy. The ESD circuit design validation is checked per different ESD failure/pass criteria, including ESD Design Window compliance, node breakdown voltage and branch current



(a)



(b)

Fig. 14 Example full-chip ESD layout design verification by SmartESD CAD: (a) ESD netlist extracted and four possible ESD discharge paths identified under IO2-to-IO1 positive ESD zapping, and (b) GUI table for extracted ESD-critical parameters (both AK and KA directions). It allows users to enter TLP-measured ESD-critical parameters for accuracy (Red box).

handling capability across the chip, and more. After the ESD-function-based full-chip ESD physical design verification done, one may then tapeout a design for foundry fabrication.

IV. Unique ESD Protection Concepts

Adequate ESD protection is required for all kinds of ICs. As said, ESD protection is IC-specific, which often requires non-traditional thinking in ESD designs to accommodate specially needs of different ICs and systems, which cannot be facilitated by traditional ESD protection designs. This section discusses a few unique ESD protection concepts made possible by ESD CAD simulation.

A. Field-Programmable ESD Protection

Good ESD protection requires careful design of the ESD-critical parameters, e.g., the triggering voltage, V_{t1}. Yet, in many cases, a post-Si adjustable V_{t1} may be needed for reasons: First, process variation may lead to a shift in V_{t1} that may be off the ESD Design Window. Second, for system vendors who use IC chips from chip design houses, it may be necessary to fine-tune the V_{t1} for chips from different IC suppliers for the same system product because the ESD-critical parameters for these chips from different IC suppliers are likely slightly different. Therefore, field-programmability of V_{t1} of ICs received can be

beneficial. A post-Si field-programmable ESD protection concept was reported to meet such needs [36]. Fig. 15 depicts a prototype V_{t1}-programmable NMOS ESD protection structure featuring a layer of nano crystal quantum dots (NC-QD) within the gate dielectric stack. By programming, these NC-QD dots can be charged and discharged to alter the threshold voltage, hence leading to a slight variation in V_{t1} (i.e., $\triangle V_{t1}$). In the prototype device, $CoSi_2$ coated quantum dots (~10nm in diameter) were placed above a thin oxide tunneling film of ~5nm. Transient TLP zapping test shows that up to $\triangle V_{t1} \sim 2V$ was achieved by gate programming, while the leakage remains very low at $I_{leak} \sim 15pA$, as shown in Fig. 15. Other device mechanisms may be used to fine-tune V_{t1} in field as well, e.g., using a SONOS FET structure [19]. Post-Si field-programmable ESD protection can be useful in system designs.

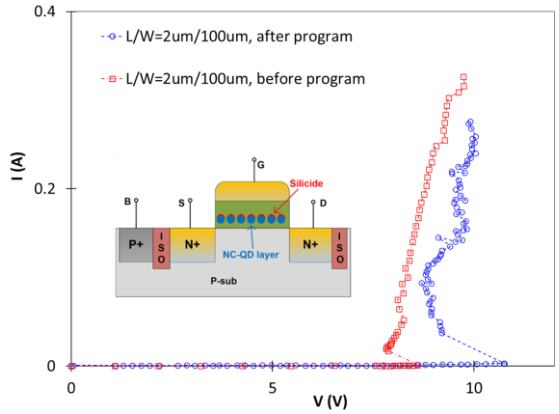


Fig. 15 An NC-QD NMOS ESD protection structure shows field-adjustable V_{t1} in TLP measurement. Inset: cross-section of the NC-QD device.

B. *Dispensable ESD Protection*

It is well known that ESD-induced parasitic capacitance can affect IC performance. Hence, ESD design optimization is needed to minimize C_{ESD} and ESD-RFIC-co-design is essential for designing high-speed, high-frequency ICs. Yet, for ICs with extremely high data rates, e.g., >100Gbps in optical backbone communications infrastructure, even a tiny C_{ESD} of a few fF is unacceptable. For such cases, even ESD-IC co-design cannot resolve the problem. To address such a challenge, a unique dispensable ESD protection concept was proposed with the following design principle: assume the ICs are used for enterprise infrastructure, hence ESD risk will be "rare" after system installment; therefore, adequate on-chip ESD protection is only required to protect ICs until the system is installed, at the time, the ESD protection structures on the chip will be physically removed from pads, as a result, the ICs in the system installed will return to its originally designed data rate since $C_{ESD} = 0$ realized after ESD removal [37]. Fig. 16 demonstrates a fuse-based dispensable ESD protection designed for a 22Gbps IO buffer circuit fabricated in a foundry 28nm CMOS. The ESD devices are connected to IO pads through specially designed fuses, which were notched metal wires or a metal-to-metal via as shown in Fig. 16b. In measurement, the ESD devices can be physically cut-off by burning the fuses. Fig. 16c shows that the measured data rate reduced substantially from 22Gbps (designed) to 12Gbps due to C_{ESD}. After ESD removal, the measured throughput was recovered to its originally designed 22Gbps. It is noteworthy that such a dispensable ESD

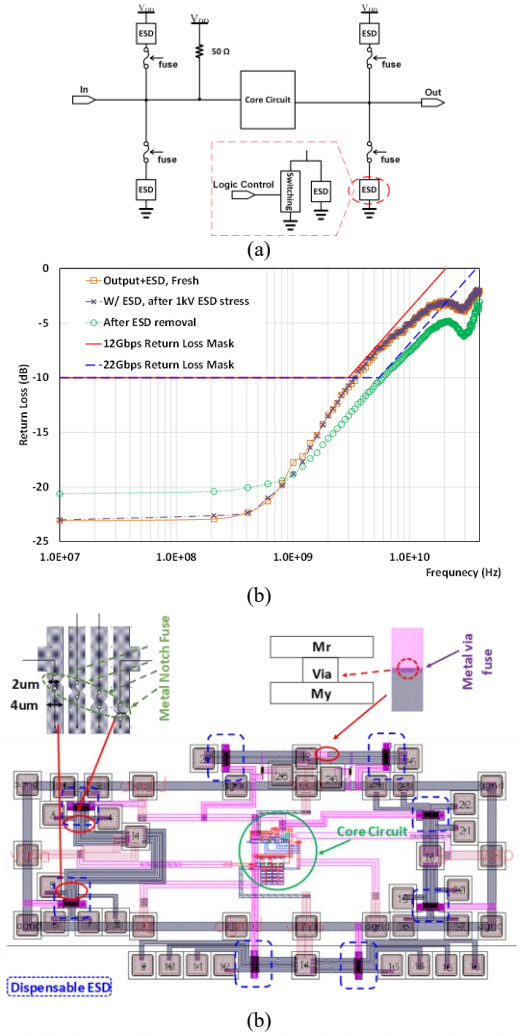


Fig. 16 A field-dispensable ESD protection design for 22Gbps I/O link: (a) circuit diagram, (b) layout, and (c) measured data rates before/after cutting-off the ESD protection device.

protection concept is only suitable for ultrahigh-data-rate enterprise systems that are not "touchable" by human users in operations; however, not useful to consumer electronics products (e.g., smartphones and tablets) that are touched by end users every second.

C. *In-TSV ESD Protection*

Existing ESD protection utilizes planar device structures placed side-by-side with pads on a chip, which makes layout design very difficult for large complex chips. In addition, planar ESD devices suffer from hot spots associated with the curvatured ESD discharging routes. To overcome this problem, an in-TSV diode ESD protection concept was developed [38]. In the design prototype shown in Fig. 17, all PN diode ESD devices are built vertically inside TSV holes in a Si substrate (a), which can be placed underneath pads. Compared to a curved ESD conduction path, e.g., in an STI ESD diode (b), the vertical in-TSV ESD diode feature vertical and uniform ESD discharging conduction (c). The prototype device is a poly-Si/Si PN junction formed inside a TSV hole that was validated by TLP testing (d). It is possible to build other ESD device structures inside a TSV hole.

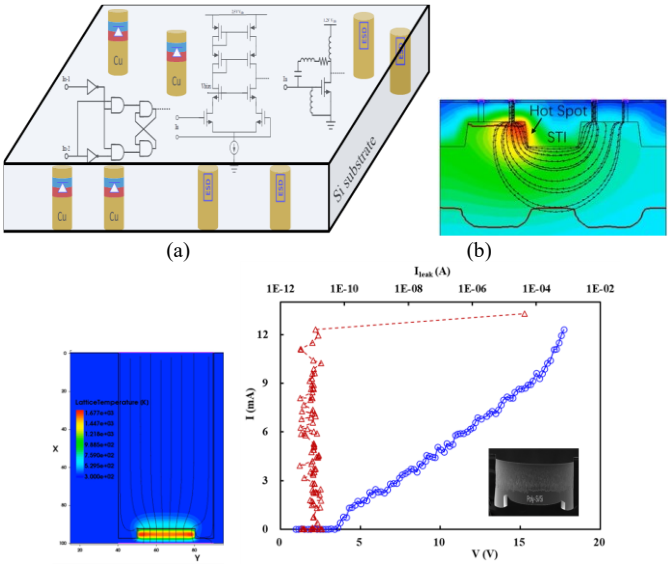


Fig. 17 A prototype in-TSV ESD diode illustration: (a) TSV ESD protection scheme, (b) traditional planar STI ESD diode showing hot spot due to current crowding, (c) in-TSV ESD diode featuring uniform vertical ESD conduction, and (d) TLP testing confirming in-TSV diode ESD discharging I-V curve, Inset shows poly-Si/Si PN junction in TSV by SEM.

D. *Interposer ESD Protection*

It is agreed that ESD protection can be very challenging for large complex chips because there are large number of ESD protection devices needed to form a complete on-chip ESD protection network. To attack this ESD design problem, a unique interposer-based ESD protection concept was developed [39]. The idea is illustrated in Fig. 18. An IC core designed without ESD protection is in one Si wafer (a) and the ESD protection network is designed and placed in a separate interposer wafer used for complex metal interconnects (b). Then, flip-chip bonding will stack the two dies together to form a stacked ESD-protected "chip". A protype design was done using a SP4T RF switch IC as the core die and diode-based ESD protection in a Si interposer die. The design was implemented in a foundry 45nm SOI CMOS (d).

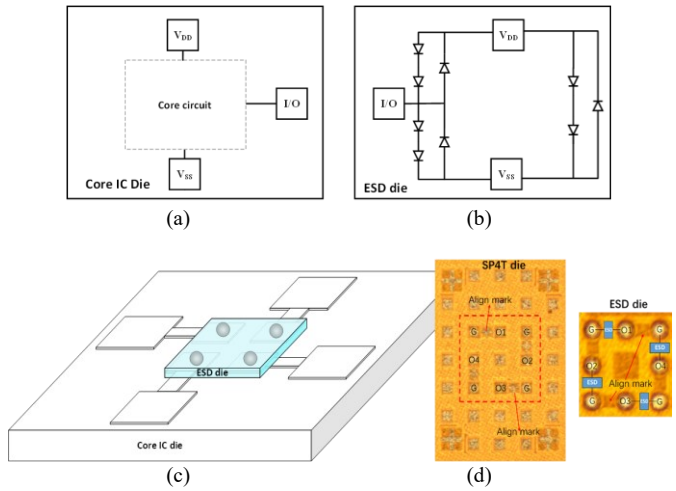


Fig. 18 Interposer-based ESD protection: (a) core IC die, (b) interposer ESD die with exemplar diode ESD protection network, (c) flip-chip bonding of core and ESD dies, and (d) prototype of SP4T die and ESD die in a foundry 45nm SOI CMOS.

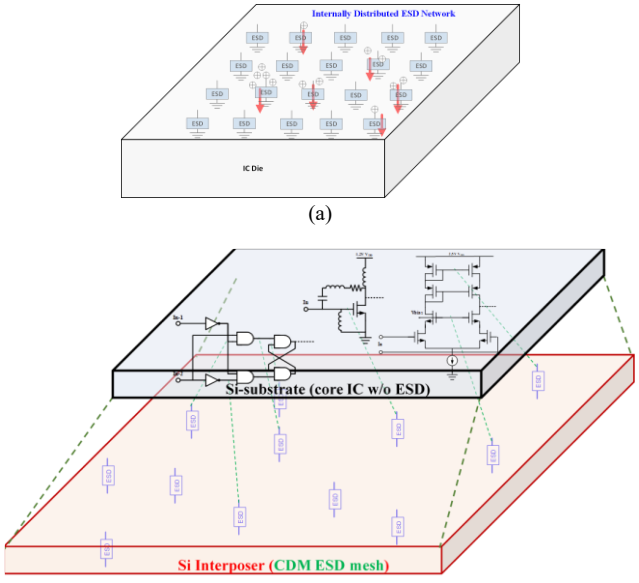
V. New CDM ESD Protection

A. *Misconception in CDM ESD Protection*

These days, CDM ESD protection is an emerging design challenge, particularly for large complex ICs made at advanced technology nodes. It is well known that CDM ESD protection seems to be mysterious and even CDM zapping test (including very fast TLP, i.e., VFTLP) results can be rather random. It is recently reported that the exiting pad-based CDM ESD protection method may be fundamentally wrong, contributing to the CDM ESD design uncertainty [40]. In theory, HBM, as well as machine model (MM) and International Electrotechnical Commission (IEC), ESD phenomenon is a from-External-to-Internal event where static charges stored inside a human body are discharged into an IC (DUT) when touching the chip; hence, the ESD device at a pad serves as a door keeper to prevent these external charges from getting into the IC core by discharging the charges into the ground (GND) at the pad. Therefore, the classic pad-based ESD protection method works for HBM, MM and IEC ESD events. However, CDM ESD phenomenon is entirely different, which is a from-Internal-to-External event in nature where charges stored inside an IC will discharge into GND when a pad is grounded. So far, CDM ESD protection still utilizes the pad-based ESD protection method and designers are mostly focusing on making an CDM ESD device faster to ensure CDM ESD triggering. Unfortunately, while the internal charges may be discharged into GND through a grounding pad, they must still run through the IC core, and likely cause internal ESD failure anyway. Since CDM charge induction and charge storage can be random over the lifetime of an IC, CDM ESD failure can be unpredictable. Also, the industrial CDM test model (e.g., field-induction CDM, a.k.a., FICDM) is oversimplified, i.e., charge induction is carried out in a very short time period and the charges induced inside an IC cannot be distributed as they may be actually distributed within a chip in a real world; hence it is reasonable to doubt about the CDM testing results. This may be one root cause to the randomness of CDM ESD failure regardless of the CDM testing results.

B. *Internal-Distributed CDM ESD Protection*

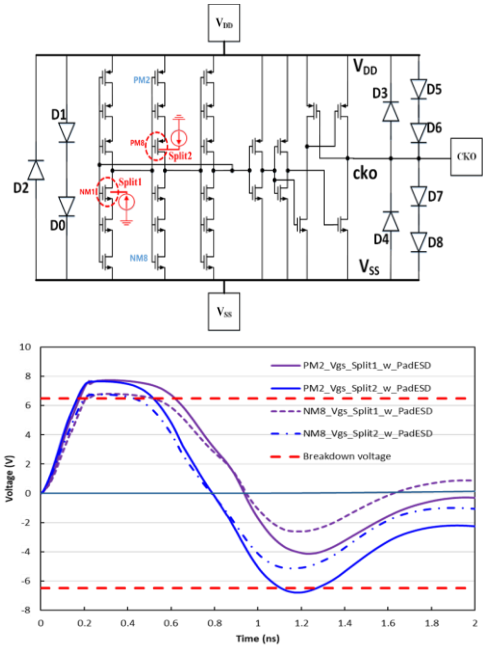
To resolve this major CDM ESD design challenge, a novel non-pad-based internal-distributed CDM ESD protection technique was recently reported [39]. The basic idea is that, since static charges are stored inside an IC; hence, an internal-distributed CDM ESD mesh network (Fig. 19a) can be designed to provide adequate CDM ESD protection. An AI-based Smart Partitioning technique can be used to analyze the chip layout and identify where the charges can be most likely stored (i.e., internal distribution within many tiny local "storage bins"). ESD devices are then placed at those internal nodes. When local charge accumulation reaches to certain level, it will trigger the local ESD device to discharge to local GND. As such, no complicated internal ESD discharge routing will occur and hence no internal CDM ESD failure will happen. It is worth to note that, since local ESD device is designed to handle small volume of static charges accumulated locally, these internal ESD devices can be much smaller than those normally needed at pads for the equivalent CDM ESD protection target. Practical implementation can vary, for example, the in-TSV ESD diodes



(a) (b)

Fig. 19 Conceptual illustration for internal-distributed CDM ESD protection: (a) a distributed CDM ESD mesh network on a chip, and (b) one way to realize internal distributed CDM ESD protection using interpose-based CDM ESD die flip-chip-bonded to a core die.

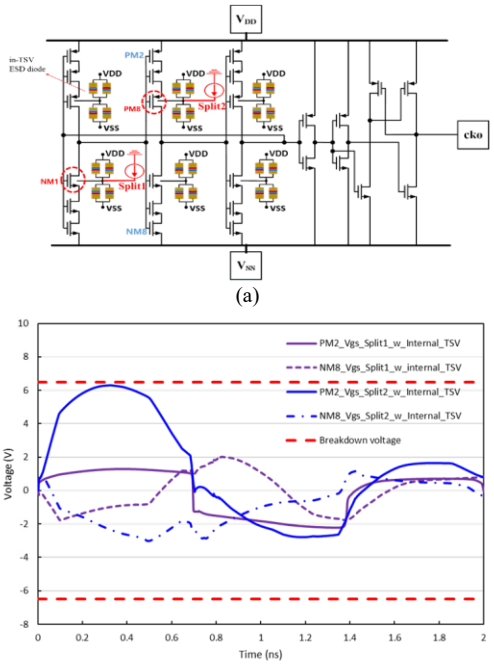
or interposer-based ESD network (Fig. 19b) discussed earlier can be used to constructed the internal-distributed CDM ESD mesh network. In a prototype validation, a 3-stage oscillator IC core was designed in a foundry 45nm SOI CMOS, which has a CDM ESD protection target of 500V [39]. There are two CDM ESD protection cases: Case 1 uses traditional pad-based CDM ESD protection, as depicted in Fig. 20a, consisting of ESD diodes at pad and diode-string power clamp, and the ESD diode



(a) (b)

Fig. 20 Case 1: a 3-stage oscillator IC with classic pad-based CDM ESD protection designed in a foundry 45nm SOI CMOS. The ESD diode size is 360μm for 500V CDM ESD protection. Smart partitioning identifies NM1 (Split 1) and PM8 (Split 2) as the internal charge storage bins. The two simulated CDM splits (Split 1 & Split 2) are discharged into V_{DD} pad. The CDM ESD failure criteria is gate breakdown BV_{OX}~6.5V: (a) core IC schematic, and (b) ESD failure occurs to PM2 and NM8 gates observed at 50V CDM ESD zapping.

size is 360μm for 500V CDM ESD protection. Case 2 uses a new non-pad-based internal-distributed CDM ESD mesh network, as shown in Fig. 21a, where the internal ESD diodes are the in-TSV diodes fabricated and their behavioral models are extracted from TLP testing for CDM ESD circuit simulation. A much smaller died size of 60μm is needed for the same CDM ESD protection. CDM ESD simulation was conducted for both cases. Smart partitioning identifies NM1 and PM8 as the likely internal charge storage bins; hence, CDM simulation was conducted accordingly by initiating CDM discharging from those two internal storage bins (i.e., two simulation splits). The CDM ESD failure criterion used is the internal gate breakdown voltage, i.e., BV_{OX}~6.5V in 45nm SOI. Fig 20b shows that CDM ESD failure occurs at 50V CDM zapping to Case 1 using classic pad-based CDM ESD protection. However, Case 2 utilizing the non-traditional internal-distributed CDM ESD mesh network can survive up to 350V CDM zapping. Obviously, CDM ESD protection requires more R&D efforts.



(a) (b)

Fig. 21 Case 2: same 3-stage oscillator IC with new internal-distributed CDM ESD protection. The internal ESD diode size is reduced to 60μm for the same CDM ESD protection. In-TSV ESD diodes and the behavioral models from TLP testing are used in CDM ESD circuit simulation: (a) core IC schematic, and (b) no gate failure observed up to 350V CDM ESD zapping.

VI. Disruptive ESD Protection Concepts

For about six decades, on-chip ESD protection has been almost entirely relying on in-Si PN-junction-based device structures for ESD discharging, which inherently introduces ESD design overhead (e.g, C_{ESD}, I_{leak}, noises and layout size) that is becoming unacceptable to complex ICs at advanced nodes [4]. Meanwhile, in the quest for future chips, one can imagine that entirely different ESD protection concepts will be needed. Disruptive thinking for future ESD protection mechanisms and structures are imperative to fundamentally resolve the problem in existing ESD protection solutions.

A. *Nano Crossbar ESD Protection*

One disruptive idea is to move an ESD device out of the Si substrate (frontend of the line, i.e., FEOL) and does not use an PN junction for ESD protection, hence eliminating the ESD parasitic effects inherent to PN junction. A novel above-IC nano crossbar array ESD protection concept was proposed [41]. Fig. 22a depicts the new ESD device structure, which is an array of nano crossbars with each node containing two metal electrodes with a dielectric layer in between. The metal electrodes are connected to IC pads as in normal on-chip ESD protection. The dielectric layer serves as an electric insulator (OFF) during normal IC operations. The device is made in the backend of the line (BEOL) in CMOS, hence being above the IC substrate. In a prototype, the dielectric layer is a $Si_xO_yN_z$ composite that is a phase-changing nano materials, which contains pre-diffused Cu ions inside serving as local tunnelling islands during ESD discharging. When an ESD pulse occurs to the electrode, it quickly turn ON the device, via phase changing, to form a low-R ESD conduction path to discharge the transient, hence providing ESD protection. Fig. 22b shows the measured ESD discharging I-V curve for a demo device and Fig. 22c presents the measured dual-directional ESD conduction I-V curve for a sample device, both by TLP testing. It is observed that the new nano crossbar structure functions as an ESD protection switch that can respond to ESD pulse with a rise time of 100ps, thanks to its local tunneling effect. The measured leakage is at ~pA level and the V_{t1} can be adjusted by device designs. TLP testing shows robust ESD current handling capability, i.e., I_{t2} ~ 8.11A for a 5x5 array device [41]. It can therefore save Si asset (above-IC) and reduce the number of ESD devices needed on a chip (dual-directional).

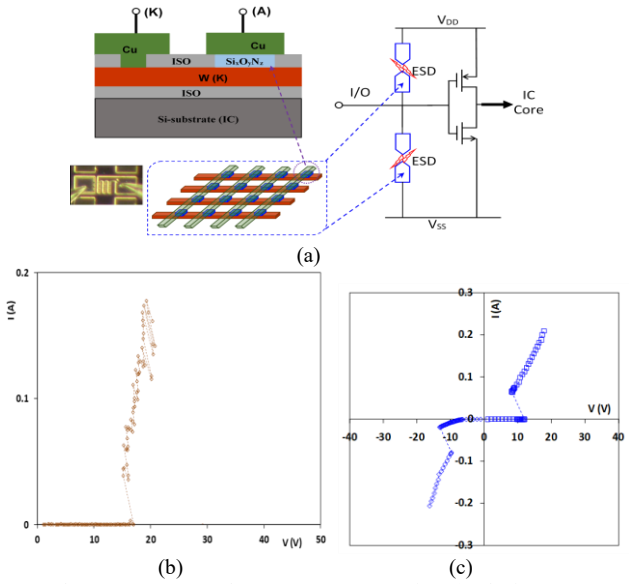


Fig. 22 Above-IC nano crossbar array ESD protection: (a) device structure and die photo, (b) TLP-measured ESD discharging I-V curve for a 1μm X 1μm crossbar node device, and (c) dual-directional ESD discharging I-V observed in TLP testing for a 5μm X 5μm crossbar node device.

B. *Graphene-Based ESD Protection*

A novel above-IC graphene NEMS (gNEMS) ESD switch device was developed as another future ESD protection solution [42]. It is well known that graphene has many unique materials properties, e.g., high mobility and thermal conductivity, superior mechanical strength, and high Young's modulus. These materials features are beneficial to ESD protection. Fig. 23a depicts the new gNEMS ESD switch structure that contains an air chamber covered by a graphene nano ribbon (GNR). The gNEMS device is fabricated in CMOS BEOL stack with the two electrodes connected to IC pads. gNEMS stays OFF during normal IC operations and has negligible impact on IC functions. During an ESD event, the transient electrostatic force will pull down the GNR to touch the bottom conductor, hence to turn ON the gNEMS to discharge the incident ESD pulses. When the ESD transient is over, the mechanical force will bring GNR back to turn off the gNEMS switch. Fig. 23b shows the measured ESD discharging I-V characteristic of a prototype gNEMS device by TLP testing, which clearly shows the desired dual-directional ESD I-V curve. Due to its high Young's Modulus, gNEMS can switch extremely fast, down to ~100pS in VFTLP testing. gNEMS has negligible ESD-induced parasitic effects due to its device structure, while achieving the highest reported ESD protection capability of J_{t2} ~ 1.19×10^{10} A/cm^2 (ESDV ~ 178KV/μm^2) under TLP stressing.

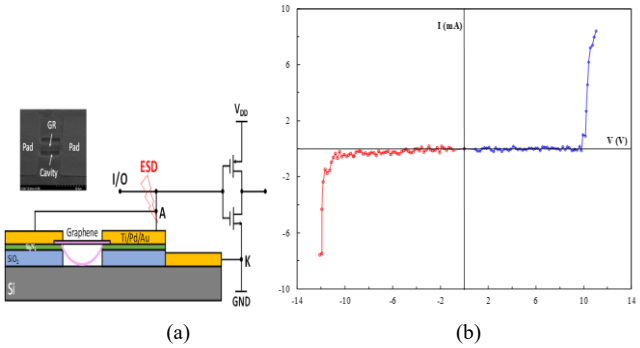


Fig. 23 An above-IC graphene NEMS ESD protection switch: (a) device structure, and (b) TLP-measured dual-directional ESD discharging I-V curve for a prototype device (d=350nm, W = 5μm, L = 7μm).

C. *Graphene ESD Protection Interconnects*

In practical IC designs, ESD metal interconnects are often designed very conservatively (i.e., wide) to avoid early ESD failure due to metal burning, which unfortunately brings in unacceptable parasitic capacitance. Graphene nano ribbon wires were proposed as future ESD interconnects due to its superior materials properties [43]. Fig. 24a illustrates the proposed GNR ESD interconnects schemes on a chip. GNR wires were thoroughly studies for ESD interconnects including its ESD protection capability, e.g., transient ESD failure threshold current (I_C) and current density (J_C), related to the length (L) and width (W) of GNR and TLP stressing pulse duration, etc. Fig. 24b presents the measured I_C/J_C ~ W curve by TLP test, which clearly shows that I_C increases for wider GNR wires. Such characteristics are essential to eventually design GNR wires to replace ESD metal interconnects.

VII. Future ESD Protection Perspective

A. *ESD Protection: More or Less?*

Understanding that IC performance and ESD protection normally adversely affect each other, the constant argument has been that how much ESD protection is enough. It is well known that ESD protection design becomes more and more

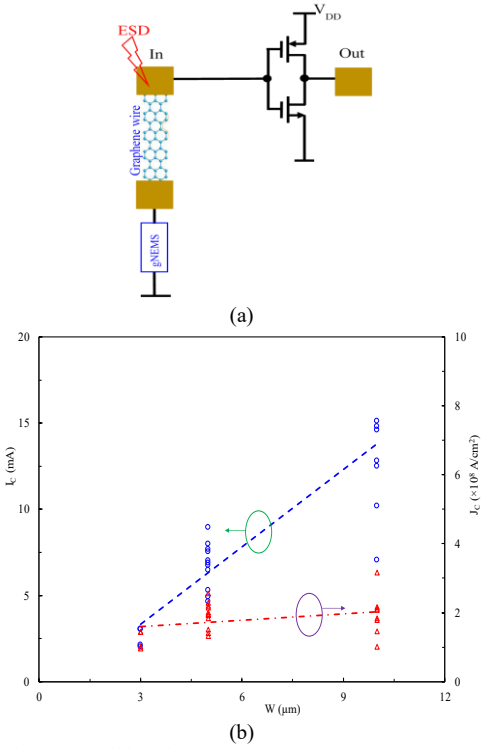


Fig. 24 Graphene nano ribbon for ESD protection interconnects: (a) ESD circuit schematic, and (b) TLP-measured critical voltage and current of GNR wires *versus* GNR length.

challenging for complex chips made at advanced technology nodes, mainly because the inherent ESD-induced design overhead problem can seriously affect IC performance. Recently, the Industrial Council on ESD Target Levels has released several white papers suggesting to dramatically reduce the ESD protection target levels of ICs, i.e., for HBM, from 2KV to 1KV (with Basic ESD Control, and to 500V with Detailed ESD Control), and for CDM, from 500V to 200V (with Basic ESD Control, and to 125V for ultrahigh-speed interfaces of 224Gbps with Detailed ESD Control) [44, 45]. There were two main rationales for the recommendations: first, enhanced ESD control existing today as required by OEMs; second, lack of correlation between ESD field returns of products (systems) and component (ICs) ESD qualification level. These white paper recommendations should be considered with great caution. It is recognized that the true motivation of the recommendations is that ESD protection design becomes increasingly challenging and the common HBM ESD protection level is becoming unsupportable for high-performance complex chips made at advanced technology nodes. Meeting the existing ESD target required by IC customers (system companies) leads to higher cost-of-ESD and longer time-to-market to IC suppliers (IC companies). However, one has to understand that ESD protection has both scientific (failure and field returns) and competitive (marketing) needs. Lack of clear correlation between product field returns and IC ESD protection levels is a problem of existing understanding, which requires more studies. Not seeing the link does not mean there is no link. It is obvious that poor IC ESD protection may not always ensure good system ESD protection, since system ESD failure may still occur at an unsatisfactory level even if all constituent ICs have high ESD protection. This is because a system is a complex product comprising many ICs and beyond. On the other hand, having good ESD control methods in factories is a small part of the whole ESD food chain, because ESD failures can occur anywhere all the way to the hands of end users, to whom even "basic" ESD control may be impossible (e.g., playing a smartphone with a wrist strap on). Therefore, the danger of ESD failure always exists and never shrunk as IC technology advances, while factory ESD control improves. In fact, ESD risk probably gets higher for advanced IC technologies (easier to damage to a thinner gate) and consumer electronics (e.g., smartphone and tablets). As such, simply choosing to reduce the ESD target levels and to shift ESD protection burden from IC suppliers (component level) to IC customers (system level) do not seem to be very reasonable [46-48]. On the contrary, engineers should think unconventionally to explore non-traditional ESD protection solutions in order to overcome the increasing on-chip ESD design challenges, such as the disruptive above-IC ESD protection concepts discussed in Sections V & VI. Nevertheless, IC ESD protection must certainly be considered jointly with system level ESD protection, which requires new thinking of cross-layer ESD protection.

B. Cross-Layer ESD Protection

It is important to know that IC ESD protection is never the ultimate goal in the ESD ecosystem. While on-chip ESD protection protects chips for IC suppliers, reducing ESD loss of system products is more important to IC customers. For on-chip ESD protection, the principle is to use a pad-based ESD protection network to discharge ESD transients efficiently (without overheating) and to clamp pad voltage safely (avoiding breakdown) through establishing a low-R ESD conduction path between any pad pairs, which is done by carefully designing the ESD-critical parameters to comply with the ESD Design Window [4]. Similarly, ESD protection must be considered at module (package laminate) and system (PCB) levels. Other than different ESD testing models required at chip, module and system levels, the ESD protection principle for modules and systems shall be analogue to on-chip ESD protection design. Treating components in a package or PCB as transistors on a chip, and Cu traces on laminate/PCB as metal interconnects of ICs. Simulation is needed for module/system level ESD protection designs, though being more difficult due to the physical boundaries at the chip/laminate/PCB interfaces. On the other hand, cross-layer ESD protection method becomes essential to modules and systems. It must be recognized that system level ESD protection is much more complex than that at IC level due to EMC/EMI considerations and different testing models (i.e., IEC, CDE, transient latch-up). To avoid possible huge revenue losses, system venders always use added board-level TVS/EMI protection components in addition to requiring adequate on-chip ESD protection for ICs. Further, a module/system contains many different chips from different IC suppliers fabricated in different IC technologies, which simply makes joint ESD protection design between IC/module/system a non-trivial task. Therefore, cross-layer ESD protection design becomes important, which is more vital to heterogeneous integration of a system comprising chips of different functionalities fabricated in disparate technologies. In addition, complexity of advanced packaging, e.g., 2.5D/3D IC stacking and CoWoS (chip on wafer on substrate), also complicates

overall ESD protection at packaging/system level. Cross-layer ESD protection requires non-traditional thinking in ESD designs, such as the post-Si field-programmable ESD protection concept discussed before where fine-tune of IC ESD at board level may be necessary.

C. ESD Protection for Chiplets

Heterogeneous integration (HI) and chiplet technologies offer a trending alternative to enrich the CMOS platform [49]. Chiplets are relatively smaller speciality dies made in disparate technologies that allow construction of complex system-on-integrated-chips/dies (SoIC/SoID). Compared to traditional monolithic system-on-chip (SoC) approach, HI-SoIC/SoID is arguably a low-cost solution with more flexibility that intends to put together individual advantages of the microelectronics ecosystem. As depicted in Fig. 25, a chiplet-based HI-SoIC can heterogeneously integrate many quite different functional dies, e.g., hi-performance CPU/GPU/NPU, high bandwidth memory stack, RF transceiver, wide bandgap power (e.g., GaN, SiC), various MEMS/NEMS and sensors and actuators together into one re-constructed SoIC chip (μ-system), all in a very flexible, efficient way for high-yield, low-cost production. Nevertheless, because of the physical boundaries among variety dies, the expected high system performance may only be possible if the intra-die communications will not be the signal bottleneck, which can be addressed using fine-pitch interconnects fabrics to network all chiplets through wafer-level chip-scale packaging (WLCSP). One proven solution is the CoWoS-based SoIC technology that integrates heterogeneous chiplets onto an organic substrate using IC-wafer process technologies. The high-throughput chiplet-chiplet interconnects techniques, such as μ-bumps, Cu pillars, Cu-Cu direct bonding, TSV, through-substrate Cu post, Si interposer and local bridge (low-cost alternative to full Si interposer), etc. However, while HI-SoIC/SoID is very promising to CMOS+ platforms, chiplet applications bring in new challenges to ESD protection designs. Due to the physical boundaries among chiplets, full-SoIC/SoID ESD protection can be more challenging than system-level ESD protection design due to its wafer-scale IC-grade feature dimensions. In general, the cross-layer ESD protection design methodology can be applied to chiplet SoIC (or, dielet SoID) μ-systems with IC-level considerations. For example, on-die ESD

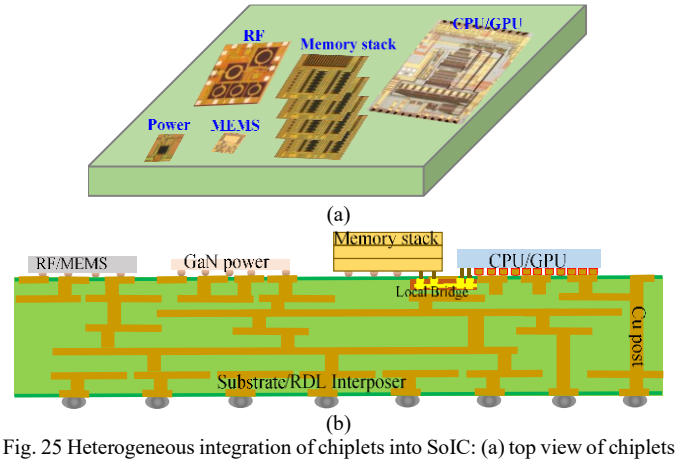


Fig. 25 Heterogeneous integration of chiplets into SoIC: (a) top view of chiplets on substate, and (b) X-section view of CoWoS packaging where interposer can be RDL/substrate or Si interposer, and local bridge may replace Si interposer. ESD protection can be in interposer or TSV or through-substrate post.

protection is still required for all chiplets because they are from different IC suppliers. Post-Si field-programmability may be essential to fine-tune V_{t1} for different chiplets, particularly, when chip replacement becomes inevitable to reduce the time-to-market of new SoIC/SoID products. To this end, the industry is currently proposing to establish the University Chiplet Interconnect Express (UCIe) protocol to facilitate standardized procedures to develop chiplet-based HI-SoIC products, for which one can expect that ESD reliability will be a major concern beyond SoIC performance [50]. Interposer-based ESD protection can be utilized either in Si interposer or Cu-RDL substrate interposer format. In-TSV ESD protection discussed before can be expanded into the through-substrate vias, which are normally used as vertical Cu posts. Similar to domain-to-domain (i.e., different power and function blocks) ESD design consideration in a monolithic SoC, a full-SoIC ESD protection network must be ensured across different chiplet dies (physical boundaries in SoIC *versus* electrical domains on a monolithic SoC chip). On the other hand, HI-SoIC may be more friendly to ESD simulation because all chiplets involved are at the same IC die level, compared to system-level ESD simulation that must communicate data across different physical dimension levels (die and PBC). Such challenges and options will no doubt make ESD protection for chiplet SoIC μ-systems very involving, which requires significant R&D efforts down the road.

VIII. Future ESD Protection Perspective

Despite advances in ESD design techniques and ESD protection solutions, there is no doubt that ESD protection will continue to be one major IC reliability challenge. For future chips (monolithic or chiplets) and emerging technologies, ESD danger remains and likely increases relative to technology sensitivity. Meanwhile, ultrahigh performance and very complex chips make ESD protection designs more complicated. Nevertheless, reducing ESD qualification target shall not be a good solution. Instead, future ESD protection requires non-traditional thinking and new design space exploration. The following key aspects may be future ESD protection perspective. First, the ESD protection fundamental remains the same, i.e., designing ways to discharge any ESD transients safely and swiftly. Second, any switch (Fig. 1) that can be precisely controlled can be a good ESD protection solution, which may be implemented in different physical varieties. Third, cross-layer ESD protection (i.e., co-design) will be very important for IC chips (monolithic or HI-SoIC, i.e., μ-system), module (sub-systems) and systems. Heterogeneity (functionality and technology) demands for a holistic full-scale consideration in ESD protection designs. Fourth, any ESD protection must be carried out using CAD and full-chip/system physical design verification by CAD will be required for any ESD protection designs. This also requires major R&D efforts to develop new CAD algorithms and tools to facilitate cross-layer and full-system ESD simulation that must be ESD function based (i.e., multi-physics). Fifth, disruptive thinking is required to explore non-traditional revolutionary ESD protection concepts for ultrahigh-performance chips and highly heterogeneous future μ-systems (e.g., beyond electronics), for example, graphene-based gNEMS ESD protection concept

discussed before. Sixth, with emerging above-IC ESD protection structures, it may be possible that future ESD protection could be made in BEOL (or in interposers) and provided by a foundry as validated ESD IPs, representing a paradigm shift in ESD protection design practice in near future. Self-limiting your mind to traditional in-Si PN-based ESD protection methods only will go nowhere. It is the time to re-think about ESD protection!

IX. Summary

This paper provides a topical overview of recent advances in selected critical aspects of on-chip ESD protection designs, with a focus on novel ESD protection concepts and design techniques, which have been experimentally validated. ESD basics, such as switch-based ESD protection, ESD-critical parameters, ESD design window and shrinking, and ESD design overhead, are provided in the Introduction. It goes on to depict the ESD-RFIC co-design method that is critical to ESD protection designs for high-speed, high-frequency and broadband ICs. ESD CAD simulation techniques are then discussed that support ESD design optimization, prediction and physical design verification. It then uses examples to argue that non-traditional thinking on ESD protection designs becomes critical to ensure un-discounted ESD protection for advanced ICs (SoC or SoIC), which are increasingly more complex, heterogeneous and depending upon advanced IC technologies, therefore, making ESD protection designs extremely challenging. An outlook to future ESD protection for future chips is given that relies more on CAD techniques, holistic design methodologies and disruptive thinking.

References

[1] E. A. Amerasekera and C. Duvvury, *ESD in Silicon Integrated Circuits*, Wiley, ISBN-13: 978-0471954811, 1996.

[2] S. Dabral and T. Maloney, *Basic ESD and I/O Design*, Wiley, ISBN-13: 978-0471253594, 1998.

[3] S. Voldman, *ESD: RF Technology and Circuits*, Wiley, ISBN-13: 978-0470847558, 2006.

[4] A. Wang, *Practical ESD Protection Design*, IEEE-Wiley, ISBN-13: 978-1119850403, 2021.

[5] S. Voldman, G. Gerosa, V. Gross, N. Dickson, S. Furkay and J. Slinkman, "Analysis of snubber-clamped diode-string mixed voltage interface ESD protection network for advanced microprocessors", J. Electrostatics, 38 (1996), pp. 3-31.

[6] J. Chen, A. Amerasekera and T. Vrotsos, "Bipolar SCR ESD Protection Circuit for High Speed Submicron Bipolar/BiCMOS Circuits", *IEEE IEDM Tech. Digest*, pp. 337-340, 1995.

[7] A. Wang and C. Tsay, "On a Dual-polarity on-Chip Electrostatic Discharge Protection Structure", *IEEE Trans. Elec. Devices*, *Vol. 48, No. 5,* pp. 978-984, May 2001.

[8] H. Feng, R. Zhan, K. Gong and A. Wang, "A New Pad-Oriented Multiple-Mode ESD Protection Structure and Layout Optimization", *IEEE Electron Device Letters, Vol. 22, No. 10,* pp. 493-495, October 2001.

[9] S. Voldman, F. Assaderaghi, J. Mandelman, L. Hsu and G. Shahidi, "Dynamic Threshold Body- and Gate-Coupled SOI ESD Protection Networks", J. Electrostatics, 44 (1998), pp. 239-255.

[10] D. Tremouilles, S. Thijs, C. Russ, J. Schneider, C. Duvvury, N. Collaert, D. Linten, M. Scholz, M. Jurczak, H. Gossner and G. Groeseneken, "Understanding the optimization of sub-45nm FinFET devices for ESD applications", *IEEE Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, 2007.

[11] Y. Ma and G. P. Li, "A novel on-chip ESD protection circuit for GaAs HBT RF power amplifiers", *Proc. IEEE Electrical Overstress/Electrostatic Discharge Symposium*, pp. 83-91, 2002.

[12] A. Mishra and M. Shrivastava, "New insights on the ESD behavior and failure mechanism of multi wall CNTs", *Proc. IEEE International Reliability Physics Symposium (IRPS)*, 2016.

[13] W. Liu, J. J. Liou, A. Chung, Y. Jeong, W. Chen and H. Lin, "Electrostatic Discharge Robustness of Si Nanowire Field-Effect Transistors", *IEEE Electron Device Letters*, *Vol. 30, No. 9,* pp. 969-971, Sept. 2009.

[14] A. Tazzoli, F. Danesin, E. Zanoni and G. Meneghesso, "ESD robustness of AlGaN/GaN HEMT devices", *Proc. IEEE Electrical Overstress/Electrostatic Discharge Symposium (EOS/ESD)*, 2007.

[15] T. Phulpin, D. Tremouilles, K. Isoird, D. Tournier, P. Godignon and P. Austin, "Failure analysis of ESD-stressed SiC MESFET", *Microelectronics Reliability, Vol. 55, No. 9-10,* pp. 1542-1548, August-September, 2015.

[16] A. Wang, H. G. Feng, K. Gong, R. Y. Zhan and J. Stine, "On-Chip ESD Protection Design for Integrated Circuits: an Overview for IC Designers", *Microelectronics Journal, Vol. 32, No. 9,* pp. 733-747, September 2001.

[17] A. Wang and C. Tsay, "A New Design Methodology Using Simulation for on-chip ESD Protection for Integrated Circuits", *Proc. IEEE Int. Conf. Solid-State & IC Technology (ICSICT)*, pp. 509-512, 1998.

[18] L. Lin, X. Wang, H. Tang, Q. Fang, H. Zhao, A. Wang, R. Zhan, H. Xie, C. Gill, B. Zhao, Y. Zhou, G. Zhang and X. Wang, "Whole-Chip ESD Protection Design Verification by CAD", *Proc. EOS/ESD Symp.,* pp. 28-37, 2009.

[19] Z. Shi, X. Wang, J. Liu, L. Lin, H. Zhao, Q. Fang, L. Wang, C. Zhang, S. Fan, H. Tang, B. Li, A. Wang, J. Liu, and Y. Cheng, "Programmable on-Chip ESD Protection Using Nano Crystal Dots Mechanism and Structures", *IEEE Trans. Nanotechnology, Vol. 11, No. 5,* pp. 884-889, September 2012.

[20] A. Wang, H. Feng, R. Zhan, G. Chen and Q. Wu, "ESD Protection Design for RF Integrated Circuits: New Challenges", *Proc. IEEE Custom IC Conf. (CICC),* pp. 411-418, 2002.

[21] M. Di, Z. Pan, F. Zhang, C. Li, H. Wang and A. Wang, "A Study of ESD-mmWave-Switch Co-Design of 28GHz Distributed Travelling Wave Switch in 22nm FDSOI for 5G Systems", *IEEE J. of Electron Devices Society (J-EDS), Vol. 6,* pp. 1290-1296, December 2021.

[22] A. Wang, H. Feng, R. Zhan, H. Xie, G. Chen, Q. Wu, X. Guan, Z. Wang and C. Zhang, "A Review on RF ESD Protection Design", *IEEE Trans. Electron Devices, Vol. 52, No. 7,* pp. 1304-1311, July 2005.

[23] V. Chandrasekhar, C. M. Hung, Y. C. Ho and K. Mayaram, "A Packaged 2.4GHz LNA in a 0.15μm CMOS Process with 2KV HBM ESD Protection", *Proc. IEEE ESSCIRC*, pp. 347-350, 2002.

[24] F. Lu, R. Ma, Z. Dong, L. Wang, C. Zhang, C. Wang, Q. Chen, X. S. Wang, F. Zhang, C. Li, H. Tang, Y. Cheng and A. Wang, "A Systematic Study of ESD Protection Co-Design with High-Speed and High-Frequency ICs in 28nm CMOS", *IEEE Trans. Circuits and Systems I: Regular Papers, Vol. 63, Issue 10,* pp.1746-1757, October, 2016.

[25] X. Guan, X. Wang, L. Lin, G. Chen, A. Wang, H. Liu, Y. Zhou, H. Chen, L. Yang and B. Zhao, "ESD-RFIC Co-Design Methodology", *Proc. IEEE RFIC*, pp467-470, 2008.

[26] X. S. Wang, X. Wang, F. Lu, C. Zhang, Z. Dong, L. Wang, R. Ma, Z. Shi, A. Wang, M-C. F. Chang, D. Wang, A. Joseph and C. P. Yue, "Concurrent Design Analysis of High-Linearity SP10T Switch with 8.5kV ESD Protection", *IEEE J. Solid-State Circuits, Vol. 49, No. 9,* pp. 1927 – 1941, September 2014.

[27] C. Diaz, S. M. Kang and C. Duvvury, "Circuit-Level Electricalthermal Simulation of Electrical Overstress Failures in Advanced MOS I/O Protection Devices", *IEEE Transactions on CAD, Vol. 13, No. 4*, pp. 482-493, 1994.

[28] H. Xie, R. Zhan, H. Feng, G. Chen, Albert Wang and R. Gafiteanu, "A 3D Mixed-Mode ESD Protection Circuit Simulation-Design Methodology", *Proc. IEEE CICC,* pp243-246, 2004.

[29] H. Feng, G. Chen, R. Zhan, Q. Wu, X. Guan, H. Xie, A. Wang and R. Gafiteanu, "A Mixed-Mode ESD Protection Circuit Simulation-Design Methodology", *IEEE J. Solid-State Circuits, V38, No. 6*, pp. 995-1006, June 2003.

[30] A. Wang, C. Tsay and P. Deane, "A Study of NMOS Behaviours under ESD Stress: Simulation and Characterization", *Microelectronics Reliability, 38*, pp. 1183-1186, 1998.

[31] Z. Pan, C. Li, M. Di, F. Zhang and A. Wang, "3D TCAD Analysis Enabling ESD Layout Design Optimization", *IEEE J. of Electron Devices Society (J-EDS), Vol. 8,* pp. 1289-1296, September 2020.

[32] F. Zhang, C. Wang, F. Lu, Q. Chen, C. Li, X. S. Wang, D. Li and A. Wang, "A Full-Chip ESD Protection Circuit Simulation and Fast Dynamic Checking Method Using SPICE and ESD Behavior Models",

IEEE Trans. Computer-Aided Design of Integrated Circuits and Systems, Vol. 38, No. 3, pp. 489-498, March 2019.

[33] R. Zhan, H. Feng, Q. Wu and A. Wang, "ESDExtractor: A New Technology-Independent CAD Tool for Arbitrary ESD Protection Device Extraction", *IEEE Transaction on Computer-Aided Design of Integrated Circuits and Systems, Vol. 22, No. 10*, pp. 1362-1370, October 2003, DOI: 10.1109/TCAD.2003.818140.

[34] R. Zhan, H. Feng, Q. Wu, H. Xie, X. Guan, G. Chen and A. Wang, "ESDInspector: A New Layout-level ESD Protection Circuitry Design Verification Tool Using A Smart-Parametric Checking Mechanism", *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, Vol. 23, No. 10,* pp. 1421-1428, October 2004, DOI: 10.1109/TCAD.2004.833613.

[35] A. Wang and R. Zhan, "A Parameter Checking Method for on-Chip ESD Protection Circuit Physical Design Layout Verification", *U.S. Patent No. 7,243,317B2,* 2007.

[36] X. Wang, Z. Shi, J. Liu, L. Lin, H. Zhao, L. Wang, R. Ma, C. Zhang, Z. Dong, S. Fan, H. Tang, A. Wang, Y. Cheng, B. Zhao, Z. Zhang, B. Chi and T. Ren, "Post-Si Programmable ESD Protection Circuit Design: Mechanisms and Analysis", *IEEE J. Solid-State Circuits, Vol. 48, No. 5*, pp. 1237-1249, May 2013.

[37] C. Zhang, Z. Dong, F. Lu, R. Ma, L. Wang, H. Zhao, X. Wang, X. S. Wang, H. Tang and A. Wang, "Fuse-Based Field-Dispensable ESD Protection for Ultra-High-Speed ICs", *IEEE Electron Device Letters. Vol. 35, No. 3,* pp.381-383, March 2014.

[38] C. Li, M. Di, Z. Pan, H. Wu and A. Wang, "Vertical TSV-Like Diode ESD Protection", *Proc. IEEE Electron Devices Technology and Manufacturing Conference (EDTM),* pp. 676-678, 2021.

[39] M. Di, C. Li, Z. Pan and A. Wang, "Non-Pad-Based in Situ in-Operando CDM ESD Protection Using Internally Distributed Network", *IEEE J. of Electron Devices Society (J-EDS), Vol. 9,* pp. 1248-1256, December 2021.

[40] M. Di, C. Li, Z. Pan and A. Wang, "Pad-Based CDM ESD Protection Methods Are Faulty", *IEEE J. of Electron Devices Society (J-EDS), Vol. 8,* pp. 1297-1304, September 2020.

[41] L. Wang, X. Wang, Z. Shi, R. Ma, J. Liu, Z. Dong, C. Zhang, L. Lin, H. Zhao, L. Zhang, Y. Cheng, R. Huang and A. Wang "Dual-Directional Nano Crossbar Array ESD Protection Structures", *IEEE Electron Device Letters, Vol. 34, No. 1,* pp. 111-113, January 2013.

[42] R. Ma, Q. Chen, W. Zhang, F. Lu, C. Wang, A. Wang, Y. H. Xie and H. Tang, "A Dual-Polarity Graphene NEMS Switch ESD Protection Structure", *IEEE Electron Device Letters, Vol. 37, No. 5,* pp. 674-676, May 2016.

[43] Q. Chen, R. Ma, W. Zhang, F. Lu, C. Wang, O. Liang, F. Zhang, C. Li, H. Tang, Y-H. Xie and A. Wang, "Systematic Characterization of Graphene ESD Interconnects for on-Chip ESD Protection", *IEEE Trans. Electron Devices, Vol. 63, No. 8,* pp. 3205-3212, July 2016.

[44] White paper 1: A Case for Lowering Component Level HBM ESD Specifications and Requirements, *Industry Council on ESD Target Levels, Rev. 4.0*, June 2018.

[45] White paper 2: A Case for Lowering Component-Level CDM ESD Specifications and Requirements, *Industry Council on ESD Target Levels, Rev. 3.0*, May 2021.

[46] White paper 3: System Level ESD, Part I: Common Misconception and Recommended Basic Approaches, *Industry Council on ESD Target Levels, Rev. 1.0*, December 2010.

[47] White paper 3: System Level ESD, Part II: Implementation of Effective ESD Robust Designs, *Industry Council on ESD Target Levels, Rev. 2.0*, March 2019.

[48] White paper 3: System Level ESD, Part III: Review of IEC61000-4-2 ESD Testing and Impact on System-Efficient ESD Design (SEED), *Industry Council on ESD Target Levels, Rev. 1.1*, May 2021.

[49] Heterogeneous Integration Roadmap, *IEEE Heterogeneous Integration Roadmap Committee, Edition 2021*, 2021.

[50] UCIe – Universal Chiplet Interconnect Express, *Universal Chiplet Interconnect Express (UCIe) consortium*, https://www.uciexpress.org/.