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Flash light assisted additive manufacturing of 3D structural electronics (FLAME)

Md Naim Jahangir [a], Jeremy Cleeman [a], Changqin Pan [b], Chih-Hung Chang [b], Rajiv Malhotra [a,*]

[a] Mechanical & Aerospace Engineering, Rutgers University, Piscataway, NJ 08854, USA
[b] Chemical, Biological & Environmental Engineering, Oregon State University, Corvallis, OR 97331, USA

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ABSTRACT

Additive integration of 3D electrical circuits with off-the-shelf electronic devices inside 3D printed polymer parts, i.e., structural electronics, can enable new paradigms in miniaturized multifunctional structures. This paper investigates a hybrid printing process called Flash Light Assisted Manufacturing of structural Electronics (FLAME) which integrates Fused Filament Fabrication (FFF) of polymers with printing and Intense Pulsed Light sintering (IPL) of silver nanoparticles. The effect of IPL parameters and nanoparticle shape on conductivity is quantified, revealing that using NWs with IPL allows greater conductivity with lesser sintering-induced polymer damage. The conductivity of planar circuits is characterized during over-FFF, i.e., during FFF of the polymer on the sintered circuit. An unexpected finding is that over-FFF increases the conductivity in a complex and non-monotonic manner that depends on the over-FFF parameters. A multi-layer IPL strategy is introduced for through-plane circuits, in which NWs are deposited in increments smaller than the circuit's total height and IPL is performed after each increment. Electromagnetic and thermal simulations reveal why through-plane circuits have lesser conductivity than planar ones and uncover the key role of multi-layer IPL in increasing the conductivity of through-plane circuits. Overall, FLAME increases the conductivity by 300 % for planar circuits and by 170 % for through-plane circuits as compared to state-of-the-art nanoparticle printing-based methods, even for low-thermal-tolerance polymers, in less than 10 s for each polymer layer. These advances break the performance-material-throughput tradeoff that plagues existing nanoparticle-based printing methods for fabricating 3D structural electronics.

1. Introduction

Structural electronics consist of off-the-shelf electronic devices connected by electrically conductive circuits in 3D layouts inside rigid 3D polymer parts (Fig. 1a). This paradigm can transform conventional parts that have a desired shape and structural behavior into smart structures with additional electromechanical, thermal, chemical, optical, communication, and magnetic functionality [1]. This approach can also reduce the planar footprint of electronic systems by using the part volume to accommodate 3D device and circuit layouts, thus enabling greater structural miniaturization and light-weighting than planar or surface-conformal electronics. These advantages can be leveraged for applications in communication [2], sensing [3], control [4], unmanned vehicles [5], biomedical implants [6,7], and other smart structures [8–10].

High circuit conductivity is crucial to the performance of structural electronics. For the same circuit dimensions and voltage the power consumption of a circuit increases proportionally as the circuit's conductivity reduces. Greater power usage reduces system capabilities by depleting the power source faster, e.g., reducing the range of drones. Low conductivity also limits system functionality. For example, for the same circuit dimensions and current supplied a lower circuit conductivity will proportionally reduce the voltage supplied to a motor and thus reduce its speed or torque, or reduce the performance of electromagnetic coil antennae fabricated with standalone circuits [11]. Increasing the cross section of a circuit can compensate for low conductivity but this approach is limited by the fact that circuit pitch needs to match pin-to-pin distance on the devices. While circuit conductivity must be increased, concurrent elimination of polymer degradation and melting during manufacturing is critical to freeing the choice of the polymer material from the circuit fabrication process in order to retain low costs and preserve the non-electronic functionality of the polymer.

An emerging approach for fabricating 3D structural electronics is to

* Corresponding author.
E-mail address: rajiv.malhotra@rutgers.edu (R. Malhotra).

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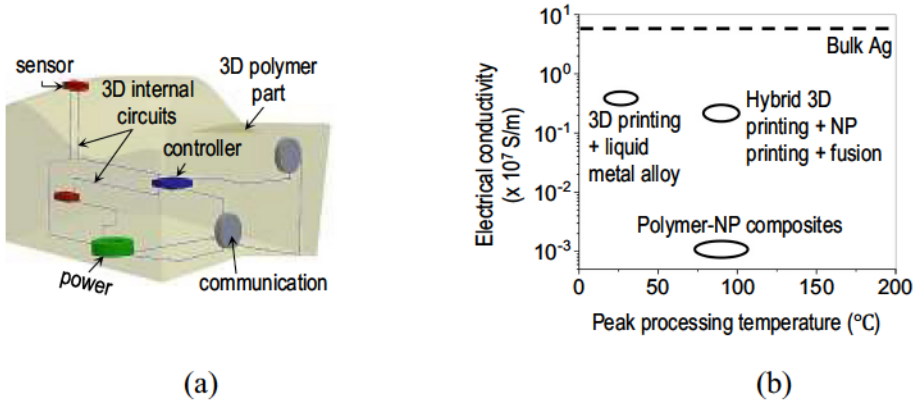

Fig. 1. (a) Schematic of structural electronics. (b) Circuit conductivity and peak processing temperature for existing techniques used to fabricate structural electronics.

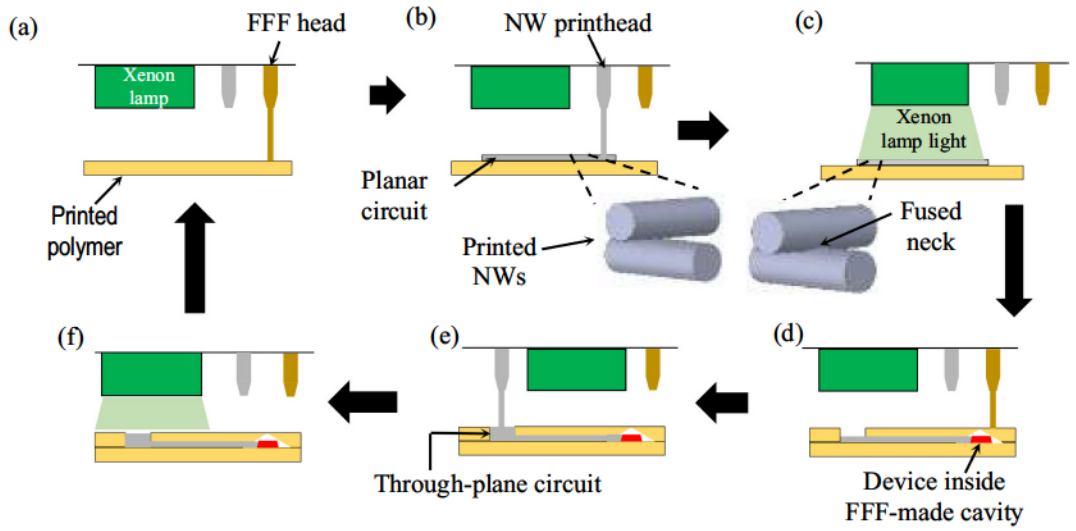

Fig. 2. Schematic of FLAME process (NW denotes nanowire).

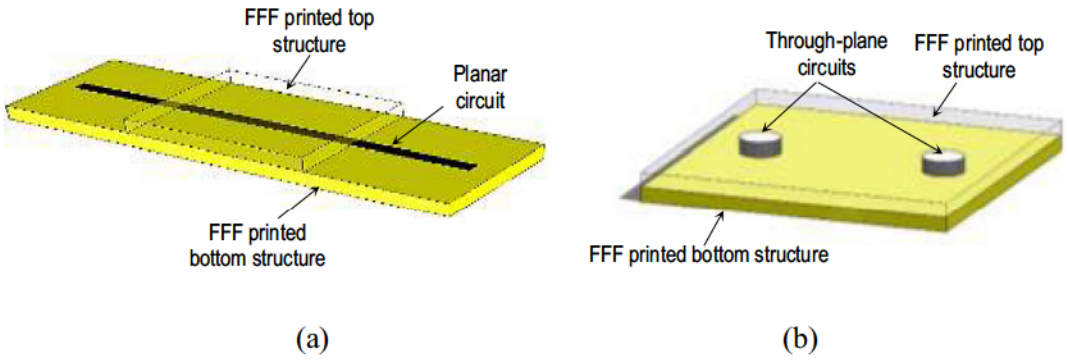

Fig. 3. Testing sample configuration for (a) planar circuit (b) through-plane circuit.

Table 1
FFF parameters used in experiments.

Parameters	Values
Raster angle	45° alternating
Build plate temperature	110 °C for ABS and 60 °C for PLA
Extrusion temperature	250 °C for ABS and 215 °C for PLA
Nozzle diameter	0.4 mm

combine polymer 3D printing, fabrication of electrically conductive circuits inside the polymer, and connection of devices placed inside 3D printed cavities to these circuits. This fabrication paradigm allows extraordinary design freedom via the concurrent creation of internal 3D electronics and structurally-motivated part geometry in a single fabrication platform. The 3D printed polymer acts as a dielectric layer for the circuits and as a packaging element that prevents exposure of the circuits to the environment. 3D printing of polymers and pick-and-place

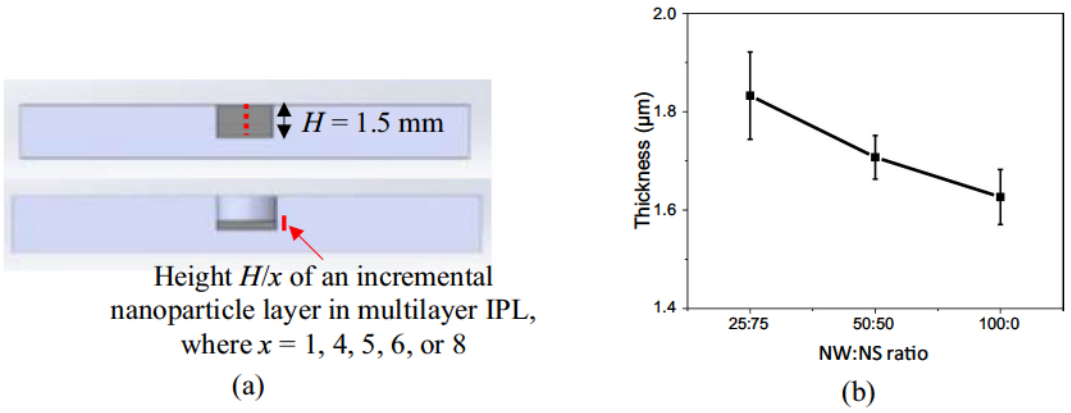

Fig. 4. (a) Schematic of nanoparticle layer height during multilayer IPL of a through-plane circuit in a FFF-made hole of height *H*. (b) Effect of NW:NS ratio on thickness of the as-printed planar circuit.

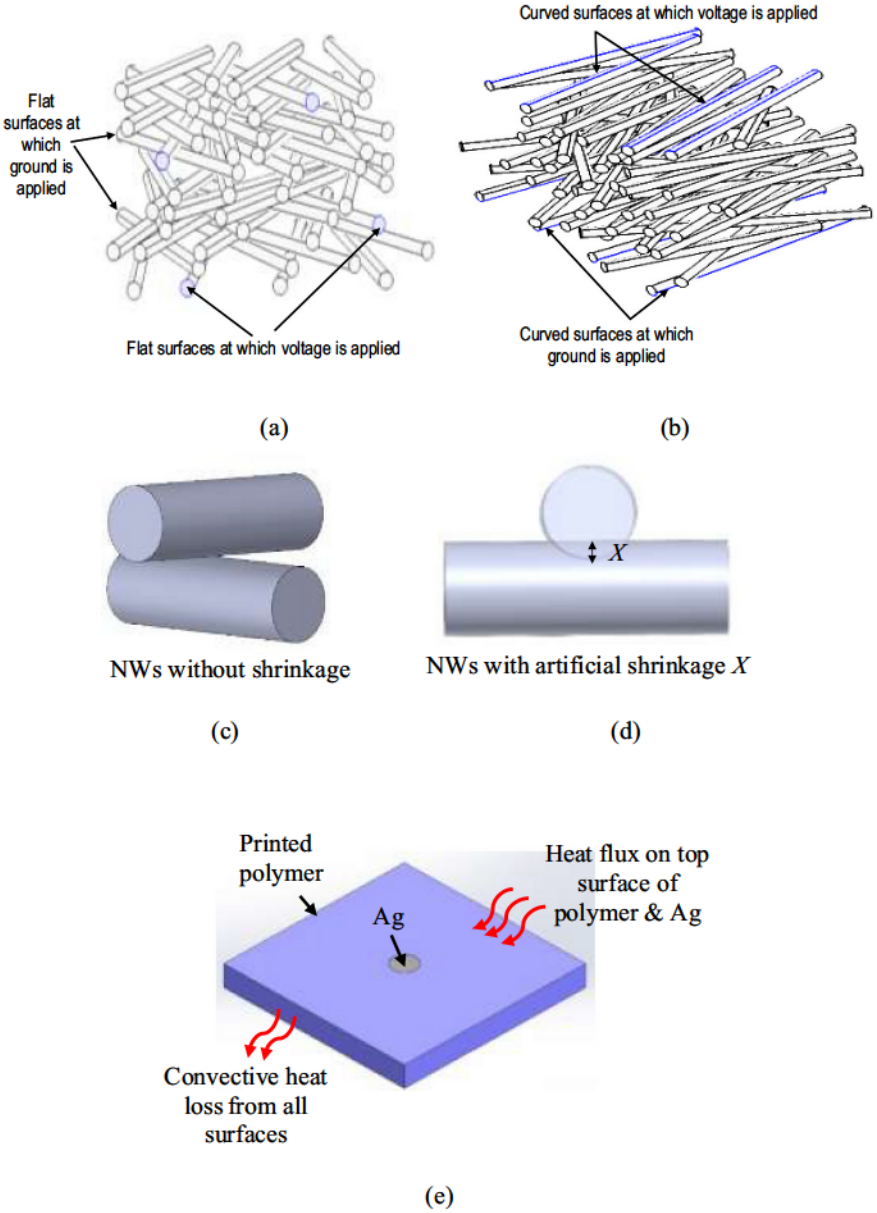

Fig. 5. Schematic of electrical FEA of NW ensemble for (a) planar circuit (b) through-plane circuit. (c–d) Artificial shrinkage *X* for a NW pair. (e) Thermal FEA of through-plane circuit.

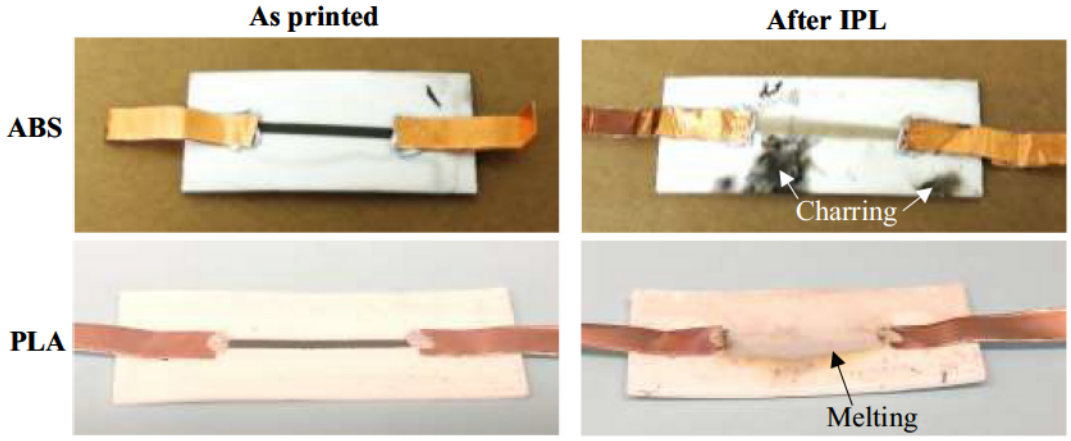

Fig. 6. IPL-induced damage of FFF-printed ABS and PLA with NW:NS ratio of 0:100.

assembly of devices are well established aspects of this paradigm. Fig. 1b compares existing processes for fabricating 3D internal conductive circuits. Ultrasonic embedding of wires is not discussed as it cannot yet create multiple internal 3D circuits. Methods used for fabricating Molded Interconnect Devices are omitted since they are usually confined to creating circuits on the surface of a structure and use molding rather than 3D printing.

FFF or stereolithography of polymer-nanoparticle composites (e.g., with metal or graphene nanospheres, nanowires, nanoflakes) yields conductivity that is orders of magnitude lesser than the intrinsic value of the nanoparticle material. This is due to tunneling based rather than ohmic percolation driven electron transport in the circuit [12]. Conductive liquid metal alloys like EGaIn have been used by injecting the liquid metal into cavities printed inside the structure [13,14]. This requires redesign of the structure's internal geometry which can affect its non-electronic function. The repeatability of this method is restricted by continuity of flow of the viscoelastic and highly wetting liquid metal inside the internal cavities, e.g., the formation of gaps and bubbles in the liquid metal circuit often breaks the conductive pathway [15]. Finally, the intrinsic conductivity of these liquid metal alloys is about 17 times lesser than that of bulk Ag or Cu whereas nanoparticle-based planar circuits have achieved conductivities that are only 3 times lesser than the bulk value [16].

The more general hybrid printing approach integrates 3D printing of the polymer with printing and sintering of metal nanoparticles to create complex high-resolution conductive 3D circuits inside 3D parts. Ohmic rather than percolative electron transport after sintering enables greater conductivity than polymer-nanoparticle composites. While tool development efforts (e.g., by Nano-Dimension) show that hybrid printing has the greatest potential to realize high-performance structural electronics, this approach still suffers from the following conductivity-material-throughput tradeoff [17–19]. In such hybrid printing techniques the conductivity of the printed material increases with interparticle fusion during sintering [20]. State-of-the-art hybrid printing typically prints metal nanospheres or nanoflakes as circuits and sinters them using oven heating outside the printing machine [21] or using in-situ laser heating [22–26]. Since direct laser sintering often causes significant thermal degradation of polymer structures, a more time-consuming alternative is often used in which laser pre-curing of the NPs is followed by low temperature-long duration oven curing (e.g., 80 °C for 16 h [26]). A more typical sintering approach places the structure printed with the embedded circuits inside an oven. The sintering is either performed rapidly at high temperature (10–30 min at 250–350 °C [21,27]) which limits the polymer material to more costly thermosets or polyamides, or is performed slowly at low temperature (e.g., 80 °C for 1.5–2 h [3,28]) which reduces the process throughput significantly. The best damage-free electrical conductivity achieved till date with the oven-based sintering approach is 2×10^6 S/m for planar circuits and 2.72×10^4 S/m for through-plane circuits (i.e., circuits that go across the FFF layers), that too with a thermally resistant thermoset material [3]. Overall, using cheaper and more thermally intolerant thermoplastics like PLA, ABS, or their composites limits the thermal budget available for sintering and thus limits the circuit's conductivity. Trying to avoid thermal damage by increasing the sintering time and reducing the sintering temperature significantly reduces the overall process speed. Thus, realizing the advantages of hybrid nanoparticle-based printing for structural electronics requires its seamless integration with a nanoparticle sintering process that can achieve high electrical conductivity, at high throughput, with minimal thermal damage of thermally intolerant 3D printed polymer structures.

This paper develops a process called Flash light Assisted Additive Manufacturing of structural Electronics (FLAME, Fig. 2) to overcome the above performance-material-throughput tradeoff. FLAME integrates Fused Filament Fabrication (FFF), printing of nanoparticles (NPs) into planar and through-plane circuits, in-situ Flash Light/Intense Pulsed Light sintering (IPL) of the printed nanoparticle-based circuits, and connection of off-the-shelf functional devices with the circuits. FFF and nanoparticle printing are well known techniques. IPL uses broad-spectrum visible light from a xenon lamp to irradiate and thermally sinter NPs over an area as large as 1 ft by 1 in. within milliseconds. The low irradiation time and the plasmon resonance effect created by the use of nanoparticles minimizes damage even for very sensitive substrates like paper and polyester. The increase in the conductivity of the printed nanoparticle ensembles is achieved via interparticle diffusion and neck growth driven by the optically-induced heating. Since IPL can be performed under ambient conditions it can be easily integrated with FFF, printing and device integration. The area-based rather than writing-based nature of IPL also gives it a throughput advantage over laser sintering. Various methods for sintering metal nanoparticle circuits on planar flexible substrates have achieved near-bulk conductivity. [29–37] Among these IPL provides additional advantages of exceptionally low thermal damage due to rapid and highly efficient energy transfer from the incident light to the metal nanoparticles via plasmonic resonance, high throughput over large areas on the feet scale, and elimination of physical contact with the circuits. This makes IPL an ideal candidate to meet our goal of seamless integration with a continuous 3D printing process. [16,32–36,38–47] For example, past work on IPL of Ag NW-based planar printed circuits on planar substrates has reduced peak sintering temperatures to as low as 125 °C, increased circuit conductivity to as high as 2×10^7 S-m, within milliseconds of IPL, over feet length scales if needed, and shown that such advantages are hard to achieve with other sintering methods. [33,48,49]

But these advantages of IPL have not been translated to structural electronics yet, where optical and thermal penetration into through-

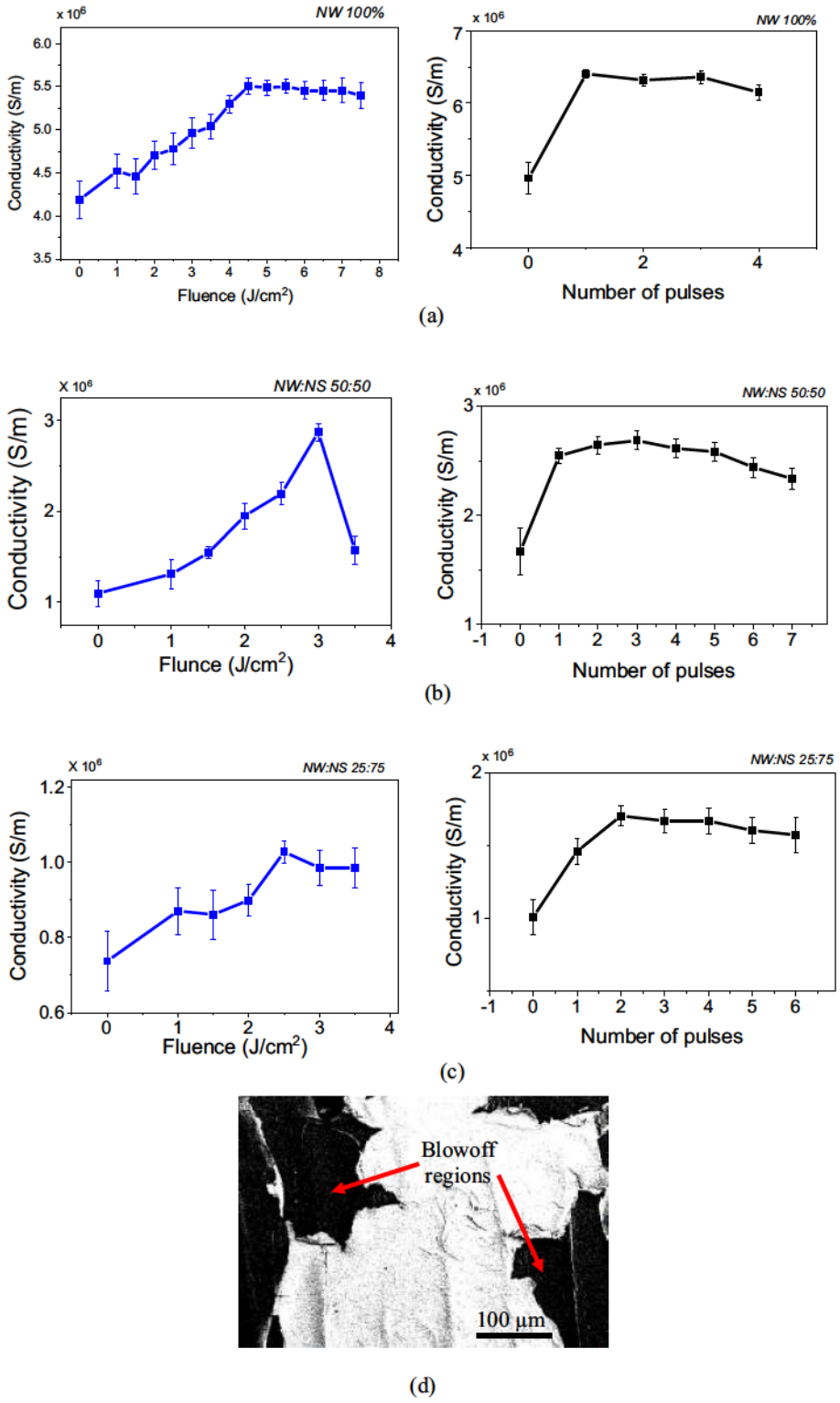

Fig. 7. (a–c) Conductivity for planar circuits with varying fluence and varying pulse number for NW:NS ratios of (a) 100:0, (b) 50:50, (c) 25:75. (d) SEM image of blowoff region of planar circuit for NW:NS ratio of 50:50 and IPL parameters of 3.5 J/cm^2 with one pulse.

plane circuits and FFF of polymer over printed circuits are aspects that cannot be neglected. There is also past work on integration of IPL with FFF or direct ink writing for fabricating surface-conformal circuits. [17,43,45,50,51] Since these works do not explore bulk-embedded structural circuits they cannot reveal how FFF of polymer on printed circuits impacts the planar circuit's conductivity or uncover the effect of IPL on through-plane circuits. Further, these surface-conformal techniques do not use NWs to constitute the circuits.

This paper first examines the effects of the IPL parameters and the nanoparticle shape on the post-sintering conductivity, temperature evolution, and polymer damage for planar circuits. A key novelty is the use of binder-free NWs rather than the typical use of nanospheres or nanoflakes with or without elastomeric binders. In another first we explore the effect of depositing the polymer on the post-IPL planar

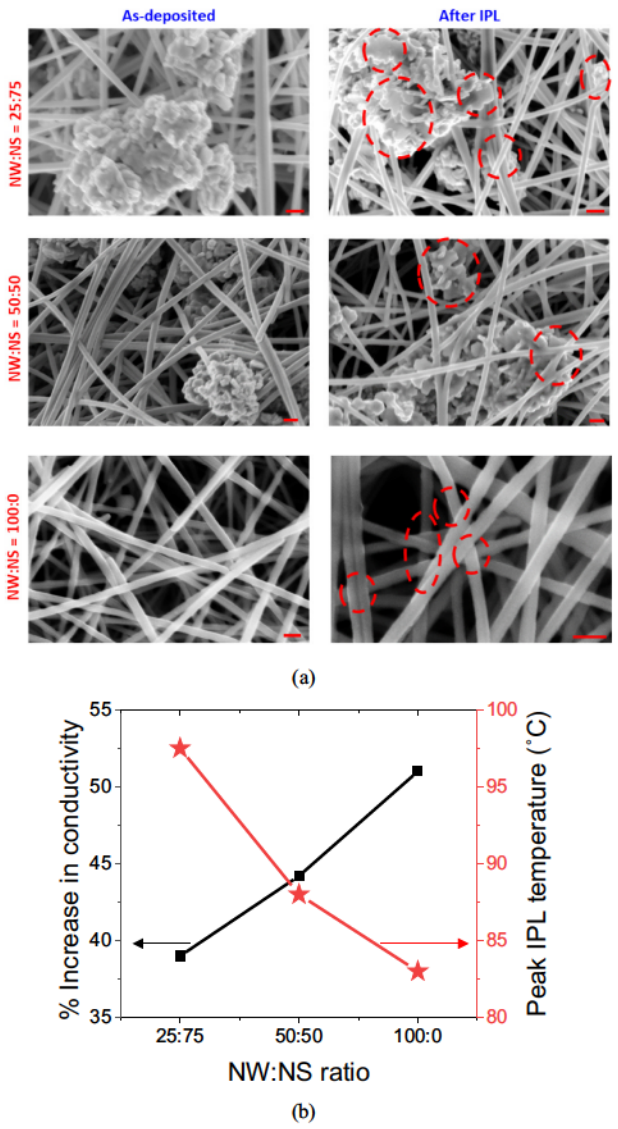

Fig. 8. (a) SEM images of as-deposited and post-IPL NPs. All scales are 200 nm. Red circles show where inter-nanoparticle neck growth is visible. Shown for ABS polymer. (b) IPL-induced change in conductivity and peak temperature for different NW:NS ratios. (For interpretation of the references to color in this figure legend, the reader is referred to the web version of this article.)

circuits, i.e., over-FFF (Fig. 2d), to provide insight into how the FFF process itself might affect conductivity. The effect of key over-FFF parameters on conductivity evolution for planar circuits is characterized. Another novel aspect is the examination of how a through-plane circuit's conductivity is affected by the IPL parameters and by printing of the circuit in multiple layers with intermittent IPL, i.e., the multi-layer IPL strategy. Finite Element Analysis (FEA) of temperature evolution during multi-layer IPL and of electron flow between fused NW ensembles is used to understand our experimental observations. Finally, two exemplar 3D structural electronics are demonstrated, a simple light sensor with hidden planar circuits inside a FFF printed part and a more complex embedded gyroscope integrated with an embedded microcontroller inside a FFF printed part.

2. Methods

2.1. Fabrication of planar circuits

Fig. 3a illustrates the sample configuration used to test FLAME of planar circuits. The samples were created by FFF of the bottom polymer structure with the parameters shown in Table 1, printing and IPL of the nanoparticle circuit on this bottom structure, and FFF of the top polymer structure on part of the post-IPL circuit. The raster angle used for FFF is a typical value used in the literature. The build plate and extrusion temperatures were based specifications from the printer manufacturer and the filament vendor. The nozzle diameter was within the feasible range specified by the filament vendor. The dimensions of the printed part were 63.5 mm × 25.4 mm. The thickness of both the bottom and top structures was 1.5 mm. The length and width of the circuit were 30 mm × 1 mm and its thickness depended on the nanoparticle shape used. ABS and PLA were used as the filament material with a CraftBot Plus FFF printer since the lower thermal tolerance and cost of these materials lets us highlight the wider material window accessible by FLAME. During over-FFF the extruder speed was varied at 30 mm/s and 60 mm/s, the layer height was varied over 250 µm and 350 µm, and a total of 6 layers of polymer were added on top of the post-IPL circuit.

Silver (Ag) was used as the nanoparticle material. The effect of the nanoparticle shape was explored by mixing nanospheres (NSs, 30–50 nm diameter, ACS Material) and NWs (150 µm length, 100 nm diameter, ACS Material) in NW:NS ratios of 0:100, 25:75, 50:50 and 100:0 by weight percentage. The inks were dispersed in ethanol solvent at a constant total solid weight of 0.5 %. A syringe-pump driven nozzle mounted on computer controlled motion stages was used to print the nanoparticles into circuit form. The heating plate used during FFF was also used during nanoparticle deposition for quickly drying the ethanol. IPL was performed using a Sinteron 3000 system (Xenon Corporation) with a 1 ft by 1 in. optical footprint at the sample surface. The supply voltage to the pulsed capacitor of the xenon lamp was kept constant at 3 kV. The optical fluence was varied by changing the on-time of the pulse, an example of which is shown in Table S1 in the Supplementary Information. At least three experiments were performed for any of the parameter combinations used.

2.2. Fabrication of through-plane circuits

Fig. 3b shows the test sample for the through-plane circuit. First, the bottom structure was printed using FFF, then the top structure was FFF printed with two cylindrical holes into which the nanoparticles were deposited to print the through-plane circuits, and then IPL was performed to sinter the deposited NPs. The size of the polymer structure was 25 mm × 25 mm × 1.75 mm. The diameter and height of the cylindrical holes was 3.25 mm and 1.5 mm respectively. FFF, printing of nanoparticle inks, and IPL were performed using the methods described in Section 2.1. Denoting the height of the hole as H, multilayer IPL was performed by depositing the nanoparticles in increments of thickness H, $H/4$, $H/5$, $H/6$ and $H/8$ with IPL performed after printing each such nanoparticle layer (Fig. 4a). This strategy was adopted because the through-plane circuits are much larger in the direction of propagation of IPL light (mm length scale) than the planar circuits (µm length scale). During IPL, this will limit optical and thermal penetration into through-plane circuits. By reducing the effective height of each nanoparticle layer, Multilayer IPL can alter the temperature history of the circuit and thus affect the degree of interparticle sintering and circuit conductivity.

2.3. Characterization

The circuit resistance was measured using a Keithley sourcemeter with copper tape attached to the circuits using silver paste, as in our past work [43]. Scanning Electron Microscopy (Zeiss Sigma Field Emission 8100) was used to characterize the morphology of the planar circuits. Through-plane circuits could not be characterized since it is difficult to access their morphology along their height without damaging them. The circuit temperature during IPL was measured using a thermal camera (MicroEpsilon thermo-imager TIM 200, maximum temperature 1500 °C, accuracy ± 2 %). The resistance evolution during over-FFF was

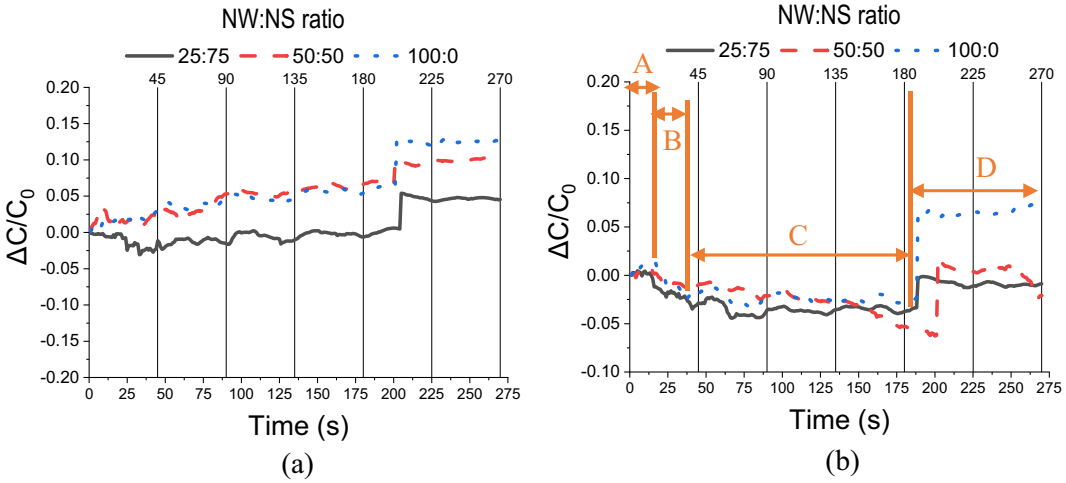

Fig. 9. Representative evolution of conductivity during over-FFF with baseline parameters for (a) as-deposited and (b) post-IPL samples.

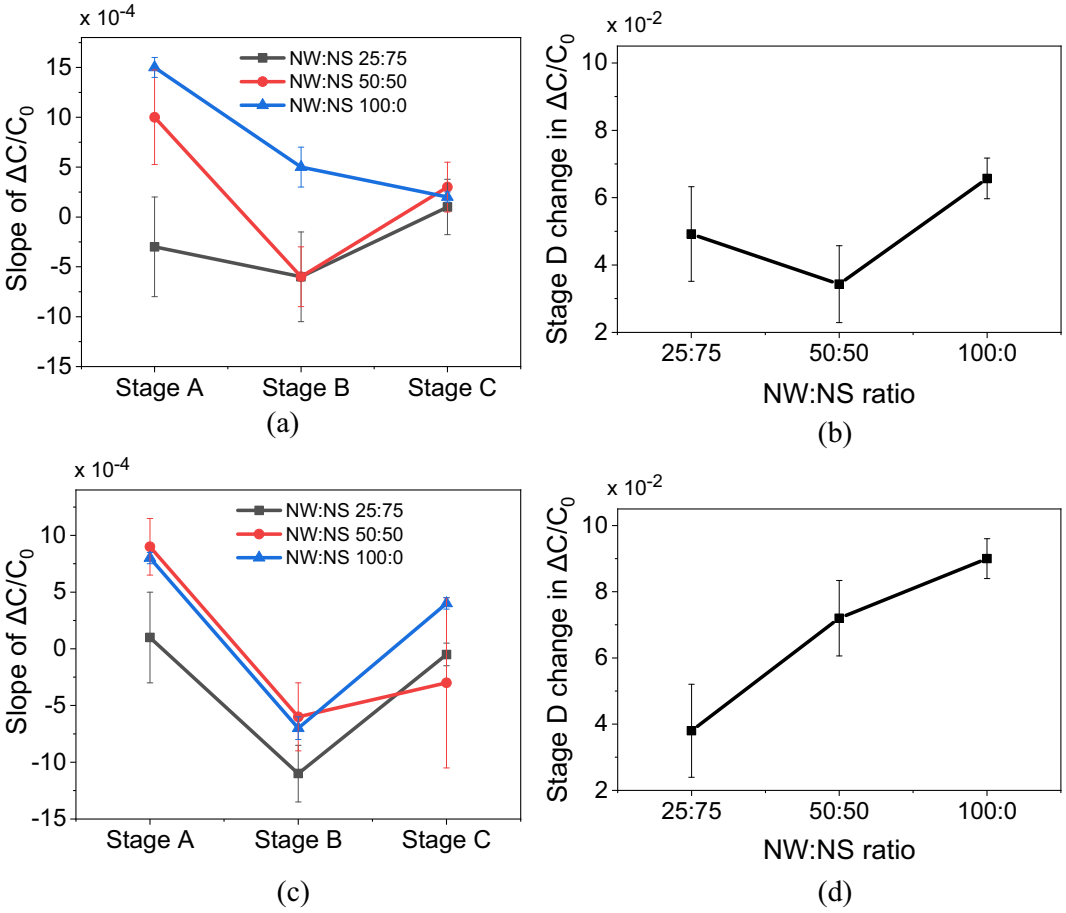

Fig. 10. Stage-specific analysis of $\Delta C/C_0$ during over-FFF with baseline parameters for (a–b) as-deposited and (c–d) sintered cases.

measured using the Kickstart 2.0 software (Tektronix). This line resistance was converted to conductivity based on optical microscopy of the line width and optical profilometry of the line thickness. Fig. 4b shows the measured thickness of the planar circuits as a function of the NW:NS ratio.

2.4. Modeling

Finite element analysis (FEA) was performed to examine the reasons behind the following experimental observations. The first is the difference in the electrical conductivity between planar and through-plane circuits. The second is the effect of multilayer IPL of through-plane circuits on the temperature evolution, since this temperature history largely controls sintering and therefore conductivity. The temperature evolution for planar circuits can be easily predicted using models from past work and is therefore not investigated here [52,53].

Differences in electrical conductivity between through-plane and planar circuits were examined via FEA of electron transfer in NW

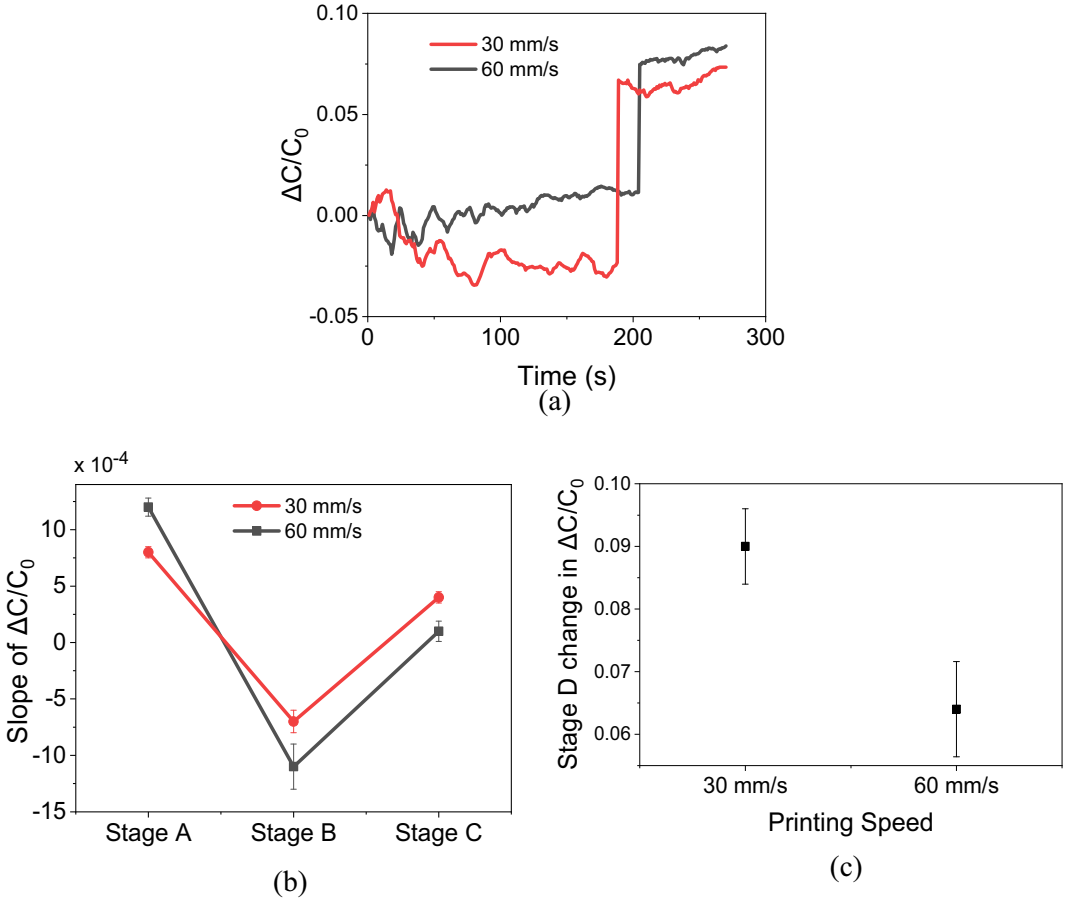

Fig. 11. Effect of printing velocity of over-FFF on (a) conductivity evolution. Stage-specific analysis of (b) stages A–C (c) stage D.

ensembles along the through-plane and in-plane directions respectively, using the COMSOL platform. A multilayer NW ensemble was created with each layer containing 4–5 randomly oriented NWs. The NW length was truncated to 750 nm as compared to the NWs used in experiments in order to avoid edge effects and in order to allow a feasible computational time. For planar conductivity a voltage was applied at the flat ends of the NWs while ground was applied at diametrically opposite flat ends of different NWs (Fig. 5a). For through-plane conductivity a similar specification of the voltage and ground surfaces was performed on the curved surfaces (Fig. 5b). The conductivity was calculated based on the constant voltage applied and the overall dimensions of the NW ensemble. The impact of sintering was examined by introducing an artificial amount of shrinkage X to qualitatively recreate interparticle neck formation (Fig. 5c–d). The value of X was varied across 0.1, 0.2, and 0.3 nm. Since increasing the number of NW layers showed an initial tendency to increase the conductivity therefore the number of NW layers were varied for $X = 0.1$ nm till the conductivity converged as a function of the number of NW layers. This number was found to be 13. At least 5 such NW ensembles were created and analyzed to account for the randomness of the NW orientation in experimental ensembles.

Thermal FEA was performed to predict the IPL-induced temperature evolution of the through-plane circuit (Fig. 5e). The circuit was modeled as a continuum structure of known height embedded as a through-plane pillar inside a hole of known diameter in a block of polymer. The IPL fluence was converted to heat flux at the surface of the polymer, the exposed surface of the through-plane Ag circuit, and the inside surface of the polymer hole not covered with Ag. This flux was calculated based on the spectrum of the xenon lamp and the absorptance of the Ag and the polymer as measured using a UV–Vis spectrophotometer (Jasco V-770), as in our past work [41]. Note that the absorptance of the Ag was based on the deposition of a similar thickness of material on a transparent glass substrate. The thermal properties of the circuit structure were assumed to be the same as that of bulk silver. The initial temperature was fixed at 20 °C. Convection was allowed with a heat transfer coefficient of 2.5 W/m^2-K.

3. Result and discussion

3.1. Planar circuits

3.1.1. Effects of nanoparticle shape and IPL

The use of only nanospheres to constitute the planar circuits yielded low as-printed conductivity of $\approx 10^0$ S/m. The conductivity was not observed to change significantly till a very high IPL fluence of about 20 J/cm^2 was used. But this high an optical energy caused charring of the ABS and significant surface melting of the PLA (Fig. 6). The rest of this work concentrates on NW:NS mixtures where the NW concentration is greater than zero since these ratios enabled more meaningful circuit conductivity without polymer damage.

Past work has shown that the degree of fusion and conductivity during IPL of purely NS ensembles and purely NW ensembles depends on both the pulse fluence and number of pulses [54]. There is also a critical pulse fluence and number of pulses beyond which the conductivity starts to reduce [43,45]. The following approach was used to identify the critical pulse fluence and critical pulse number for a given NW:NS ratio. First, the number of IPL pulses were fixed and the pulse fluence was changed till the above inflection point in the conductivity was observed. At this optimal fluence the number of pulses was increased in increments of one till the inflection point in the conductivity was observed again. This number of pulses was chosen as the optimal number of pulses.

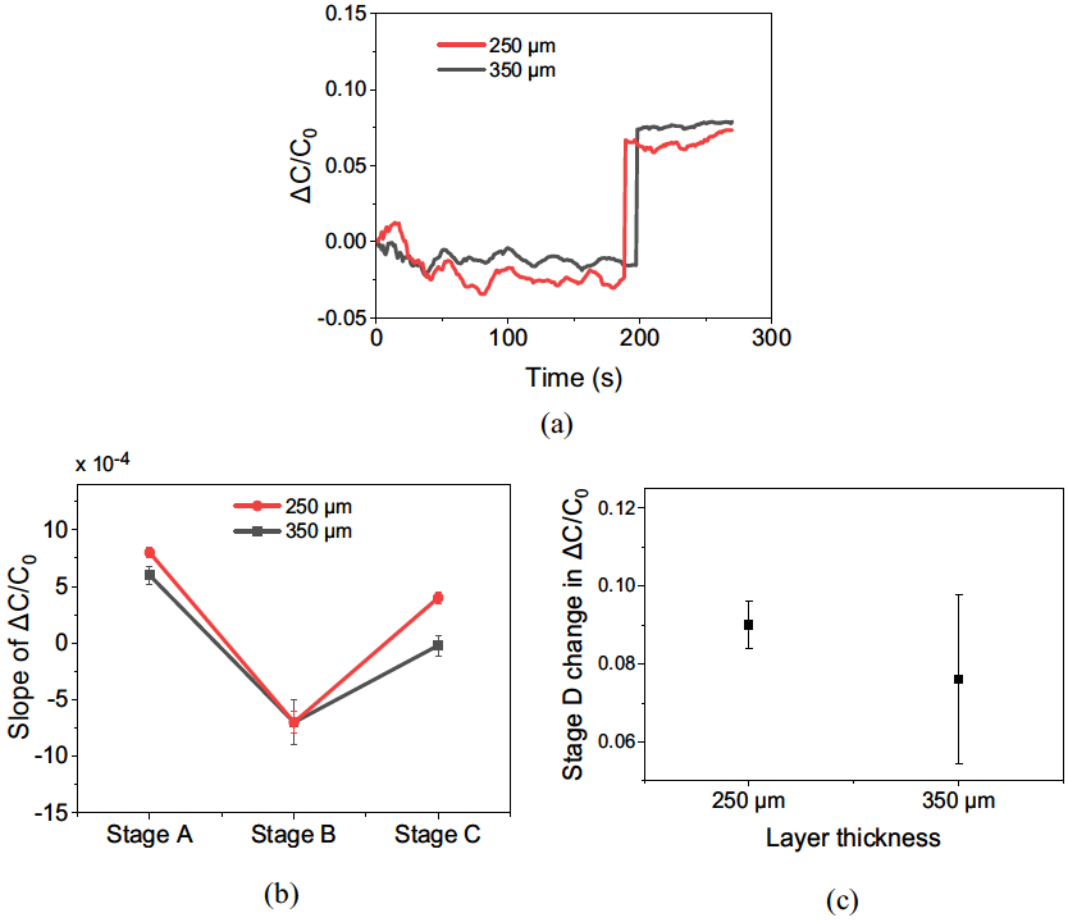

Fig. 12. Effect of layer thickness of over-FFF on (a) conductivity evolution; and stage-specific analysis of (b) stages A–C (c) stage D.

Changes in the fluence and number of pulses did not have an accumulative effect since a new sample was used for each separate pulse fluence and pulse number. Fig. 7a–c show the corresponding conductivity obtained after IPL where the inflection point in the conductivity denotes an optimal pulse fluence or pulse number. The inflection point occurs due to blowoff or evaporation of the nanoparticles when exposed to excessive pulse energy or too many pulses, as seen in the SEM image in Fig. 7d. This reduces the effective cross-sectional area of the circuit so that the apparent change in conductivity is due to a reduction in the circuit's cross-sectional area rather than an intrinsic change in the material's conductivity.

For NW-NS ratios of 25:75, 50:50 and 100:0 the optimal parameters were found to be 3 pulses at 2.5 J/cm^2, 3 pulses at 3 J/cm^2 and one pulse at 4.5 J/cm^2, respectively. The total IPL time for these parameters was 1.3, 1.5 and 0.75 s respectively. This indicates the high speed at which the sintering can be performed. No visible surface damage on ABS or PLA was seen for any of these cases. For planar circuits, the highest conductivity of 7.6 × 10^6 S/m is obtained for a NW:NS ratio of 100:0 with one pulse of 4.5 J/cm^2 fluence that lasts 750 ms.

Fig. 8a shows SEM images of the circuit's nanoscale morphology corresponding to optimal IPL parameters for each NW:NS ratio, and highlights the locations where inter-particle junctions are formed due to IPL-driven fusion. Greater quantitative insight into the effects of the NW:NS ratio are obtained in Fig. 8b, which shows that the peak IPL temperature reduces with greater NW:NS ratio but the change in conductivity relative to the as-printed state increases. Thus, the addition of NWs into a NS ensemble accelerates sintering at lower temperature. This is in line with recent atomistic simulations of NW sintering which show that surface diffusion and dislocation-driven anisotropic neck growth cause greater inter-NW fusion at lower temperatures as compared to inter-NS fusion [52,53,55]. Past work also shows that using NWs instead of NSs reduces optically-induced heating as fusion proceeds during IPL [45,56]. But the IPL-induced heating of NWs is more sustained, i.e., it does not reduce as significantly with the progression of fusion as it does with NSs. As a result the temperature stays lower but more sustained during IPL of NWs, which is known to enhance fusion. [41,57] Greater fusion enhanced conductivity. This is why the replacement of NSs with NWs allows circuit conductivity to increase while reducing thermal damage of the polymer.

3.1.2. *Effect of over-FFF on planar circuits*

Fig. 9a shows the evolution of the planar circuit's electrical conductivity during over-FFF with the baseline parameters, i.e., ABS filament material, layer thickness 250 μm, printing speed 30 mm/s, and 6 layers of the top structure. C_0 is the post-IPL conductivity (in Fig. 9b) or the as-printed conductivity (in Fig. 9a), Cs is the conductivity at any instant during over-FFF, and $\Delta C = C_s - C_0$. The through-plane grid lines correspond to the times at which deposition of the different over-FFF layers (layers 1–6) is completed. The observed non-monotonic evolution of conductivity was qualitatively similar across different values of over-FFF parameters, and is therefore separated into stages A to D (Fig. 9b). Note that resistance measurement was performed to a resolution of 3 decimal points and was started 10 min before the beginning of over-FFF to ensure that the initial measurement was stable. The change in conductivity during this initial measurement was no more than ±0.1 %. Thus, the $\Delta C/C_0$ evolution seen in Fig. 9 is due to deposition of polymer on the post-IPL circuit.

Fig. 9b shows that Stage A, with very little change in conductivity,

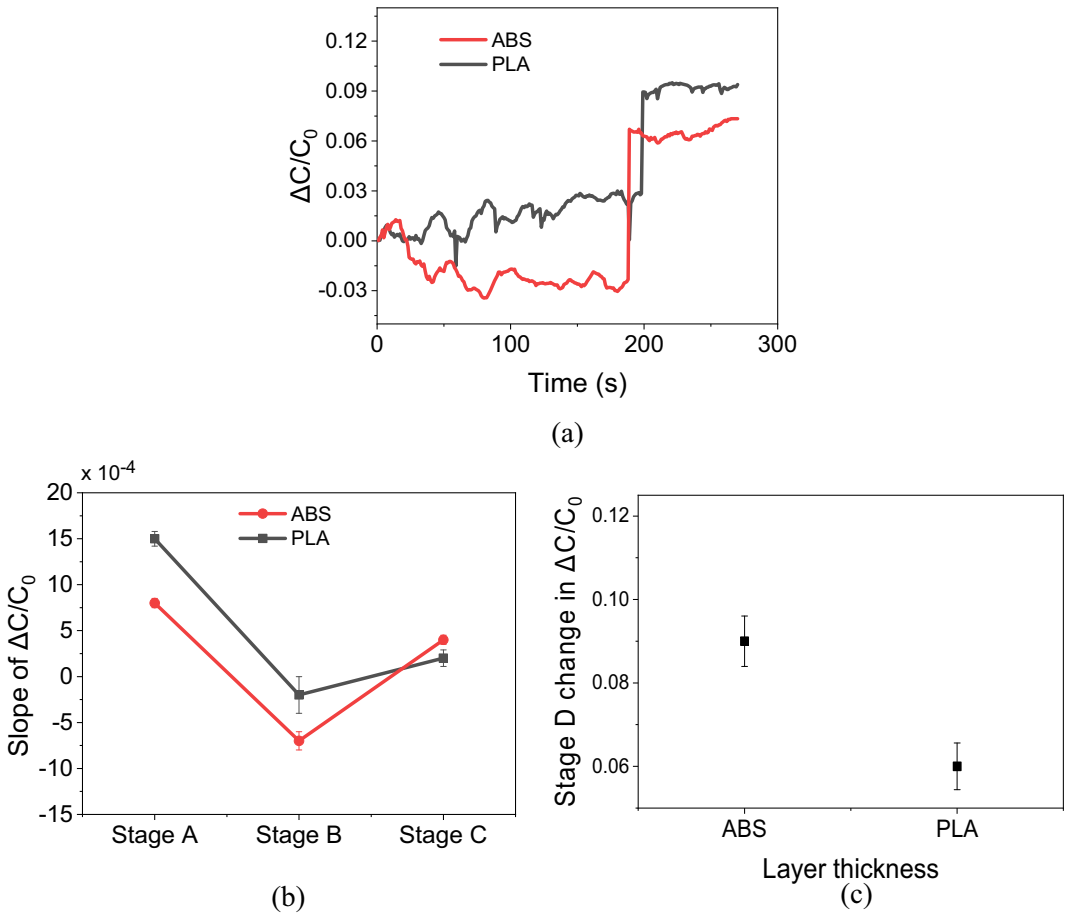

Fig. 13. Effect of filament material during over-FFF on (a) representative example of dynamic conductivity; and stage-specific analysis of (b) stages A–C (c) stage D.

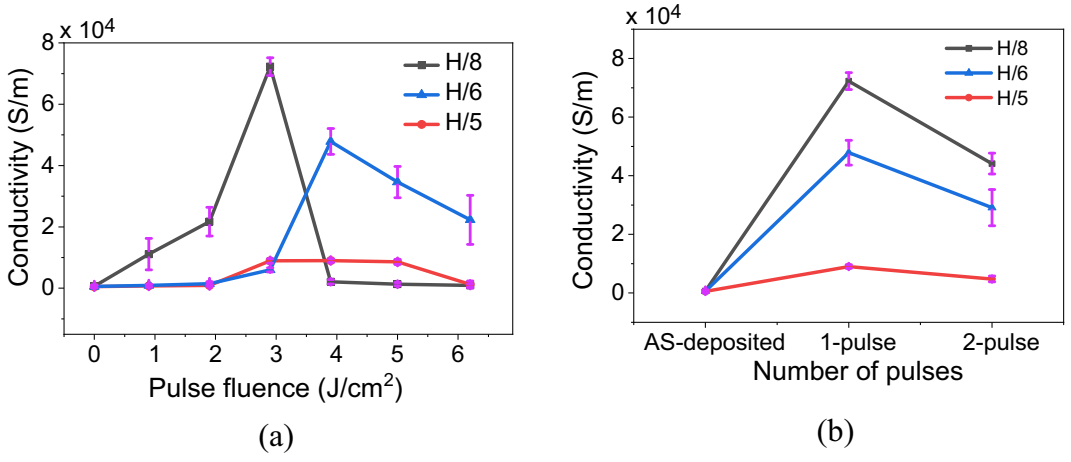

Fig. 14. Effect of (a) Pulse fluence and NW layer height for one IPL pulse (b) number of IPL pulses with the optimal pulse fluence at a given NW layer height.

lasts for about 1/4th of the first layer. This is followed by a reduction in conductivity in stage B which lasts till the end of layer 1. In stage C, the conductivity stays constant or drops slightly depending on the parameters used. In stage D, there is a significant increase in the conductivity even compared to the post-IPL case in some cases (e.g., NW:NS ratio of 100:0). No further change in conductivity was seen after stage D even though over-FFF is performed into the sixth layer. Note that the net change in conductivity in each stage relative to the post-IPL conductivity depends significantly on the NW:NS ratio. For stages A to C, the stage-specific change in conductivity is quantified in terms of the slope of the corresponding $\Delta C/C_0$. Stage D is characterized by the magnitude of change in conductivity since the $\Delta C/C_0$ line is vertical in this stage.

Fig. 10a and c analyze the slopes of stages A–C for the baseline parameters, with and without IPL. The slopes of $\Delta C/C_0$ have a significant dependence on the NW:NS ratio for the as-deposited case but not for the sintered case. For both sintered and unsintered samples there is a slight change in conductivity from stages A–C. But the largest increase is observed in stage D for increasing NW content with sintering (Fig. 10d). In fact, due to the increase in stage D the final conductivity ends up being higher than that before over-FFF. The unsintered cases also show

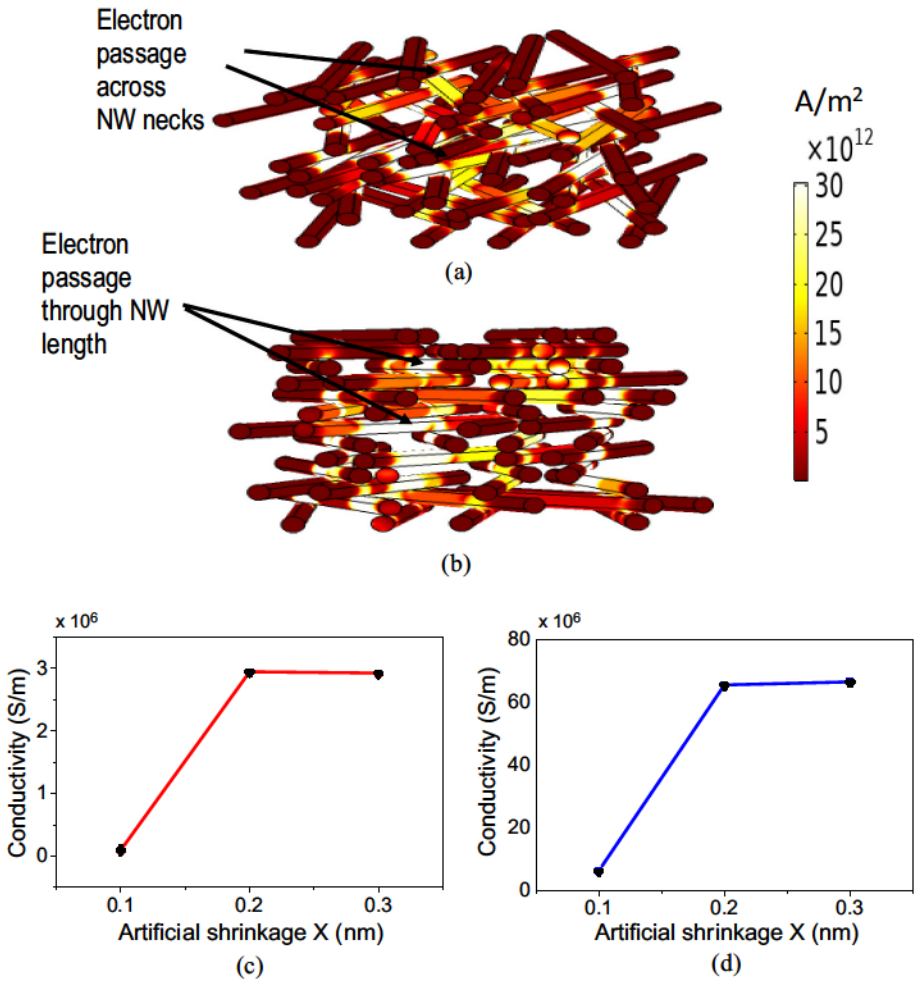

Fig. 15. Current density contours for (a) through-plane conduction and (b) planar conduction corresponding to artificial shrinkage $X = 0.1$ nm. Calculated ensemble conductivity as a function of X for (c) through-plane conduction (d) planar conduction.

increase in conductivity during stage D (Fig. 10b) but the magnitude of increase is relatively lower.

To summarize, over-FFF can yield a further increase in conductivity after IPL. This increase is higher when IPL is used with a higher NW content. The steady-state conductivity of the sintered samples with a NW:NS ratio of 100:0 after over-FFF was 8.3×10^6 S/m, which is 7.5 times lesser than the intrinsic conductivity of bulk silver, 4 times higher than state-of-the-art hybrid printing [58], and 2.4 times higher than the intrinsic conductivity of liquid metal based circuits [59]. But the conductivity is still slightly lower than that achieved by IPL and thermal sintering of planar circuits on planar substrates, e.g., IPL of planar printed NWs can achieve a conductivity of $\approx 20 \times 10^6$ S/m. [16]

Since the conductivity after IPL and after over-FFF was the highest for a NW:NS ratio of 100:0, this ratio was used to further understand how the over-FFF parameters and the filament material affect conductivity evolution during over-FFF. Fig. 11a shows the effects of the printing velocity, an over-FFF parameter that has an inherent effect on the process throughput and temperature history of the part. The total time for over-FFF was kept the same by printing 12 layers of the top structure at a speed of 60 mm/s and 6 layers of the top structure at a speed of 30 mm/s to ensure that the cumulative time-temperature history experienced by the circuit material during over-FFF was similar. All other FFF parameters and the filament material were the fixed at the baseline parameters. The conductivity increases slightly for higher printing velocity in stages A–C but the greatest increase is again seen for stage D. This increase in conductivity is almost 50 % higher when the printing velocity is reduced by 50 %.

Fig. 12 shows the influence of layer thickness, a key FFF parameter that affects both the printing throughput and the part's surface finish and geometric resolution. The other parameters and the material were fixed at the baseline parameters. The layer thickness does not significantly affect the conductivity in stages A to D. Thus, the layer thickness during over-FFF may be varied to satisfy throughput and surface finish/resolution requirements without significantly altering the final conductivity. Fig. 13 compares the conductivity evolution during over-FFF for two materials, PLA and ABS, while all the other parameters are kept constant at the baseline values. In stages A–C, the conductivity increases slightly for PLA as compared to a reduction for ABS, but again the greatest conductivity increase is observed in stage D (Fig. 13c). The stage D increase for ABS is about 50 % higher than that for PLA. The higher extrudate temperature and bed temperature for ABS are the likely cause of this difference. Thus, filament material can influence the final conductivity of planar circuits.

A number of mechanisms might be responsible for the experimentally observed change in conductivity during over-FFF. The first is flow of the just-deposited polymer melt onto the circuit during over-FFF of the first layer. This viscous flow can create stress in the sintered interparticle necks and break them to decrease conductivity. The second mechanism is intrinsic reduction in the material's conductivity due to increase in its temperature during over-FFF. This occurs due to heat transfer to the sintered NPs from the polymer melt or the solidified polymer. Another pathway is thermomechanical stress, created by the

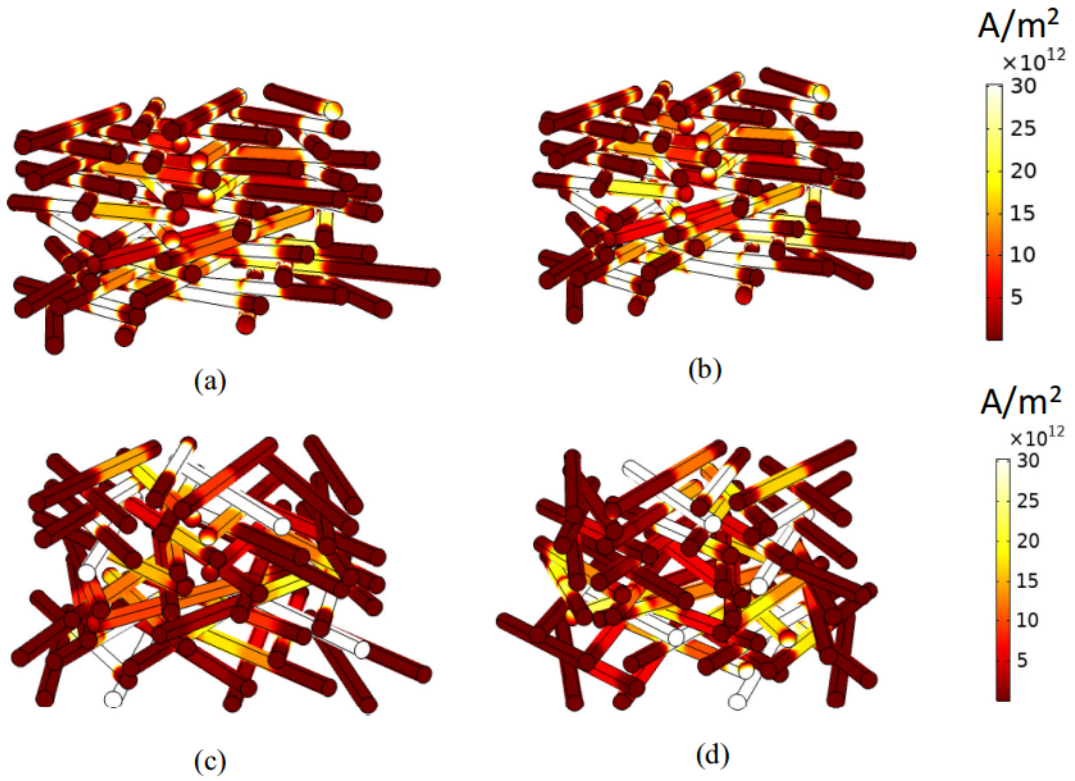

Fig. 16. Current density contours for through-plane conduction with (a) $X = 0.2$ nm (b) $X = 0.3$ nm; for planar conduction with (c) $X = 0.2$ nm (d) $X = 0.3$ nm.

cyclic temperatures and the repeated expansion and contraction cycles that the printed structure adjacent to the post-IPL circuit experiences during printing [60]. Tensile stresses during expansion can break necks between particles and reduce conductivity. Compressive stresses imposed by polymer shrinkage can increase the interparticle neck size via pressure-driven sintering to increase the conductivity. Finally, it is also possible that that long-term temperature history imposed on the circuit by over-FFF causes temperature-induced sintering, which in turn increases the conductivity. However, a quantitative delineation of which specific mechanisms dominate conductivity evolution in over-FFF is not possible at this point and is outside the scope of this work.

3.2. Multilayer IPL of through-plane circuits

3.2.1. Conductivity and process parameters

IPL of through-plane circuits was only investigated for a NW:NS ratio of 100:0 since this composition yields highest conductivity with no thermal damage for planar circuits. The multilayer IPL strategy was used, in which the NWs constituting the through-plane circuits were deposited in layers and IPL was performed after printing of each such NW layer (Fig. 4a). The impact of the NW layer's height was characterized by varying it at H, $H/4$, $H/5$, $H/6$, $H/8$, where H is the depth of the printed hole in which the through-plane circuit is created. Fig. 14a shows that the optimal IPL fluence and the corresponding conductivity depend significantly on the height of the NW layers. Smaller heights of each NW layer yield greater conductivity with lesser fluence. NW layer heights of H and $H/4$ showed orders of magnitude lower conductivity than those shown in Fig. 14 and are therefore not reported here. More than one pulse at the optimal fluence only resulted in a blowoff-induced reduction in conductivity (Fig. 14b). No surface damage was seen for the optimal IPL parameters used for any of these NW layer heights. Therefore the highest conductivity was obtained with a NW layer height of $H/8$, pulse fluence of 3 J/cm^2, and 1 IPL pulse. The corresponding time needed for each intermittent IPL step is 865 μs. The maximum conductivity (7.2×10^4 S/m) is 2.7 times greater than existing hybrid printing which performs damage-free oven sintering using low sintering temperature and long sintering time (2.7×10^4 S/m) [58]. Thus, the advantage of higher conductivity with a wider polymer material range is also translatable to through-plane circuits.

The conductivity of these through-plane circuits is still orders of magnitude lesser than bulk Ag. But Fig. 14b also shows an order of magnitude increase in conductivity when the thickness of the NW layer reduces by ≈1.6 times, i.e., from 300 μm in the $H/5$ case to 187 μm in the $H/8$ case. Commercially available printers can deposit NW networks as thin as the cumulative diameter of 3–4 NWs. This would equate to a NW layer thickness of ≈300–400 nm for the NWs used in this work. Based on the above observed relationship between NW layer thickness and IPL-induced conductivity increase, this order of magnitude reduction in layer thickness could result in much higher conductivity than that observed with a simple lab-made printing nozzle in this paper. Thus, using commercially available printers with greater thickness resolution is a potential pathway to further increasing the conductivity of through-plane circuits. [61–63] The achieved conductivity is not compared to other sintering methods here since these methods have not yet been used for through-plane sintering. However, the use of other sintering methods with NW based through-plane circuits is an interesting area of future work.

3.2.2. Electron transfer in planar and through-plane circuits

Figs. 15 and 16 show representative current density contours for through-plane and planar circuits with the converged number of NW layers (i.e., thirteen) and for different values of artificial shrinkage X. The calculated ensemble conductivity over at least three ensembles, each with random NW orientations, is shown in Fig. 15c–d. At a given X the conductivity for planar circuits is much higher than that for planar circuits. This reflects experimental observations. The underlying reason can be observed from the current density contours. For planar circuits (Fig. 15b) the maximum current density occurs primarily along the length of the NWs. This indicates that more electrons pass through the length of NWs rather than inter-NW necks. Since inter-NW necks act as

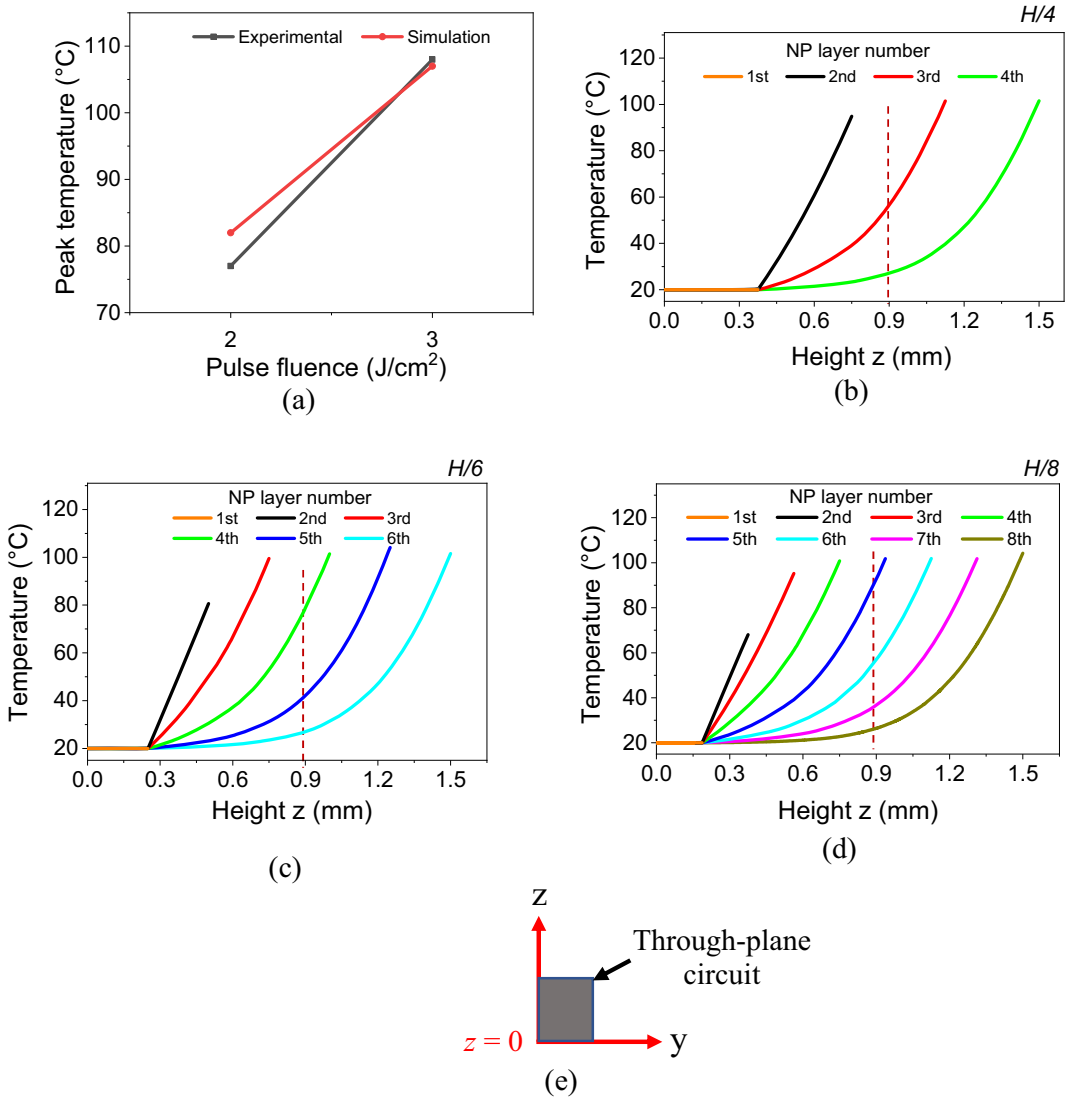

Fig. 17. (a) Comparison of experimental and predicted peak temperature on the top surface of the circuit for a NW layer height of H. Layer-specific temperature along the height z of the through-plane circuit for NW layer heights of (b) $H/4$ (c) $H/6$ (d) $H/8$. (e) Schematic showing direction of height z where x = 1–8. Temperature profile is shown at the point of time when the top surface of the NW layer reaches its maximum temperature.

bottlenecks for electron flow the conductivity is higher. For through-plane circuits there are relatively fewer NWs through the length of which electrons pass (Fig. 15a). Instead the current density is largely concentrated at inter-NW necks since electrons must pass through the height of the NW ensemble. Thus the conductivity of through-plane circuits is higher since electrons must pass through greater number of bottlenecks in the form of inter-NW necks rather than pass through the length of the NW. The conductivity also increases with X, i.e., sintering, but levels off after a certain amount of sintering (Fig. 15c–d).

3.2.3. *Effect of multi-layer IPL*

The peak temperature of the top surface of the circuit predicted by the thermal FEA was validated against experimental measurements for a NW layer height of H (i.e., equal to hole height). Fig. 17a shows that the predictions and experiments agree well with each other with a maximum error of ≈5 %. Fig. 17b–d show the temperature distribution along the height of the circuit at the point of time when the top surface of the latest deposited NW layer reaches its maximum temperature. This spatial temperature distribution is shown for each deposited NW layer and for layer heights of $H/4$ (Fig. 17b), $H/6$ (Fig. 17c), and $H/8$ (Fig. 17d), with the optimal experimentally identified IPL parameters. Fig. 17e shows the height along the z-axis along which the temperature is reported.

Sintering between NWs depends on the temperature history that the ensemble is exposed to. To illustrate the impact of multi-layer IPL and NW layer height on the temperature history Fig. 17b–d examine the temperature at an arbitrary fixed point along the height of the through-plane circuit, i.e., at $z = 0.9$ mm. Lesser layer height exposes this point to higher peak temperature, e.g., ≈60 °C for $H/4$, ≈80 °C for $H/6$, ≈90 °C for $H/8$. This same point also gets exposed to more repetitive temperature rise when smaller NW layer heights are used, i.e., the temperature rises by two times for $H/4$, three times for $H/6$, and four times for $H/8$. This combination of higher peak temperature and more repetitive exposure to an elevated temperature is the reason why a smaller nanoparticle layer height results in greater conductivity for a through-plane circuit. The observed temperature evolution is despite the fact that a smaller NW layer height causes a greater area of the inner polymer surface of the hole to be exposed directly to IPL light, so that the amount of light reaching the NW layer is reduced.

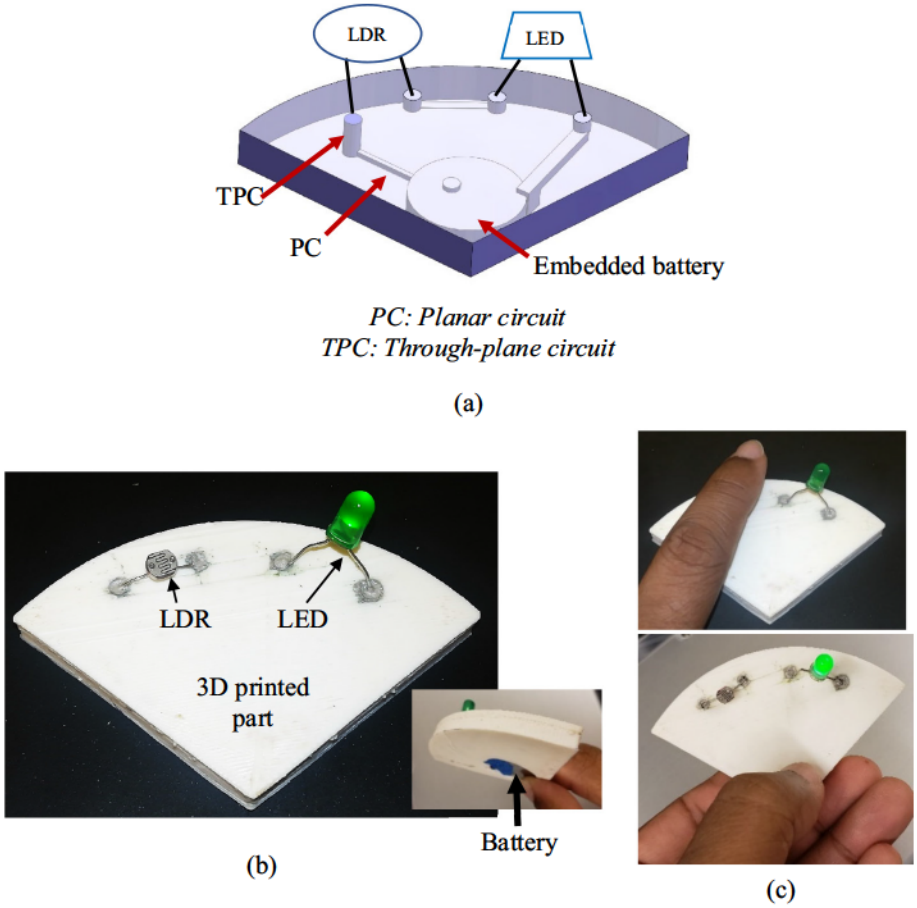

Fig. 18. The LDR-based structural electronics device fabricated with FLAME (a) schematic of different elements of the device (b) fabricated device (c) device operation.

3.3. Exemplar structural electronics

Two examples are used to demonstrate the potential of FLAME to fabricate functional structural electronics consisting of off-the-shelf devices connected by fully 3D circuits inside 3D printed parts. In both cases the height of the through-plane circuits is ≈6–8 mm. The electrical connection between the circuits and off-the-shelf devices was made using a small amount of PELCO high performance silver paste consisting of silver flakes. This paste was applied with a brush at the circuit-pin interface and allowed to dry for 30 min at room temperature so that it became electrically conductive. The first example consists of a 3D circuit with a Light Emitting Diode (LED) and a Light Dependent Resistor (LDR) connected in series with a 3 V battery (Fig. 18a). The LDR (NSL 6112, Digikey) and the LED are mounted externally whereas the battery is embedded inside the 3D printed ABS part (Fig. 18b). The LDR has a resistance of 150–400 Ω when exposed to light and a resistance of 30–50 MΩ in the dark. The light source was a 60-watt incandescent light bulb with 800 lm intensity kept 1 ft away from the fabricated part. Thus, the LED turns on when the LDR is exposed to light but turns off in the dark, acting as a light sensor (Fig. 18c).

The second example consists of an Arduino Nano microcontroller connected to a Bosch BNO055 gyroscope sensor with through-plane and planar circuits (Fig. 19a). The output of this gyroscope-controller circuit is the displacement vector in mutually orthogonal directions relative to the start of measurement. The displacement magnitude is reported for ten arbitrary changes in the part's position in the plane of the table on which the part was kept. These positions are quantified as P1–P10. The ability of the gyroscope to change its output signals for based on a change in part position is sufficient to demonstrate the ability of the FLAME-fabricated 3D circuits to functionally connect the gyroscope and the controller, which is the goal of this demonstration. Since we do not aim not to measure or test the accuracy or vendor-fabricated functionality of the gyroscope, a more involved calibration of the gyroscope's position against an external position measurement system is not performed here. Fig. 19b shows the gyroscope embedded in a printed cavity in the 3D part and Fig. 19c shows the measured magnitude of the displacement vector as this integrated structural electronic device is manually moved around. These examples show how FLAME can expand the geometric or structural functionality of a 3D printed polymer part via off-the-shelf electrical components.

4. Conclusion

This work develops an advanced variant of nanoparticle-based hybrid printing of structural electronics called Flash Light Assisted Manufacturing of 3D structural Electronics (FLAME). The use of NWs, which are 1D in nature as compared to NSs which are 0D nanoparticles, combined with the use of IPL mitigates polymer damage by reducing the peak sintering temperature while concurrently increasing the conductivity. The fact that the sintering time is on the order of a second or two even over a relatively large area of 1 ft × 1 in. allows IPL to be seamlessly integrated with 3D printing and NW printing without a significant increase in the total fabrication time.

For planar circuits, the post-IPL conductivity is 1/8th that of bulk Ag, 3.5 times higher than the maximum conductivity with existing hybrid printing processes, and 2.2 times higher than the conductivity of liquid metal circuits. The conductivity of planar circuits evolves in a complex manner during over-FFF, i.e., during FFF based deposition of polymer on

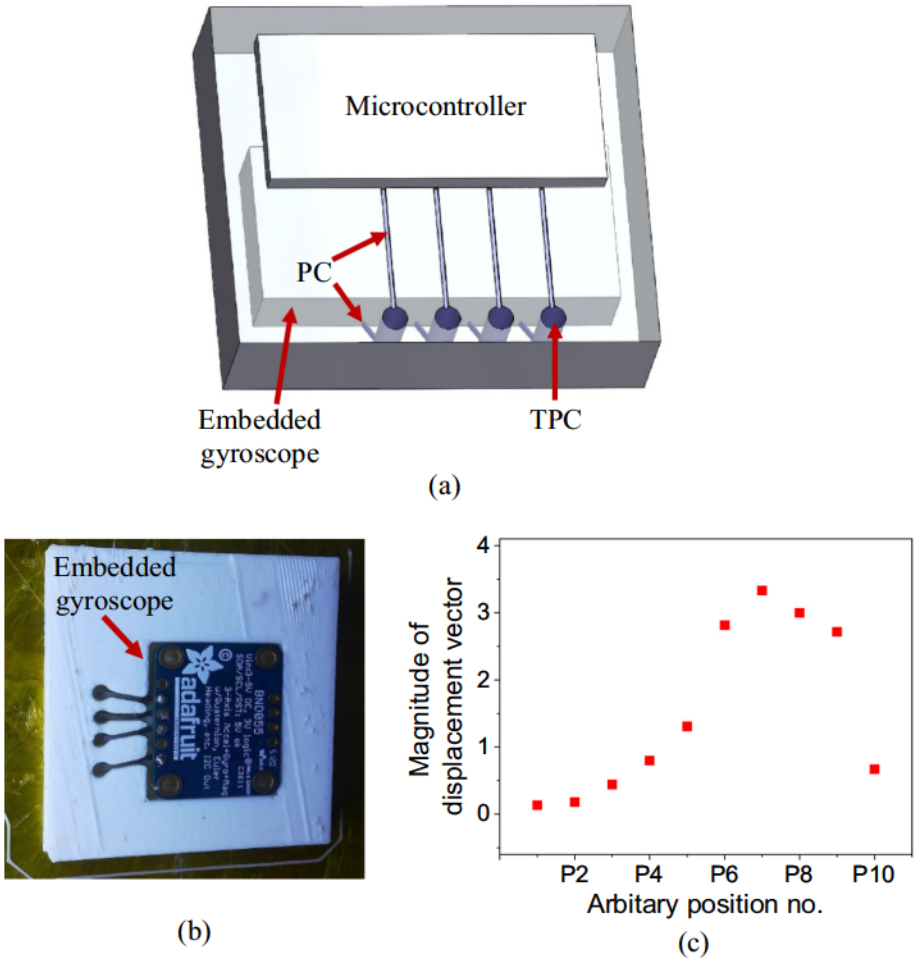

Fig. 19. Demonstration of a gyroscope-based structural electronics device fabricated with FLAME (a) schematic of different elements of the device (b) fabricated device part (c) magnitude of the displacement vector output from the gyroscope during motion of the part.

to post-IPL planar circuits. This evolution depends significantly on the FFF velocity and the polymer material as well as on the NW content and the performance or the omittance of IPL. The conductivity of the circuit after over-FFF increases even above the post-IPL conductivity to within 7.5 times lesser than that of bulk silver.

FLAME also increases the conductivity of through-plane circuits by 2.7 times as compared to state-of-the-art hybrid printing methods. The key to realizing this advance is multi-layer IPL, which allows a given location in the through-plane circuit to be exposed to a greater peak temperature and a more repetitive temperature history. This, in turn, realizes greater sintering and, therefore greater conductivity through the height of a through-plane circuit as compared to IPL with just one NW layer. The electromagnetic simulations show that the conductivity of through-plane circuits is lesser than that of planar circuits since the electrons have to pass through more inter-NW necks in through-plane circuits as compared to planar circuits. While the conductivity of the through-plane circuits is still lesser than bulk Ag, Fig. 14b indicates that further reductions in the NW layer height for multi-layer IPL via the use of higher resolution NW printers may enable much greater increases in conductivity. These findings show the importance of using the appropriate nanoparticle shape, and using multi-layer IPL, for scalably breaking the conductivity-damage-throughput tradeoff in hybrid printing of 3D structural electronics. Further, the device demonstrations show the ability to augment the structural or geometric functionality of a 3D printed part with additional capabilities.

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Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

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