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Process Considerations for selective doping of poly-Si thin films with spin-on dopants and nickel silicide formation for planar thermoelectric devices

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ABSTRACT

The formation of highly doped p-type (boron-doped) and n-type (phosphorus-doped) poly-Si thin films with spin-on dopants on the same wafer poses unique challenges. This work evaluates the pros and cons of different approaches to dopant diffusion, residue removal, and diffusion mask selection when working with spin-on dopants. The experiments have been carried out to optimize the formation of highly doped poly-Si thin films that will form the active layers of a micro-thermoelectric generator (μ-TEG). Building upon previous work on residue removal methods, we report that the residue formation is also dependent on the oxide-silicon surface with a PECVD oxide-Si interface not requiring a post-dopant diffusion nitric acid treatment to achieve a hydrophobic surface. Furthermore, comparing the direct dispense and proximity diffusion methods verifies the existing reports of enhanced diffusion in the latter case. Besides, we observe that doping first with Boron is more conducive than doping first with phosphorus to reduce sheet resistance. We also optimize the contact formation with Ti/Ni thin films and report the mean contact resistivity. Notably, contact annealing precludes the nitric acid treatment requirement even if the surface is hydrophilic after removing dopant residue. Additionally, the sequence of silicidation is observed to be dependent on the doping of the underlying areas.

1. Introduction

Spin-on dopants provide a cost-effective alternative to ion implantation for doping semiconductors, with several dopants available for p-type and n-type doping of common semiconductors like Si [1] and GaAs [2]. Spin-on dopants emerged as an alternative doping method to address channeling tails and transient diffusion challenges during activation annealing while fabricating shallow junctions with ion implantation [1]. The extensive search for methods that do not induce as much crystal damage led to the demonstration of rapid thermal annealing (RTA) driven diffusion from spin-on dopant sources as a convenient way to form highly doped shallow sub-micron junctions in [1,3,4]' primarily since the dopant sources can be formed on the device wafer by a simple spin-coating step. Damage-free junctions can also be obtained via other doping techniques like the growth of doped oxides by chemical vapor deposition (CVD) [5] as dopant sources on device wafers or by having dedicated solid source doping wafers for doping multiple device wafers in diffusion furnaces [6,7]. However, the CVD technique lacks spatial control and involves working with harmful gases such as $POCl_3$ and BBr_3 while the diffusion furnaces drive up the thermal budget. In addition to providing a method to form damage-free junctions at a low thermal budget, spin-on dopants are also cost-effective and require inexpensive equipment. Although ion implantation has been a reliable workhorse for the semiconductor industry, given it offers control over several parameters such as dose, depth, and spatial profile [8], it is a costly process with tools that are often not viable investments for smaller companies and university-based research facilities. Thus, a low thermal budget RTA-based spin-on dopant process provides a valuable option for small-scale facilities and reduced cost prototyping. Spin-on dopants have also been studied for Boron doped emitter formation in n-Si solar cells [9,10], minimal fab applications [4], and demonstrations of doping on 150 nm wide Si channels [11].

This work focuses on selectively doping poly-Si thin films by spin-on dopants and forming good-quality ohmic contacts. We compare different dopant diffusion masks, and dopant diffusion schemes, and comment on the importance of spin-on dopant residue removal methods. The dopant

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diffusion mask options are based on spin-on-glass and PECVD oxide. In this work, we are interested in forming highly doped 2 μm thick poly-Si thin films, which will form the active layer of a micro-thermoelectric generator (μ-TEG). Among CMOS compatible materials, poly-Si thin films have been widely investigated for thermoelectric applications [13,14] with a few works reporting micro-thermoelectric generators (μ-TEGS), which are compact TEGs designed for harvesting ambient thermal energy to power wireless sensor nodes. In MEMS-based efforts [15,16], poly-Si thin films have been doped during Low pressure chemical vapor deposition(LPCVD) growth, while in CMOS compatible studies [17], ion implantation is utilized. The formation of doped poly-Si thermoelectric legs, low contact resistance, and thermally stable contacts are crucial to fabricating active thermoelectric elements. Aided by enhanced dopant diffusion along grain boundaries [18], deeper junctions have been reported for numerous poly-Si thin film growth conditions compared to single crystal silicon. Hence, although spin-on dopants are designed for use in both diffusion furnaces and RTA systems, the need for maintaining the desired dopant distribution during successive rounds of dopant diffusion led us to explore rapid thermal annealing, which offers the advantage of a reduced thermal budget. The formation of closely packed p-type and n-type thermoelectric legs via selective doping also requires a suitable diffusion mask, an effective residue removal method, and a contact formation scheme compatible with the needs of the final application. Since parasitic contact resistance can deteriorate TEG performance [12], and the latter stage device processing steps involve wafer bonding, we also investigate the formation of thermally stable Ti/Ni and Ni contacts with a specific contact resistance low enough for our intended application.

We discuss the fabrication process before presenting the effectiveness of residue removal treatment for samples with different diffusion masks. Next, proximity diffusion is compared with direct dispense, and finally, we analyze the optimization process for forming low resistance contacts based on nickel silicide.

2. Methods

Processing commenced with the deposition of 2 μm thick polysilicon thin films on 100 mm wafers comprised of a 2 μm thick wet thermal oxide grown on a <100> p-type Si substrate. The poly-Si thin films were deposited at 580 °C by LPCVD in a horizontal vacuum furnace at an external vendor's facility. The films were undoped, and the growth rate was 44 Å/min. After receiving the wafers, 11 mm × 11 mm pieces were diced from the wafer, piranha cleaned, and processed individually. Diffusion masks were formed on the samples in 3 different ways. Mask1 (M1) is comprised of a 2-layer stack of spin-on-glass. Here, the samples were cleaned with solvent, dehydrated by baking for 5min at 115 °C, and coated with spin-on-glass. The 700B spin-on-glass (SoG) solution from Filmtronics was used, and it was spun at 2000 rpm for 20 s with no spin-out time as suggested in the datasheet. Then, a soft bake at 200 °C for 10 min solidified the SoG polymer. Next, the second layer was spun, followed by a 20min soft bake at 200 °C. Finally, a further 60-min bake at 400 °C was required to improve polymer cross-linking, resulting in an oxide layer with a refractive index of 1.43, comparable to that of a thermal oxide film. On samples with Mask2 (M2), an oxide layer was deposited in a PECVD system at 300 °C, followed by a dual spin-on-glass (SoG) dispense that yielded a 1.3 μm thick mask compared to the 650 nm thick dual SoG only mask (M1). Mask 3 (M3) consisted of the PECVD oxide + dual SoG stack further annealed at 900 °C. Fig. 1 presents the main steps of the fabrication procedure for the device samples.

We patterned windows into the diffusion masks by direct lithography on a Heidelberg up-101 system followed by etching in Buffered Oxide Etch (BOE) solution to enable selective doping. Preparation for proximity diffusion doping involved spin coating (2000 rpm, 400 rpm/s, 20 s) a Si test wafer with spin-on dopant and baking at 200 °C for 20min. The spin-on dopants B155 and P509 manufactured by Filmtronics were coated for Boron and Phosphorus doping, respectively. The test pieces

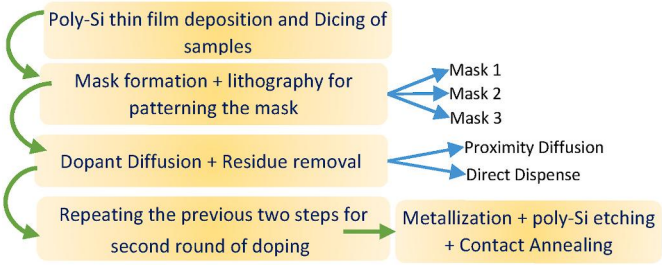

Fig. 1. Fabrication steps for device samples.

were loaded into a Heatpulse 610 RTA on a carrier wafer, and the dopant-coated wafer was suspended upside down over the pieces with the help of supportive pieces at the edges (Fig. 2). After covering the entire setup with a 6″ cover wafer to protect the tool from dopant outgassing, a controlled ambient of 75% N_2 and 25% O_2 was established, and the pieces were annealed at 1075 °C for 1 min. Four such rapid thermal diffusions (RTD) annealing cycles were completed in succession.

For pieces doped via the direct dispense method, the preparation of a carrier wafer was not required. Instead, the dopant was spun individually onto each sample before loading them into the RTA furnace with an unprocessed cover wafer suspended above the samples. After the dopant diffusion anneal, samples were submerged in BOE for 30min to remove the doping residue. The doped areas were visible on the poly-Si thin film at this stage. As discussed later, an additional dopant residue removal step was added in some cases, and it involved heating the samples in 65% nitric acid at 75 °C for 30 min–45 min.

Fabrication of the oppositely doped regions was similarly completed by repeating all the steps starting with diffusion mask fabrication. After completing both rounds of doping, a metallization pattern was defined with bi-layer lithography with LOR5A and SPR220 resists. Metal interconnects were deposited by e-beam evaporation of Ti and Ni. Lift-off of metal contacts involved leaving the samples for a few hours in NMP (N-methyl 2-pyrrolidone). Metal contacts were inspected visually to identify any regions with poor adhesion before the pieces were prepared for poly-Si dry etching. The dry etching was carried out in Oxford RIE with a plasma consisting of SF_6, O_2, and CHF_3 gases. The dry etch removed a large proportion of the un-doped poly-Si areas (Fig. 3). The etch mask was composed of a hard-baked S1813 photoresist. The pieces were now ready for contact annealing and I–V measurements.

Contact annealing was done in an AnnealSys RTP system, and the I–V data was collected on a probe station equipped with a Keithley 4200SCS system. Wet etching in BOE and HF for up to 2 h was ineffective in residue removal. Fig. 3 depicts the sample cross-section after the RIE step. Contact resistivity was calculated with Transmission Line Measurements (TLM) on a series of rectangular contact pads with distances varying from 25 μm to 175 μm. On each 11 mm × 11 mm sample, TLM structures in 4 different locations were probed. After linearly fitting the resistance vs. distance data, the y-intercept was interpreted as twice the contact resistance (R_C) & the x-intercept is considered as 2 x (transfer length, L_T). From these values, the contact resistivity is calculated [19]

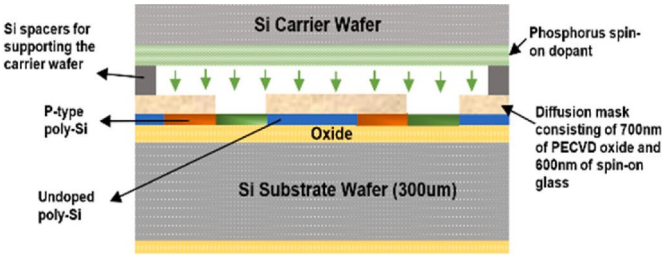

Fig. 2. Proximity diffusion step with carrier and device wafers.

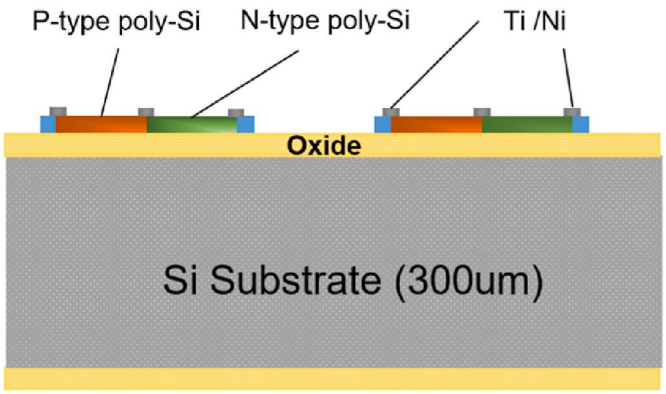

Fig. 3. Cross-section of the samples after metallization and poly-Si dry etching.

as Rc*Lt*W, where W is the width of the contact. (100 μm). In addition to the TLM test structures, the samples contained sets of p-type and n-type regions metalized to form thermoelectric legs, as shown in Fig. 4. X-ray diffraction measurements were taken on a Rigaku Miniflex600 system with Cu-Kα incident radiation.

3. Results and discussion

3.1. Post-annealing residue removal

In both direct dispense and proximity diffusion, the Rapid thermal diffusion (RTD) anneal leaves behind a residue on the sample surface [2,3]. Post-diffusion, the masked areas on the samples consist of both spin-on dopant (SOD) & diffusion masks, whereas the unmasked areas are only coated with the spin-on dopant residue.

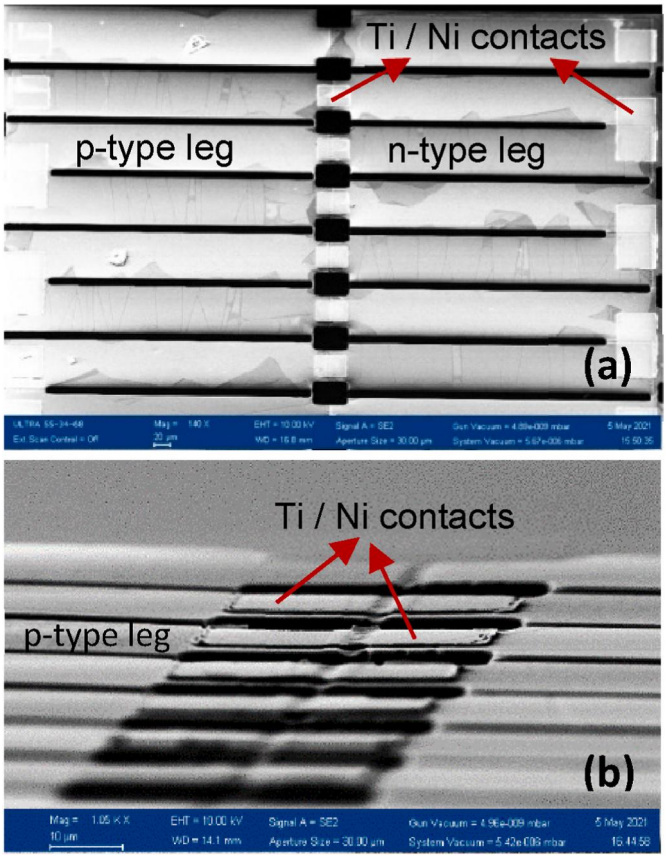

Fig. 4. (a) SEM top view at 140X magnification of the typical sample after the metallization and poly-Si etching steps. (b) SEM image presenting lateral view.

Deglazing this residue from the samples is a critical step affecting the device surface quality. Although most of the doping residue etches away in Buffered Oxide Etch (BOE), it has been reported that working with boron spin-on dopants such as B155 can result in the formation of an HF-insoluble residual layer [10,19]. This boron-rich B–Si residual layer (BRL) [19,20] can lead to the spatial variation of contact resistances and open contacts. Since our process relies on successive doping cycles, BRL could interfere with the second round of dopant diffusion. A hydrophilic surface and a reddish-brown residue are two indicators of incomplete dopant residue removal [4,10,19]. Initial runs under nitrogen ambient yielded hydrophilic surfaces on both masked and unmasked areas. Wet etching in BOE and HF for up to 2 h was ineffective in residue removal. Several groups have reported oxidation of the BRL by either boiling in nitric acid [10,19] or in-situ oxidation at a low temperature [4] during the furnace anneal. BOE can attack BRL once BRL is oxidized.

Hence, we attempted hot nitric acid treatment, which involved immersing the samples in a 65% nitric acid solution heated to 75 °C for 30–40 min. A 15min BOE soak followed this. Table 1 shows the different surface behaviors observed after the initial post-diffusion BOE soak & after residue removal treatment, depending on the diffusion mask, annealing ambient, and dopant. Apart from sample 1, all other samples were annealed in an oxidizing ambient of 75% N_2 and 25% O_2. Samples 4 and 5 did not undergo nitric acid treatment. Under an N_2 environment (Sample 1), both the masked and unmasked (doping windows) areas displayed hydrophilic behavior after the initial soak in BOE. An oxidizing ambient ensured hydrophobic surfaces over unmasked areas, but we still observed hydrophilic surfaces in the masked areas on samples 2 and 3. In the case of samples 4 and 5, where the PECVD oxide was grown on the poly-Si surface before dual SoG layers were coated, hydrophobic surfaces were visible over the entire sample after the post-RTD BOE soak itself. Fig. 5 illustrates the differences between the hydrophilic and hydrophobic surfaces seen on the samples.

Based on Table 1, we saw post-drive-in anneal hydrophilic surface behavior in samples where the SOG film is in contact with the poly-Si surface (samples 1, 2 & 3). Interestingly, these hydrophilic surfaces are seen after residue removal following both boron and phosphorus doping cycles, irrespective of the chosen sequence of doping & the annealing ambient. This contrasts with the largely BRL-centric discussion in the existing literature. Possible outdiffusion of Boron from previously doped but currently masked areas during the second round of doping(with P) might have led to BRL formation but this does not explain the sample 3's observation in Table 1 since only 1 round of doping has been carried out. Under oxidizing ambient, the hydrophilic surfaces are only visible over areas masked with dual-SOG layers & it is intriguing to note that nitric acid treatment + BOE soak converts these areas into hydrophobic surfaces. The diffusion of both B and P SODs through the dual-SOG layers during the long 4 min RTD seemingly generates a surface with characteristics like the widely reported BRL. Samples 4 and 5 from Table 1 show that switching to a PECVD + dual SOG mask can eliminate the need for nitric acid treatment if proximity diffusion is employed, as further discussed in the next section. The samples in Table 1 were 11 mm × 11 mm in dimensions, so a 15-min nitric acid etch was effective. But another complication was seen in the case of a 4″ wafer. Table 2 tracks the step sizes with surface treatments on a 4″ wafer doped with B155 followed by P509. After the B155 residue removal, a 30-min nitric acid treatment is sufficient to obtain a hydrophobic surface.

However, multiple rounds of nitric acid treatment are needed to observe a similar surface after the P509 doping. Consequently, the extensive BOE soak time from multiple residue removal methods increases the step size to more than 150 nm (Table 2). Due to a difference in BOE etch rates on p-type and n-type poly-Si [20], long soaks in BOE can lead to step sizes greater than 150 nm, which are detrimental to lift-off during metallization & can add to the interconnect resistances. In samples where hydrophilic surfaces are obtained and nitric acid

Table 1
Surface behavior post-residue removal with different masked samples.

Sr No	Diffusion Mask	Densification Bake	Spin-on Dopant	Surface after 45min in BOE		Surface after HNO_3 treatment +15min in BOE	
				– Masked areas	Unmasked areas	Masked Areas	Unmasked areas
1	M1	400 °C, 1hr	B155 (annealed in N_2)	HPL	HPL	HPB	HPB
2	M1	400 °C, 1hr	B155 (annealed in N_2 & O_2)	HPL	HPB	HPB	HPB
3	M1	400 °C, 1hr	P509 (annealed in N2 & O_2)	HPL	HPB	HPB	HPB
4	M3	900 °C, 30min	B155 (annealed in N2 & O_2)	HPB	HPB	–	–
5	M3	900 °C, 30min	P509 (annealed in N2 & O_2)	HPB	HPB	–	–

***HPL – Hydrophilic *HPB – Hydrophobic M1:** Dual SoG layers(650 nm) **M2:** Dual SoG + PECVD Oxide (1.3 μm) baked at 400 °C for 60min **M3:** Dual SoG + PECVD Oxide (1.3 μm) annealed at 900 °C for 30min.

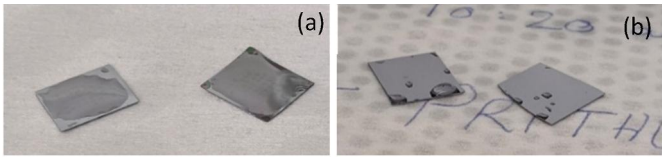

Fig. 5. (a) Samples with a hydrophilic surface. (b) The hydrophobic surface on samples.

Table 2
Evolution of step sizes (n-type to p-type) with residue removal methods following the final dopant (P509) diffusion. Step size was measured by the Dektak Stylus profilometer.

Device	BOE (40min)	Nitric Acid Treatment	
		Round 1 (45min) + 30min BOE	Round 2 (70min) + 12min BOE
A1	110 nm	130 nm	170 nm
B3	134 nm	167 nm	180 nm
C5	142 nm	166 nm	185 nm
D7	91 nm	136 nm	150 nm

treatment is required, the total BOE soak time must be balanced by more prolonged oxidation in nitric acid to preserve a flat surface topology suitable for contact deposition.

The impact of the dopant diffusion mask on surface morphology is also seen in data from optical profilometry measurements. Fig. 6 indicates the presence of streak-like residue on the doped areas of the samples where a dual SoG layer mask (M1) was deployed. M1 consists of 2 layers of spin-on glass (SoG) applied as stated in the methods section. These streaks were found to be insoluble in BOE. On the other hand, such streaks are not visible on the surface with masks M2 and M3 where the SoG layer is never in contact with the poly-Si surface since the dual-layer SoG is applied after deposition of a 700 nm thick PECVD oxide layer. The surface roughness of the areas excluding the streaks was approximately 3.5 nm (Table 3), irrespective of the diffusion mask deposited during fabrication. The inset of Fig. 6(a) shows the profile of a single streak with a step height close to 60 nm.

3.2. Comparison of RTA dopant diffusion methods

Dopant diffusion can be driven by furnace annealing (FA) or Rapid thermal diffusion (RTD). In early studies involving spin-on dopants, the large thermal budget of FA and the requirements for sub-micron junctions drove the efforts to study RTD. Although we do not require sub-micron junctions, we have opted for RTD to reduce the thermal budget enabling successive high concentration doping steps without excessive lateral diffusion. Diffusion processes can be further distinguished based on the SOD application method.

We have tested both direct dispense and proximity diffusion. We have resorted to the proximity diffusion method for most of our samples,

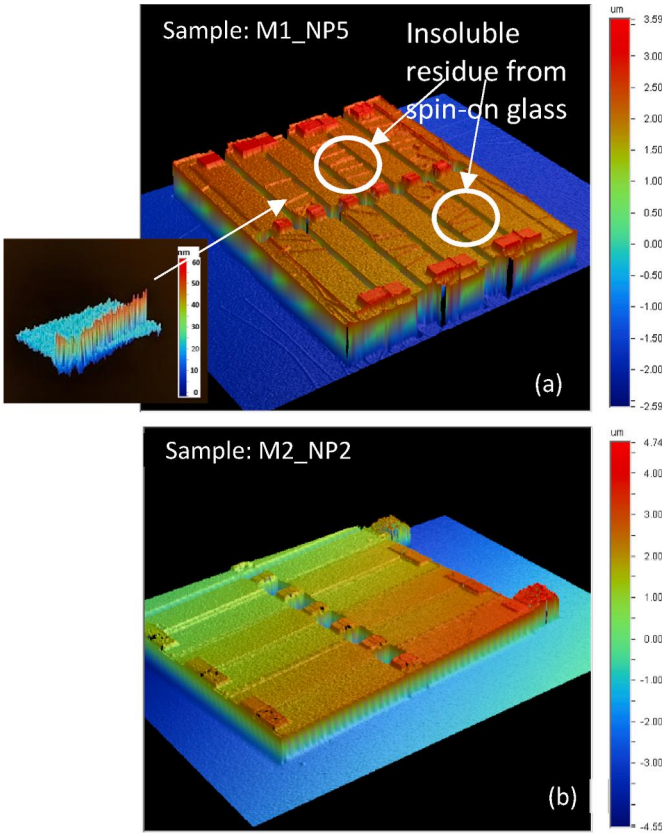

Fig. 6. Surface profiles of device samples after metallization and the final poly-Si etch step. (a) Sample where a dual SoG layer was in contact with poly-Si. Inset shows that the height of the streaks is ~60 nm(b) Sample where mask M2 acted as the diffusion mask.

Table 3
Roughness measurements on areas without streaks on samples processed with diffusion masks M1, M2, and M3, respectively. (Mask described in the Methods section).

Sample	Mask	p-type area roughness	n-type area roughness
M1_NP5	M1	5.07 nm	3.44 nm
M2_NP2	M2	4.78 nm	3.65 nm
M3_NP2	M3	3.84 nm	3.92 nm

where a carrier wafer coated with a spin-on dopant (SOD) is suspended over the samples. In proximity diffusion, the SOD layer thickness and low-temperature bake times are critical parameters [1]. The direct dispense [21] method involves spinning the SOD directly on the device wafer or samples before proceeding to the low-temperature bake and drive-in anneal. Table 4 compares the sheet resistances measured on the

Table 4
Comparison of resulting sheet resistance from different dopant diffusion approaches (B155: Boron spin-on dopant, P509: Phosphorus spin-on dopant, data measured with 4-point probe method).

Sr No	Doping Method	Spin-on Dopant	Sheet resistance
1	Direct dispense	B155	7.32 Ω/sq
2	Proximity diffusion	B155	5.10 Ω/sq
3	Direct dispense	P509	5.63 Ω/sq
4	Proximity diffusion	P509	3.35 Ω/sq

different samples with the data showing that proximity diffusion in an oxidizing ambient leads to lower sheet resistivities. Wosik et al. [1] explained that the dopants outgas from the SOD layer as gaseous oxides that get adsorbed on the Si surface, reduce to dopants (B or P) and form a doped SiO_2 film, which acts as the dopant source. The oxidizing ambient facilitates the formation of SiO_2. In direct dispense, the restricted availability of Oxygen at the Si-SOD interface hinders the formation of a doped oxide layer. As discussed in [22], a constant source-driven diffusion results in higher sheet resistivities than an infinite source-driven diffusion. Proximity diffusion cannot be categorized as an infinite source, but the continuous diffusion of dopant atoms from the carrier wafer and oxide formation on the device wafer surface is likely to provide a higher surface dopant concentration than the direct dispense method. The results in Table 3 are measured from samples that have undergone four cycles of 1 min anneals at 1050 °C.

Another significant advantage of proximity diffusion we observed was the absence of reddish-brown residue seen during direct dispense doping with B155 SOD. This reddish-brown residue could be oxidized with hot nitric acid treatment to turn it BOE soluble, as illustrated in Fig. 7.

The higher diffusion constants in poly-Si [18], due to a higher concentration of dopant atoms diffusing through the grain boundaries and the greater activation of dopants, aid in forming deeper junctions relative to single-crystal Si. Upon measuring I–V across the sets of 7 legs in Fig. 4, we observed lower resistance across sets of legs with well-defined current paths due to poly-Si etching compared with sets without any poly-Si etching between adjacent legs. This suggests the presence of lateral leakage currents across multiple p-type and n-type regions despite masked areas between them. Hence, the four cycles of annealing that we used were insufficient to produce a doping level that was high enough to form isolating p-n junctions throughout the 2 μm depth, leaving current paths through the undoped poly-Si.

3.3. Ohmic contact formation

The electrical properties of Ti (25 nm)/Ni(300 nm) & Ni contacts to the doped poly-Si films were probed by Transmission Line Measurements (TLM) as discussed in the methods section. Initial data on samples that had not undergone contact annealing often showed non-ohmic I–V curves or had considerable resistance between the TLM pads, or had anomalies in resistance data. To investigate the possibility of contact resistance degradation on samples with hydrophilic surfaces, we compare them with samples that have undergone nitric acid residue removal treatment. The primary process parameters such as diffusion mask, residue removal treatment, metal interconnects, and contact annealing details for the discussed samples are summarized in Table 5. For the same set of samples, the contact resistance and sheet resistance values extracted from the TLM data are presented in Table 6 and Table 7.

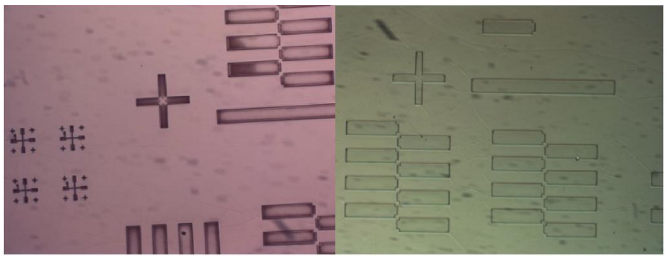

Fig. 7. (Left) Reddish-brown BOE insoluble dopant residue visible on the poly-Si surface after B doping via direct dispense. (Right) A clear surface was observed after a 30min hot HNO_3 treatment followed by a 15 min BOE soak.

Fig. 8 presents the TLM data for n-type regions on M1-NP5, a sample that underwent nitric acid treatment. The large and unevenly distributed resistance values measured after annealing at 450 °C are found to decrease after annealing at 700 °C in Nitrogen (N_2) for 45 s. Finally, Fig. 8 shows the lowest values after further annealing at 700 °C in N_2 for 105 s. At high temperature anneals in this sample and others, we observed a change in appearance and texture, as shown in Fig. 9. Based on the observations reported in [23,25], we can conclude that silicidation of Ni has taken place.

Fig. 9 illustrates the visual difference between the Ti/Ni contacts without NiSi formation and those after silicidation at higher temperatures. Additionally, during multi-step anneals to ensure complete Ni silicidation, we noticed that the agglomeration accompanying the silicidation was first seen on undoped areas, followed by p-type areas and finally n-type areas. This dopant dependence of the sequence of silicidation adds to the report of dopant dependence of the sheet resistance and cross-sectional profiles of NiSi in [26].

Optical profilometry data in Fig. 10 provides a better picture of the surface morphology changes in the Ti/Ni contacts upon Ni silicidation after annealing at 700 °C. The surface roughness increased from 3.28 nm to 95 nm. This is expected as per reports of agglomeration in the existing literature [25].

After annealing, X-ray diffraction data were taken from the samples in Table 5. NiSi (211) and (013) peaks were detected, as shown in Fig. 11.

From the contact resistance values measured on the samples (Table 6, Table 7), it can be concluded that irrespective of residue removal treatment or dopant diffusion masks, the final values of contact resistances after high-temperature contact annealing are in a similar range of $\sim 5 \times 10^{-5}$ Ω cm^2 with most values within one standard

Table 5
Summary of processing steps for various samples.

Samples	Dopant Diffusion Mask	Post-doping residue removal	Metal Contact	Contact Annealing Parameters (N_2 ambient)
M1-NP2	Dual-Layer SOG, baked at 400 °C for 60 min.	–	Ti(20 nm)/Ni (300 nm)	450 °C,30min + 700 °C, 45s + 105s
M1-PN2				700 °C, 45s + 105s
M1-PN6		SF_6 Plasma dry etch		700 °C, 45s + 45s
M1-NP5		HNO_3 treatment		700 °C, 45s + 105s
M2-PN2	Dual-Layer SOG, baked at 400 °C for 60 min + 700 nm PECVD Oxide, Dual SOG + 700 nm PECVD Oxide baked at 900 °C for 30min	–	Ni (300 nm)	–
M2-NP2		–	Ti(20 nm)/Ni (300 nm)	700 °C, 120s
M3-PN2		–		700 °C, 180s + 120s
M3-NP2		–		700 °C, 180s + 120s
M3D-PN2		HNO_3 treatment	Ni (120 nm)	450 °C, 180 s
M3D-NP3		–	Ti(20 nm)/Ni (300 nm)	700 °C, 105s + 60s

(M1, M2, and M3 refer to masks as described in Table 1. NP implies Phosphorus doping was done before Boron doping. PN implies that Boron doping was done before phosphorus doping. M1-PNx means that the sample had a diffusion mask of dual SoG, and the Boron doping was done before the Phosphorus doping. 'X' denotes the sample number.).

Table 6
Contact resistivity and sheet resistance data for samples where round 1 of doping was with Boron.

Samples	Specific Contact resistivity (Ω cm^2)		Sheet Resistance (Ω/sq)	
	p-type	n-type	p-type	n-type
M1-PN2	6.31×10^{-5}	3.65×10^{-5}	5.19	4.14
M1-PN6	4.98×10^{-5}	7.56×10^{-5}	5.2	6.6
M2-PN2	4.36×10^{-5}	6.00×10^{-5}	5.76	3.23
M3-PN2	6.22×10^{-5}	5.49×10^{-5}	5.76	3.23
M3D-PN2	2.63×10^{-5}	4.00×10^{-5}	5.54	3.09

Table 7
Contact resistivity and sheet resistance data for samples where phosphorus was doped first.

Samples	Specific Contact resistivity (Ω cm^2)		Sheet Resistance (Ω/sq)	
	p-type	n-type	p-type	n-type
M1-NP2	2.04×10^{-5}	4.64×10^{-5}	7.00	3.12
M1-NP5	3.44×10^{-5}	3.82×10^{-5}	4.80	3.92
M2-NP2	4.75×10^{-5}	4.86×10^{-5}	6.34	3.06
M3-NP2	4.05×10^{-5}	2.42×10^{-5}	6.54	4.20
M3D-NP3	4.89×10^{-5}	7.55×10^{-5}	7.53	4.15

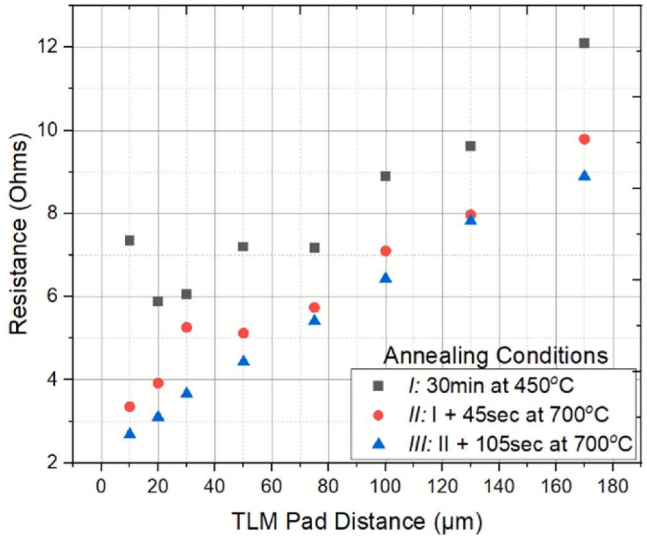

Fig. 8. Reduction in resistance between TLM pads on n-type regions for different anneal parameters. The annealings are done consecutively on the same sample. The sample has undergone nitric acid treatment. Legend denotes the annealing temperature and times.

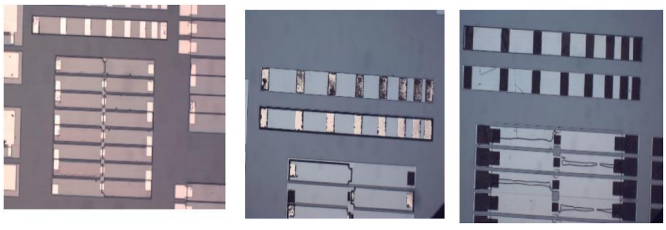

Fig. 9. (a) sample before annealing. (b) Incomplete and non-uniform silicidation (c) sample after Ni silicidation upon annealing at 700 °C.

deviation of the mean. The lowest reported values [23] for NiSi are ~1 × 10^{-5} Ω cm^2 with a Holmium interlayer.

Despite reaching similar final contact resistivity values, the initial contact behavior did depend on residue removal treatment. Amongst the

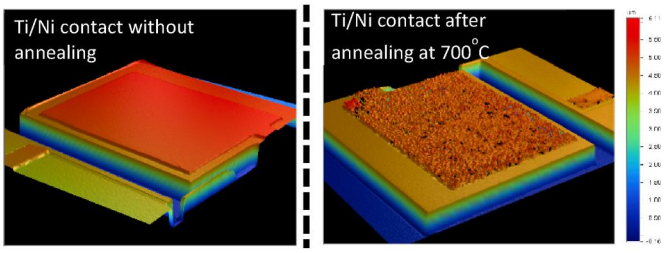

Fig. 10. Effect of annealing on the surface morphology of Ti(20 nm)/Ni(300 nm) contacts due to silicidation.

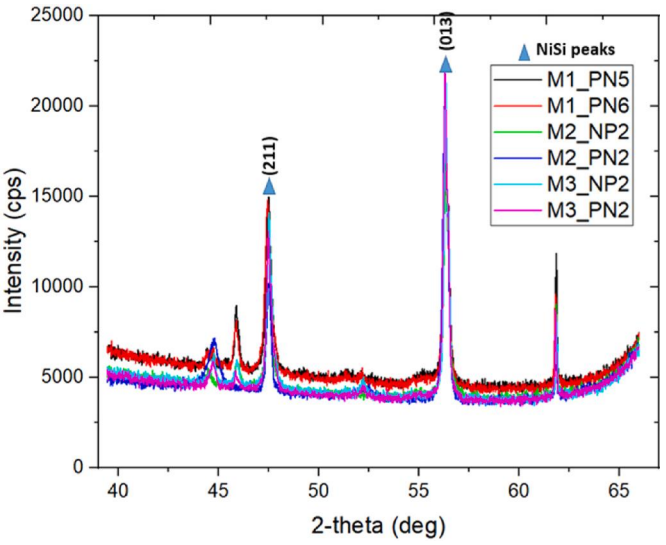

Fig. 11. NiSi peaks detected in XRD data from various samples after contact annealing.

samples not undergoing any hot nitric acid treatment, the TLM resistance values before annealing were higher than 200 Ω with a nonlinear variation. After high-temperature annealing, silicidation was observed, indicated by a visible change [24] in contact texture and appearance (Fig. 9) & the resistance measurements fell dramatically to the range shown in Fig. 8. In samples treated with nitric acid & a 450 °C forming gas anneal, lower contact resistivity was observed despite no visible evidence of silicidation. However, a subsequent 700 °C anneal further reduces their contact resistivity (Fig. 8) and shows signs of silicidation. Based on our observations of the evolution of contact resistivity with annealing in both treated and untreated samples, we conclude that once Ni silicidation is complete, the contact resistivities have very similar values, highlighting the greater importance of contact annealing over nitric acid treatment in attaining low contact resistivities. The annealing temperature is dependent on the choice of the metal stack. A Ti/Ni contact shows silicidation only above 700 °C. This agrees with Setiawan et al. [24], although, in that work, a Ti/Ni alloy target was sputtered while we deposited a Ti(20 nm)/Ni(300 nm) stack. On the other hand, sample M3D-NP3 showed that a Ni contact could be converted to silicide at 450 °C, as also reported in [25]. This reduces the thermal budget but affects contact stability during post-metallization device processing as we faced adhesion problems with Ni only contacts. Since the post-metallization packaging process for our target thermoelectric device involves PECVD isolation oxide growth at 300 °C, deep reactive ion etching, and multiple rounds of wafer bonding, a metal contact stable at temperatures above 300 °C meets the device requirements.

4. Conclusion

We presented an optimized fabrication process for forming highly doped poly-Si thin films and their ohmic contacts. Working with spin-on dopants introduces unique challenges, such as residue formation and diffusion mask-related surface degradation. We conclude that proximity diffusion is better than direct dispense in an RTA setup to avoid BRL and reduce the sheet resistance. The choice of diffusion masks is essential for selective doping and surface quality, as proved by the consistently hydrophobic surfaces achieved with masks where PECVD oxide is in contact with poly-Si. The residue removal treatment involving the heating of samples in nitric acid has been explored. We recommend an oxidizing ambient and a PECVD oxide-based mask to avoid residue and eliminate the need for nitric acid treatment. In the case of non-visible residue, nitric acid treatment may be excluded since the final contact resistivity value depends more on the silicidation during high-temperature contact annealing. In the presence of a visible residue, nitric acid treatment can be deployed to oxidize and subsequently etch away the BRL. If post-metallization thermal contact stability is a priority, Ti/Ni contacts are more suitable than Ni contacts. Furthermore, Ti/Ni contacts show superior adhesion characteristics. Dopant dependence of the sequence of silicidation was also observed during the course of these experiments.

CRediT authorship contribution statement

Prithu Bhatnagar: Writing – original draft, Methodology, Investigation, Formal analysis. **Daryoosh Vashaee:** Writing – review & editing, Project administration, Funding acquisition, Conceptualization.

Declaration of competing interest

The authors declare that they have no known competing financial interests or personal relationships that could have appeared to influence the work reported in this paper.

Data availability

Data will be made available on request.

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