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A Scalable Integrated DC/DC Converter with Enhanced Load Transient Response and Security for Emerging SoC Applications

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***Abstract*— In this paper we propose a novel integrated DC/DC converter featuring a single-input-multiple-output architecture for emerging System-on-Chip applications to improve load transient response and power side-channel security. The converter is able to provide multiple outputs ranging from 0.3V to 0.92V using a global 1V input. By using modularized circuit blocks, the converter can be extended to provide higher power or more outputs with minimal design complexity. Performance metrics including power efficiency and load transient response can be well maintained as well. Implemented in 32nm technology, single output efficiency can reach to 88% for the post layout models. By enabling delay blocks and circuits sharing, the Pearson correlation coefficient of input and output can be reduced to 0.1 under re-keying test. The reference voltage tracking speed is up to 31.95 V/µs and peak load step response is 53 mA/ns. Without capacitors, the converter consumes 2.85 mm^2 for high power version and only 1.4 mm^2 for the low power case.**

Keywords—DC/DC converter, load transient response, dynamic voltage scaling, scalability, power side-channel security.

I. Introduction

Power management for System-on-Chip (SoC) applications is facing new challenges as both load transient responses and side-channel security requirements are becoming more important [1]. Meanwhile, as more Internet-of-Things (IoT) and Edge Computing enabled applications come to the market, we are looking for more flexible and scalable solutions to lower design complexity and reduce cost without sacrificing any performance. Traditionally, large off-chip power converters are working with point-of-load on-chip converters to meet power delivery and management requirements. However, the limited area cannot allow independent power supplies for each of the ever-increasing number of workloads [2, 3]. On the other hand, protecting such embedded devices from various types of attacks are also urgent. Among them power side-channel attack is still the most common and effective one to steal critical information from the circuit. Thus, conventional architectures may not be sufficient, to match response speed, efficiency, scalability, and security requirements [4, 5]. In this paper we will target these problems and propose a hardware-based solution by using single-input-multiple-output DC/DC converter. The proposed converter will feature modularized circuit blocks in order to be scaled easily. In Section II we will show the converter schematics and related control blocks. Both transient response waveforms and security related test results are shown in Section III with a brief discussion about scalability. In Section IV we will summarize the work with some future works.

II. Proposed Design

In this paper most of the results will be based on the 3-output DC/DC converter shown in Figure 1 and later the 6-output version will be shown to demonstrate scalability. In this figure the first stage is used to generate additional voltage rails and the second stage is to do voltage regulations. Reference voltages are generated from off-chip circuits and output capacitors are modelled off-chip as well. V_{set} here is added externally to help select the right pair of switches for charging and discharging.

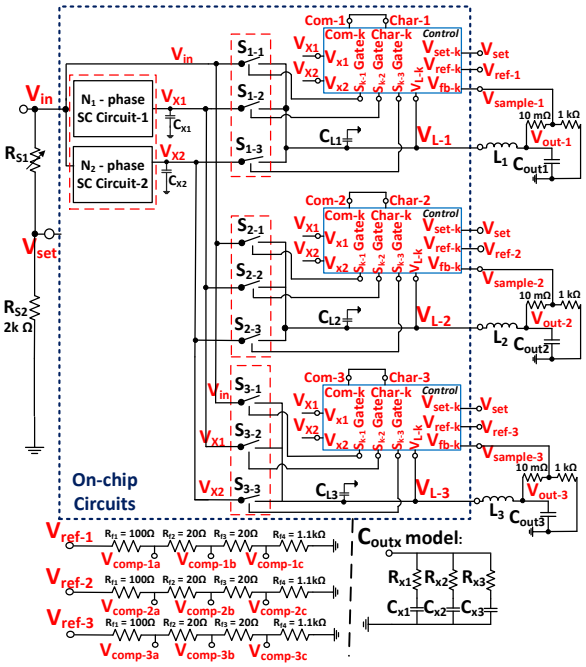

Fig. 1. Schematic of the 3-output converter, showing 2 switched capacitor circuits as the first stage, and 3 controllable switches and low pass filters as the second stage. Reference voltages come from off-chip sources and are used to generate 3 compensation voltages for delay and auxiliary blocks.

Details of the control block are shown in Figure 2. In this work we use $V_{set} = V_{set\text{-}k} = 550$mV. Without enabling the delay block, port *Com-k* and *Char-k* are connected directly. Auxiliary

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circuits and delay blocks are shown in Figure 3 and 4. Auxiliary blocks are only added when power ratings are higher to improve efficiency. Delay blocks are inserted between port *Com-k* and *Char-k* to enhance side-channel leakage resistance. The delay time varies based on the 5-bit results Crl(x) coming from the five comparators. From post-layout simulations, the delay varies from 0.4 ns to 2.9 ns and C1 = C2 = 4pF.

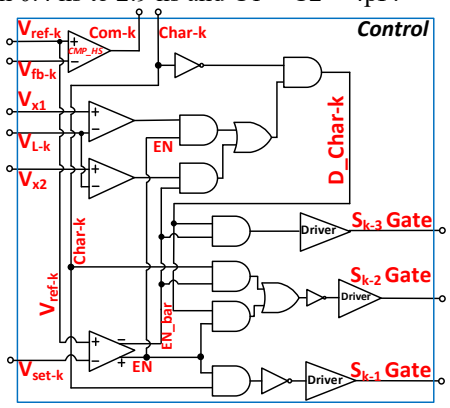


Fig. 2. Schematic of the control block where gate driving signals for switches are generated based on multiple references.

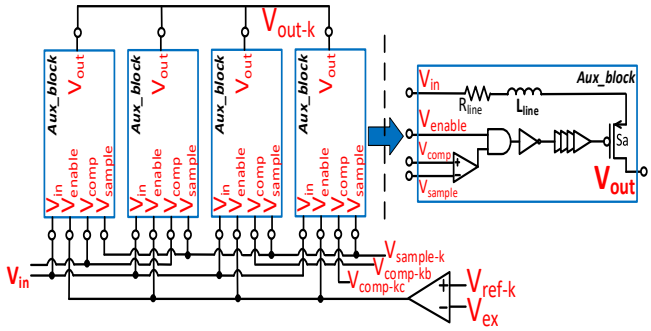


Fig. 3. Schematic of auxiliary circuits (left) for V_{out-k} showing how multiple compensation and sampled voltages are used, and aux blocks (right) is shown in details with R_{line} = 0.03 Ω, L_{line} = 8.7 pH.

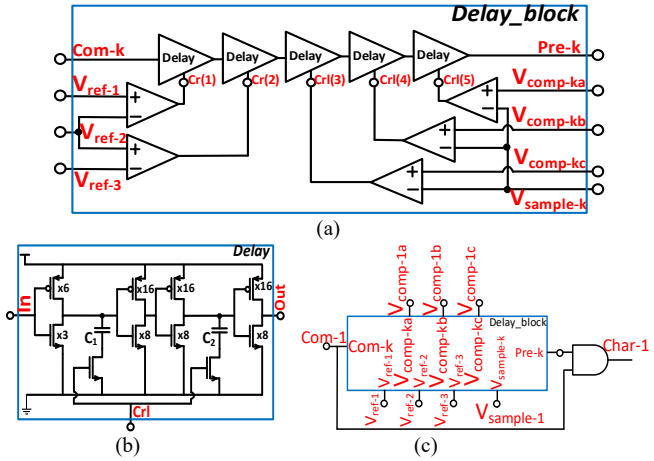


Fig. 4. Schematics of (a) the delay block; (b) details of each delay unit; and (c) usage of the delay block of output-1 by inserting it between port *Com-1* and *Char-1* of the control block.

The regulated output V_{out-k} follows equation (1) and (2) where T_{char} and T_{disc} are charging and discharging time determined by the control block.

When $V_{set} < V_{ref-k} < V_{in}$,

$$V_{out-k} = T_{char} * V_{in} + T_{disc} * V_{x1} \quad (1)$$

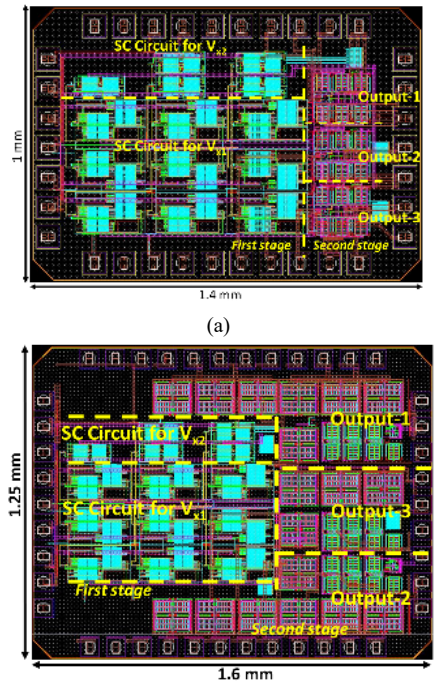
When $0 < V_{ref-k} < V_{set}$,

$$V_{out-k} = T_{char} * V_{x1} + T_{disc} * V_{x2} \quad (2)$$

In this work we follow our previous works [6] by using modularized PMOS and NMOS switches and fixed switched-capacitor circuits to lower design complexity and enable scalability. We let V_{x1} = 2/3 V_{in} and V_{x2} = 1/3 V_{in}. Each basic MOS switch block is designed to support up to 40mA load current and each switched capacitor circuit reaches about 81.6% efficiency while supporting 40mA current.

III. Implementation and Results

Post-layout models (in 32nm technology) are implemented to get all the simulation results. We first designed a low-power version as shown in Figure 5, which only supports up to 150mA each output and there are no delays or auxiliary blocks added. Then we propose a high-power version that supports up to 1A load and delays and Aux blocks are added as well, as shown in Figure 5(b).



(a)

(b)

Fig. 3. (a) Layout view of low-power version in which three outputs are identical and supposed to provide up to 150mA to each load; (b) layout view of the high-power version where output-1 and output-2is scaled to support high power, while output-3 is designed for lower power.

In this section both steady-state and load transient responses results will be listed based on post-layout simulations. We also add a total of 12.8 nF output capacitor based on off-chip ceramic models. Single output power efficiency is shown from Figure 7 to 9 for different cases. We can find out that the efficiency can be well maintained for different cases and these curves remain relatively flat for different loads. However, low voltage and lower power cases still suffer from additional loss due to additional control loss and charging loss. A 6-output

version is shown in Figure 6 while each output is designed to support about 150mA load. All the performance metrics maintain same as the 3-output one.

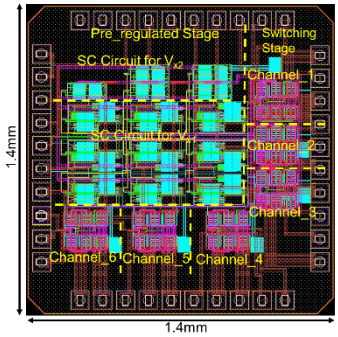


Fig. 6. Layout of the extended version of the converter with 6 output channels consuming 1.4mm x 1.4mm area;

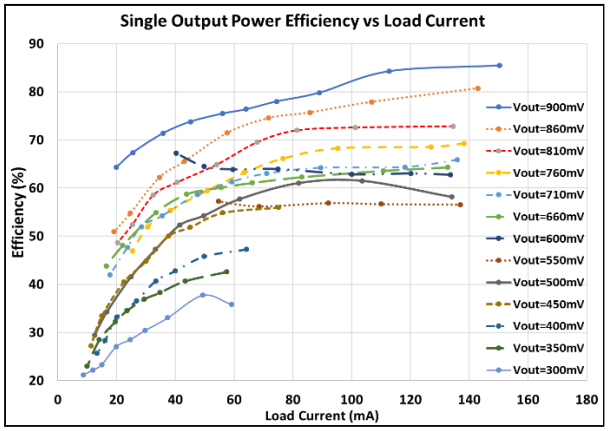


Fig. 7. Single-channel power efficiency versus load current for low power.

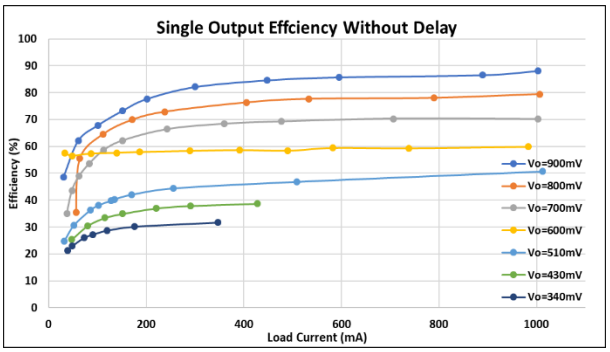


Fig. 8. Single output efficiency when no delays are added for high power case.

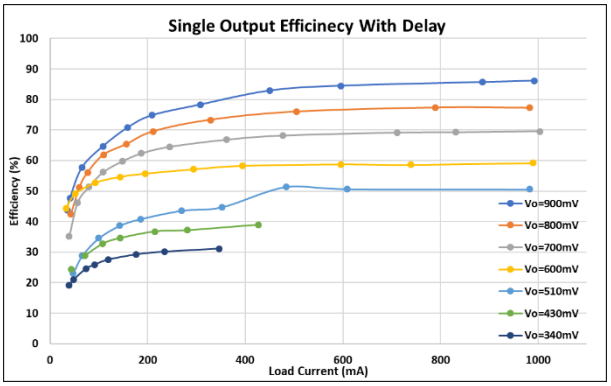


Fig. 9. Single output efficiency with delays blocks, for high power case.

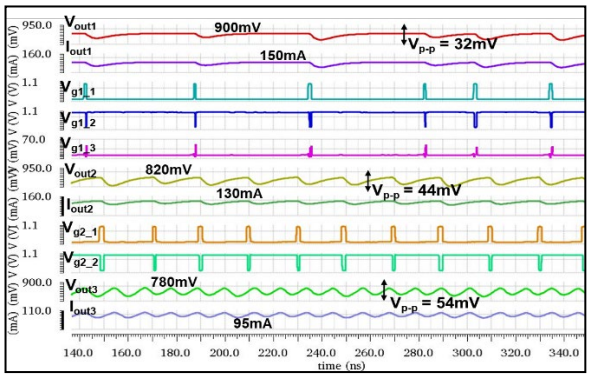


Fig. 10. Steady-state waveforms of three outputs for lower-power version, each supplying 150mA at 900mV, 130mA at 820mV and 95mA at 780mV with gate driving signals for output-1 and output-2 shown as well.

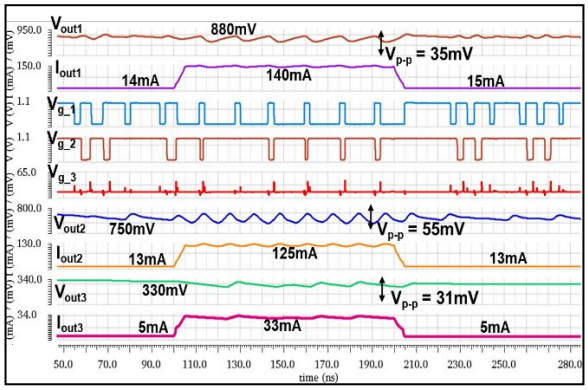


Fig. 11. Transient responses of all outputs (for low-power version) while responding to at least 6 times change in the load simultaneously showing no voltage droops/spikes and no observable cross regulations.

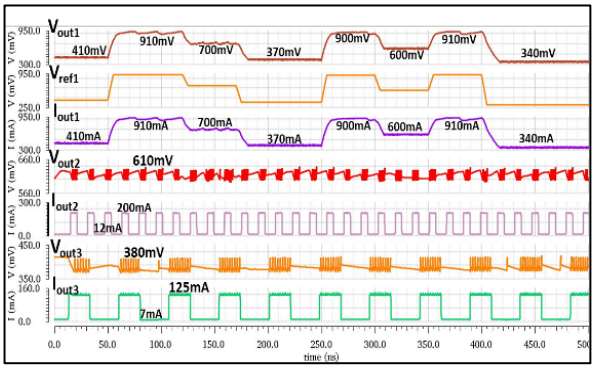


Fig. 12. Transient responses of all outputs in high-power version when V_{out1} is doing voltage scaling, and output-2 and -3 are responding to digital loads.

We can see from steady-state waveforms shown in Figure 10 that all the outputs are stable. We check load transient response including both load transitions voltage scaling. From Figure 11 and 12 for different versions, we can find out that all the outputs can remain stable without generating additional voltage spikes or droops, and there are no cross regulations among all the output voltages. A maximum step-up reference tracking speed of 30.6 V/µs and step-down of 31.9 V/µs are achieved. Max load current step response is 53 mA/ns.

Based on single-trace re-keying scenario, where the attacker can only get a few repetitive traces, we will do correlation coefficient and SNR studies which can reflect the security level of the converter. SNR in our work is

$$SNR = \frac{Var(I_{load})}{Var(I_L - I_{load})} \quad (3)$$

We first do an open-loop switch assignment test that connects the encryption load to different outputs following this sequence: to V_{out1} between 0 – 150ns and 440ns – 2µs; to V_{out2} between 150ns – 220ns and 260ns – 340ns; to V_{out3} between 200ns – 260ns and 340ns – 440ns. The transient waveforms are shown below in Figure 13.

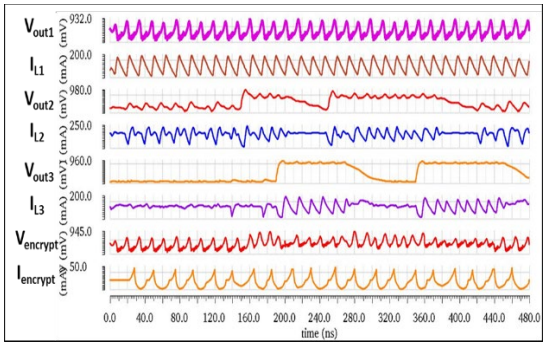


Fig. 13. Transient waveforms showing three output voltages, three inductor currents, encryption load supply voltage and current.

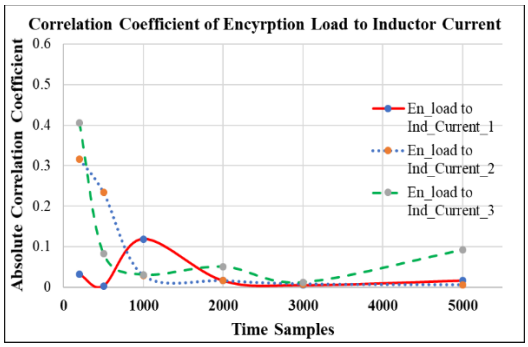


Fig. 14. Power correlation coefficient between actual encryption load current and different measurable inductor currents based on the switch assignment scheme.

TABLE V. COMPARISON WITH RELATED WORKS

Reference	[7]	[8]	[9]	[10]	This work
Technology	28nm	180nm	130nm	180nm	32nm
Input Voltage (V)	2.8-4.2	3.3	1.2	1.8	1
Output Voltage (V)	0.6-1.2	1-2.5	0.45-1.05	0.4-1.6	0.3-0.92
Load Current per Phase(mA)	33.3	1800	70	150	1000
Peak Efficiency (%)	78	90.7	71	87.5	88.0
Max Load Step Response (mA/ns)	0.2	23.6	0.75	0.07	**53**
Reference Tracking (V/µs)	N/A	4.25	2.9	0.0375	**31.9**
Max Voltage Ripple (mV)	12	< 20	84	100	95
Voltage Spike / Droop (mV)	Non-observable	225	100	160	Non-observable
Inductor (nH)	3	150	11.8	4700	1
Output Cap (nF)	50	660	3.2	6000	15.8
Chip Area (mm^2)	1.5	2.3	0.5	1.95	2.85

We can find out that the by using different outputs to supply the encryption workload, the correlations between the real encryption load and the measurable inductor currents all become quite week. More measurements are needed at first place to determine the connections between the inputs and the load and it becomes more difficult to further derive the key. We also compare the current work with other works in Table I.

IV. CONCLUSION

We presented a scalable DC/DC converter for multiple outputs to improve both load transient responses and side-channel security for emerging heterogeneous SoCs. Due to the modularized circuit blocks, the converter can be easily scaled to different power levels with low design complexity. Load transient responses are improved as the converter provides more than 2 times faster load transitions and 7 times faster voltage scaling speed than other works. Under re-keying scheme, with circuit sharing architecture, the correlation coefficient between input and output is reduced to less than 0.1, The proposed converter shows potentials in mitigating power side-channel attacks and solving load transient response power management issues for future SoCs.

Our future works include detailed modeling of the converter and exploring specific side-channel attack mitigations with a dynamic key insertion scheme.

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