A Scalable DC/DC Converter with Fast Load Transient Response and Security Improvement

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***Abstract*—We present a scalable DC/DC converter for system-on-chip (SoC) applications, to improve load transient response and reduce side-channel information leakage. Implemented using modularized circuit blocks, the proposed power supply can be scaled simply by interleaving and/or parallelizing. Using 1V as input, three outputs (each ranging from 0.3V to 0.92V with load currents from 40mA to 1A) are provided. Based on 32nm CMOS technology post-layout and in-package air-core inductor models, peak efficiency for a single output can reach 88%. Maximum reference voltage tracking speed is 31.95 V/μs and peak load step response is 53 mA/ns. There are no observable voltage spikes, droops or cross regulations at any outputs and this can be maintained for cases with different power ratings. Further, delay blocks and circuit sharing are employed to protect side-channel information. Under re-keying settings, the Pearson correlation coefficient between input and output can be lowered to 0.1 and the actual key induced power trace cannot be recognized. The signal-to-noise ratio (SNR) for correct key guess can also be reduced by 10 times to resist information leakage. Without output capacitors, the converter consumes 2.85 mm^2 chip area.**

Keywords—*DC/DC converter, load transient response, scalable, side-channel attack, correlation coefficient.*

I. Introduction

Power management for System-on-Chip (SoC) applications has always been crucial in obtaining performance and high efficiency [1]. As we are moving beyond Moore's law and Dennard scaling, emerging SoC applications will implement heterogeneous, customized and optimized units, such as signal transmitters, memories, multi-core processors, or GPUs and enable diverse operation modes and flexible integration to balance power consumption, performance demands and cost [2]. Conventional on-chip or off-chip power converters may not be sufficient, in terms of load transient response, voltage scaling, efficiency, scalability, and security, to meet various requests. Ideally, each workload should have one specifically designed power supply to meet these requirements efficiently [3], but the limited chip area cannot allow an infinite number of power supplies and ever-increasing design complexity. Exploring novel powering solutions that can power multiple workloads efficiently, reliably and securely is necessary.

Traditional methods that supply multiple and distributed workloads throughout the entire chip or package include (a) using hierarchical power network with distributed low dropout voltage regulators (LDOs) or (b) applying single inductor multiple output (SIMO) topologies. However, because of the limited regulation capability of small standardized LDOs, solutions belonged to method (a) may provide fine-grained and distributed voltages but cannot meet load transient response or voltage scaling requests [4]. On the other hand, SIMO related works can fully utilize the inductor by assigning charging and discharging for each output. But they would usually generate cross regulations and voltage droops along with slow response speed [5]. Some more recent works have derived better and simple control schemes and extended SIMO converter to multiple-input-multiple-output (MIMO) architectures with improved cross regulation performance [6]. But they could suffer from a voltage drop during load step transitions and some converters are built for board level applications with bulky inductors and limited output voltage range. The feasibility for on-chip applications is unexplored.

Besides, side-channel attacks over modern cryptographic circuits or low-cost embedded devices are evolving. Future applications would require more generic solutions to protect certain devices from side-channel attacks [7]. Among all types of encryption operation related information, power consumption is still one of the most effective one to steal critical data. State-of-the-art countermeasures against power side-channel attacks usually target isolating the power supply from the encryption device in order to break the correlation between input power and output data. Signature attenuation is also proposed recently to further increase MTD (minimum number of traces needed to disclosure). Unfortunately, these methods could induce more than 30% power or area overhead and overall design complexity is increased. A scalable solution with minimized performance overheads is preferred and demanded [8]. Recently, 2.5D or 3D integration is gaining more popularities recently as it provides an alternative to traditional 2D monolith designs to improve performance when Moore's law is ending. Figure 1 is an example of how four proposed power converters can fit into a 16-node SoC.

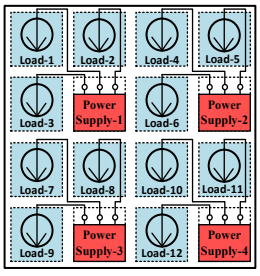

Fig. 1. The example floor plan showing how 4 proposed power converters can fit into a 16-node SoC, each supplying the 3 surrounding workloads.

Followed by technology advances in silicon interposer, System-in-Package (SiP) and Chiplet implementations are

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enabling more heterogeneous integrations and bringing optimized intellectual properties into the same system simply [9]. Considering this, our proposed converter will take advantage of in-package air-core inductors. In addition, we propose a delay stage that generates different delay timings for the control based on multiple reference voltages. The evaluation of side-channel leakage resistance will be based on power correlation coefficient and signal-to-noise ratio under single-trace scenario, which represents re-keying process and refers to one encryption cycle [7]. We also provide some studies about how to apply modularized circuit blocks under different cases for efficiency improvement. Load transient response and efficiency metrics can be well maintained for different power levels. Details of the converter are shown in Section II. Section III includes all the simulation setups and results for the converter, including both power management performance and study of side-channel leakage mitigations. Section IV concludes the work with future direction listed.

II. Proposed Converter

In our previous work [10], we proposed a simplified converter architecture as shown in Figure 2, where independent switched capacitor circuits are used to generate additional internal voltages while transistors and low-pass filters will provide regulated outputs at the second stage.

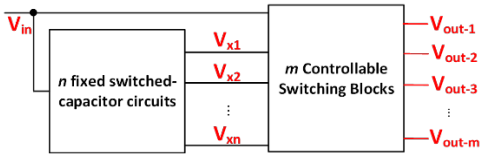

Fig. 2. The simplified architecture of the converter, where *n* additional internal voltage rails are generated through switched capacitor circuits and *m* regulated outputs are provide at the second stage.

In this design we will keep n = 2 so that there will be V_{in}, V_{x1} and V_{x2} serving as either charging or discharging source for the output. We follow steps in [11] and equations (1) and (2) to determine each transistor width W_{sw} and switching frequency f_{sw}, based on flying capacitor C_{fly}, peak inductor voltage $V_{L\text{-}k}$, and average inductor current I_{L_ave}.

$$f_{sw} \propto \frac{I_{L\_ave}}{C_{fly} * V_{L-k}} \quad (1)$$

$$W_{sw} \propto \sqrt{\frac{C_{fly} * I_{L\_ave}}{V_{L-k}}} \quad (2)$$

As reported in [11], enabling multiphase switched capacitor converters would improve efficiency but this benefit will quickly disappear if more than 10 phases are utilized. In our design, the maximum load current is 1A under a 900-mV supply voltage. Considering voltage drops due to parasitic impedance of each circuit blocks, in this design V_{x2} will always be the sinking source and V_{x1} will only be the source when V_{out} is lower than 550mV. In order to improve power efficiency, we propose modularized circuit blocks and then use interleaving or paralleling to fit different power levels. Modularized circuit blocks include switched capacitor circuits and PMOS/NMOS used in switching blocks. Here we choose 40mA as the sourcing or sinking capability for each component, which means I_{L_ave} would be 40mA for basic blocks. The schematic of two switched capacitor circuits are shown in Figure 3 with sizing information in Table I. Each switched capacitor circuit is controlled with a fixed 50MHz frequency and in this design, they can reach 81.6% efficiency while delivering 40mA. Another modularized block is the switch. We simply set PMOS and NMOS switch same size for easy layout routing. Similarly, each modularized PMOS is supposed to support 40mA and that for NMOS will be 80mA. The layout of the switch is shown in Figure 4.

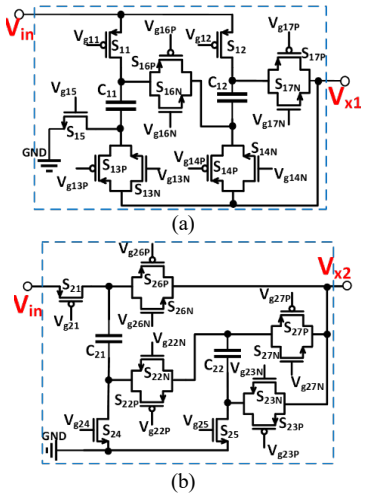

Fig. 3. (a) The schematic of SC circuit located at first stage with voltage conversion ratio 2/3; (b) the schematic of SC circuit with voltage conversion ratio 1/3.

TABLE I. Components Information

Component	Sizing Information
PMOS S_{11}, S_{12}	W/L: 124.8 µm / 40 nm
NMOS S_{13N}, S_{14N}, S_{16N}, S_{17N}	W/L: 31.2 µm / 40 nm
NMOS S_{15N}	W/L: 62.4 µm / 40 nm
PMOS S_{13P}, S_{14P}, S_{16P}, S_{17P}	W/L: 62.4 µm / 40 nm
PMOS S_{21}	W/L: 20.8 µm / 40 nm
PMOS S_{22P}, S_{23P}, S_{26P}, S_{27P}	W/L: 10.4 µm / 40 nm
NMOS S_{22N}, S_{23N}, S_{26N}, S_{27N}	W/L: 5.2 µm / 40 nm
NMOS S_{24N}, S_{25N}	W/L: 10.4 µm / 40 nm
C11, C12	0.8 nF
C21, C22	0.5 nF

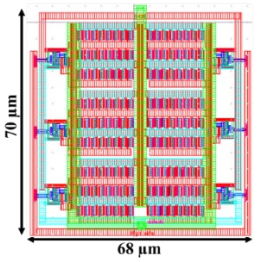

Fig. 4. Layout of a modularized PMOS or NMOS transistor switch with driving circuits and supports 40mA load current.

By using modularized circuit blocks, our proposed power converter with three outputs is shown in Figure 5. Theoretically, we can choose any combinations of N1 and N2 depending on the power rating. Decoupling caps C_{x1} and C_{x2} are optional. In Figure 5 if there are no delay blocks, port *Com-k* and *Char-k* of the control block is connected. Since our reference voltages come externally, for each one we build a simple voltage division to generate a few more voltage levels to help tune the delay units and other controls. Output capacitor is also modeled using commercial off-chip ceramic capacitors just for simulations.

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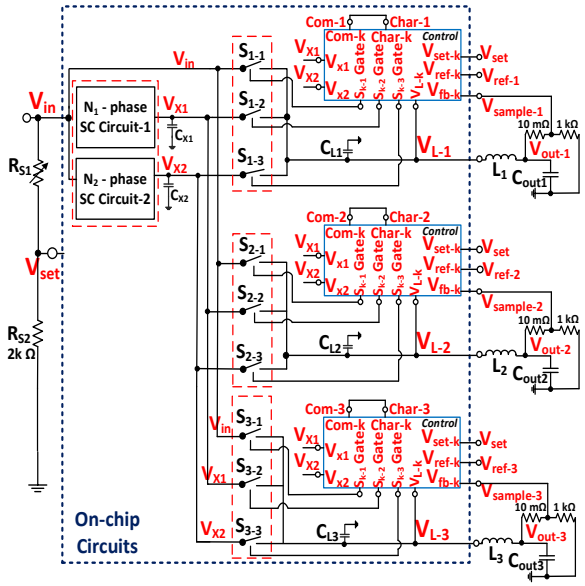

Fig. 5. Schematic of the 3-output converter, showing 2 switched capacitor circuits as the first stage, and 3 controllable switches and low pass filters as the second stage.

The regulated output $V_{out\text{-}k}$ follows equation (3) and (4) where T_{char} and T_{disc} are charging and discharging time determined by the control block.

We select V_{set} = 550mV to help assign charging and discharging sources accurately. The control block will assign charging and discharging signals to two switches in each output, based on feedback sample voltage, reference voltage and inductor node voltages. The delay block will be connected between port *Com-k* and *Char-k* if needed, otherwise the two ports are directly connected. In our work the delay is only added directly to change the original charging signal coming from hysteresis comparator *CMP_HS*. Details of the control block are shown in Figure 6.

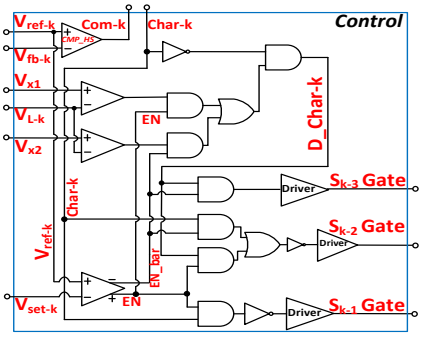

Fig. 6. Schematic of the control block where gate driving signals for switches are generated based on multiple references.

When $V_{set} < V_{ref\text{-}k} < V_{in}$,

$$V_{out\text{-}k} = T_{char} * V_{in} + T_{disc} * V_{x1} \quad (3)$$

When $0 < V_{ref\text{-}k} < V_{set}$,

$$V_{out\text{-}k} = T_{char} * V_{x1} + T_{disc} * V_{x2} \quad (4)$$

We also propose auxiliary circuits, as shown in Figure 7, to reduce output voltage ripples and ensure enough power delivery when the converter is scaled to provide more load current. Each auxiliary circuit has four *Aux* blocks, in which the input voltage is connected to the output through a PMOS switch *Sa*. V_{ex} can be tuned to change the activation condition. This switch *Sa* is turned on whenever the sampled voltage is lower than any compensation voltages. Due to high switching frequency and parasitic impedance R_{line} and L_{line}, the auxiliary circuits will not cause any short circuits. Based on layout results, R_{line} = 0.03 Ω, L_{line} = 8.7 pH.

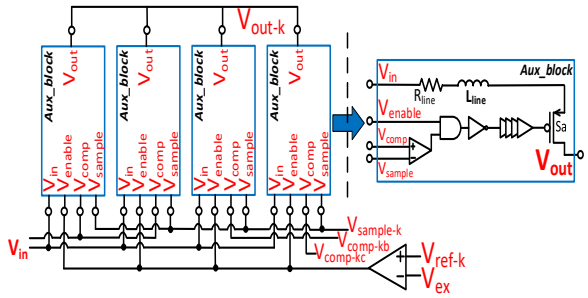

Fig. 7. Schematic of auxiliary circuits (left) for $V_{out\text{-}k}$ showing how compensation and sampled voltages are used with aux blocks (right) to reduce output ripples and provide enough power.

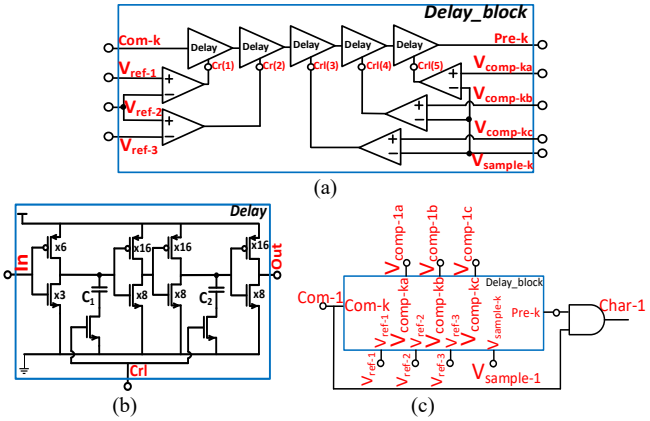

Fig. 8. Schematic of (a) the delay generation block; (b) details of the delay unit; and (c) how the delay block is applied to output-1 by inserting between port *Com-1* and *Char-1* of the control block.

The proposed converter is designed to resist side-channel attacks. Due to the shared components, the converter can intrinsically complicate the relationships between inputs and outputs. To further improve security level, we propose specialized delay blocks, which utilize three reference voltages and three compensation voltages, to generate delays that are added to the original control signals. The schematics of the delay blocks are shown in Figure 8, together with how it can be applied to output-1, with just an additional AND gate to connect *Com-1* and *Char-1*. The delay time varies based on the 5-bit results Crl(x) coming from the five comparators. From post-layout simulations, the delay varies from 0.4 ns to 2.9 ns and C1 = C2 = 4pF.

III. Simulation Results

A. Implementation

In this design we extend the previous work (supports up to 150mA per output) by adding more switches at the second stage to support up to 1A load. Using discrete layout models, we first studied how different numbers of modularized circuit blocks can affect the power efficiency and provide near-optimal

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combinations for different outputs in Table II and III. Other than N1 and N2, we define numbers P1, P2 and K for PMOS S_{k-1}, PMOS S_{k-2} and NMOS S_{k-3}. We can see from these tables that when output voltage locates at the higher range, number of charging PMOS is proportional to the load current while other parameters only have limited effect. For low voltage cases, we need more switched capacitor circuits to do both charging and discharging. Based on this study, we have our extended version shown in layout and shown in Figure 9 with N1 = 9, N2 =5, P1 = 20, P2 = 8 and K = 1.

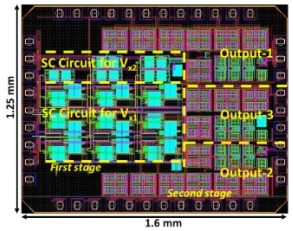

Fig. 9. Layout view (using 32nm CMOS technology) of the proposed converter where output-1 and output-2 are scaled to support high power, while output-3 is designed for lower power.

TABLE II. NEAR-OPTIMAL COMBINATION FOR V_{OUT} = 930 mV

R_{load}	I_{load}	N_1	N_2	P1	P2	K
2 Ω	465 mA	5	1	15	2	1
3 Ω	310 mA	5	1	10	2	1
4.5 Ω	206.7 mA	5	1	8	2	1
6 Ω	155 mA	5	1	6	2	1
9 Ω	103.3 mA	5	1	4	2	1
18 Ω	51.7 mA	2	1	2	1	1
20 Ω	46.5 mA	2	1	1	1	1
30 Ω	31 mA	2	1	1	1	1
45 Ω	20.7 mA	2	1	1	1	1

TABLE III. NEAR-OPTIMAL COMBINATION FOR V_{OUT} = 330 mV

R_{load}	I_{load}	N_1	N_2	P1	P2	K
1.5 Ω	220 mA	9	5	N/A	8	1
2 Ω	165 mA	9	3	N/A	5	1
2.4 Ω	137.5 mA	8	3	N/A	3	1
3 Ω	110 mA	6	3	N/A	2	1
4 Ω	82.5 mA	4	2	N/A	2	1
5 Ω	66 mA	4	1	N/A	2	1
6 Ω	55 mA	4	1	N/A	2	1
10 Ω	33 mA	2	1	N/A	2	1

B. Simulation Setup and Results

In this section both steady-state and load transient responses results will be reported for the extended version with studies on side-channel leakage protection. The simulation is done through Cadence Virtuoso and the setup is shown in Figure 10. All the two-stage converters and proposed delay and auxiliary blocks are implemented together on-chip. We measure all the input and output voltages and currents and change load resistors to reference voltages to create different operation conditions. Following commercial air-core inductor designs and our previous work, we choose the 1nH model with all the parasitics added and the information is shown in Table IV. $C_{L1} = C_{L2} = C_{L3}$ = 100pF and they are just for testing without optimization. Each of the two symmetrical outputs supports up to 1A load and one low-power output is designed to provide up to 500mA load. Auxiliary circuits, designed to support 100 mA current, are included for all the outputs but delay blocks are only applied to Output-1 and -2. We set V_{ref-2} = 700mV and V_{ref-3} = 400mV to activate delays when collecting single output efficiency.

TABLE IV. SIMULATED AIR-CORE INDUCTOR PARAMETERS

Inductance	Size	DCR	ACR at 250MHz
1 nH	0.7mm * 0.68mm * 0.25 mm	8.0 mΩ	70.2 mΩ

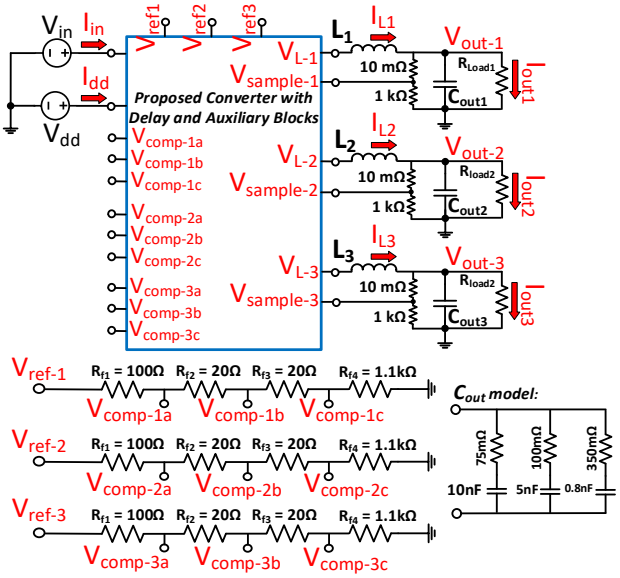

Fig. 10. Overview of the simulation setup where only the proposed converter is on-chip embedded with layout parasitics and other circuit components are based on models and for test use.

For most the load cases, the efficiency curves can remain flat but delivering low output voltages still suffer from additional control losses as the structure is fixed. To improve low-power and low-voltage efficiency, we need circuit level reconfigurations to activate different modular circuits blocks. Based on results shown in Fig. 11 and 12, each delay block will cause an average of 2% power loss.

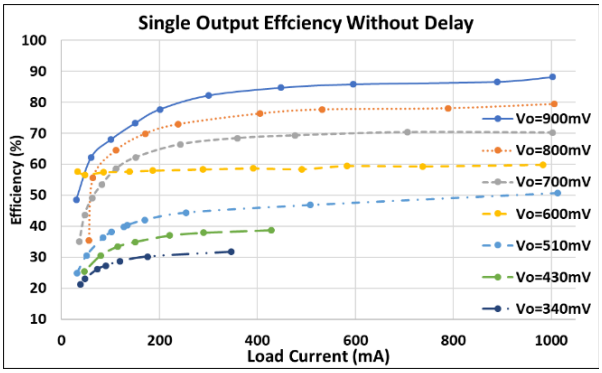

Fig. 11. Single output efficiency when no delays are added.

We check the load transient response performance by revising either the reference voltages or output load resistors. and as shown in Fig. 13 and all the three outputs are responding to different load demands. All the transitions are set to be done in 5ns. We can observe that there are no cross regulations or voltage spikes/droops observed. Based on simulation results, this proposed extended version provides a maximum step-up reference tracking speed of 30.6 V/μs and step-down of 31.9

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V/µs. When load has a step transition within 5ns, the maximum output response speed is 53 mA/ns. The high frequency ripples at V_{out2} and V_{out3} come from the activation of auxiliary circuits.

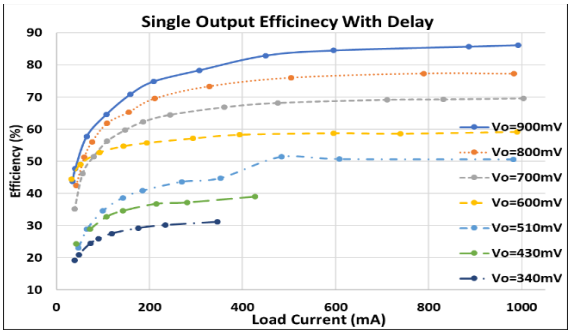

Fig. 12. Single output efficiency with delays blocks activated.

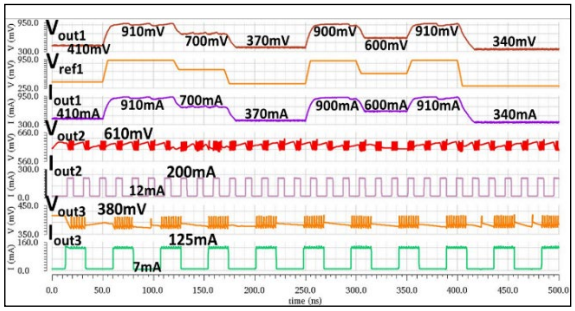

Fig. 13. Transient responses of all outputs when V_{out1} is doing voltage scaling, and output-2 and -3 are responding to digital loads.

We also compare our work with several recent works from [12]-[15] in Table V in terms of power management.

TABLE V. COMPARISON WITH RELATED WORKS

Reference	[12]	[13]	[14]	[15]	This work
Technology	28nm	180nm	130nm	180nm	32nm
Input Voltage (V)	2.8-4.2	3.3	1.2	1.8	1
Output Voltage (V)	0.6-1.2	1-2.5	0.45-1.05	0.4-1.6	0.3-0.92
Load Current per Phase(mA)	33.3	1800	70	150	1000
Peak Efficiency (%)	78	90.7	71	87.5	88.0
Max Load Step Response (mA/ns)	0.2	23.6	0.75	0.07	**53**
Reference Tracking (V/µs)	N/A	4.25	2.9	0.0375	**31.9**
Max Voltage Ripple (mV)	12	< 20	84	100	95
Voltage Spike / Droop (mV)	Non-observable	225	100	160	Non-observable
Inductor (nH)	3	150	11.8	4700	1
Output Cap (nF)	50	660	3.2	6000	15.8
Chip Area (mm^2)	1.5	2.3	0.5	1.95	2.85

Other than power management related performance, we also explore whether the converter can mitigate side-channel leakage. There are multiple performance metrics like MTD, attenuation ratio or SNR that can determine how much a design can resist side-channel attacks. Ultimately the objectives are to decorrelated input from output and to increase the number of traces that attackers need to collect in order to derive the security key [7]. In this design we will use Pearson Correlation coefficient [16] and SNR to evaluate our design. In a correlation power analysis, hypothetical power traces with correct key guess would reflect correlation peaks referring to real measurement. Meanwhile, as shown in [7], SNR for the correct key-guess related power trace would be much larger than those using incorrect key guesses and could reach as much as 0.5. Considering this, based on single-trace re-keying scenario, where the attacker just needs to get a few repetitive traces, we will do correlation coefficient and SNR studies. We directly collect the correct key related current waveforms (with delay blocks) and the measurable inductor currents to check the performance. Using the setup in Figure 10, the SNR is

$$SNR = \frac{Var(I_{load})}{Var(I_L - I_{load})} \tag{5}$$

We add an additional open-loop switch assignment scheme for testing that connects the encryption load to different outputs following this sequence: to V_{out1} between 0 – 150ns and 440ns – 2µs; to V_{out2} between 150ns – 220ns and 260ns – 340ns; to V_{out3} between 200ns – 260ns and 340ns – 440ns. The transient waveforms are shown below.

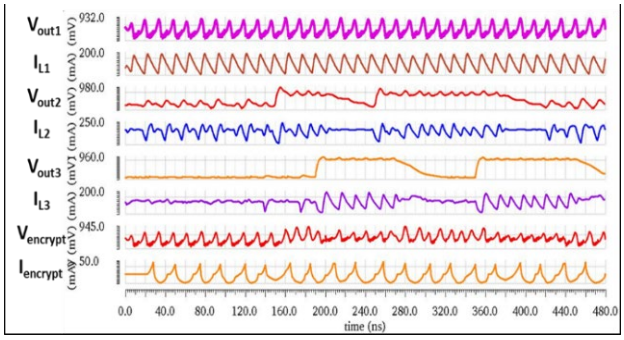

Fig. 14. Transient waveforms showing three output voltages, three inductor currents, real encryption load supply voltage and current.

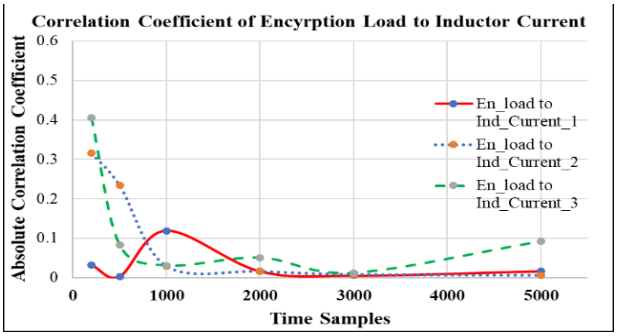

Fig. 15. Power correlation coefficient between actual encryption load current and different measurable inductor currents.

We can find out that the by switching multiple outputs to supply the encryption workload in a preset sequence, the correlations between the real encryption current and the measurable inductor currents all becomes quite week. This method could be very helpful since more measurements are needed at first place to determine the connections between the inputs and the load. Based on the three-output architecture setup

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in Figure 10, we generate multiple guess related power traces, by revising load resistors to create digital or steady-state workload. Figure 16 shows the results of correlations between actual input measurement and different key-guess related power traces. Theoretically the solid curve should be identifiable as it is based on real key. With delay units and shared circuit blocks, it cannot be easily recognized and leads to more difficulties for attackers. In addition, we connect the same encryption load to one output that supplies a steady-state 900mV with a digitalized workload, which is similar to I_{out2} shown in Figure 13 but the magnitude only switches between 1.5mA and 15mA. By measuring the encryption load current and inductor load current, we can calculate the SNR based on sample numbers.

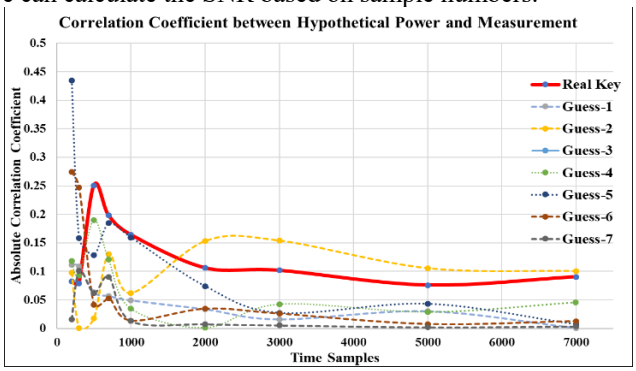

Fig. 16. Correlation coefficient between key-guess related hypothetical power traces and real measurements for re-keying scenario where the actual key related power trace may not be easily identified.

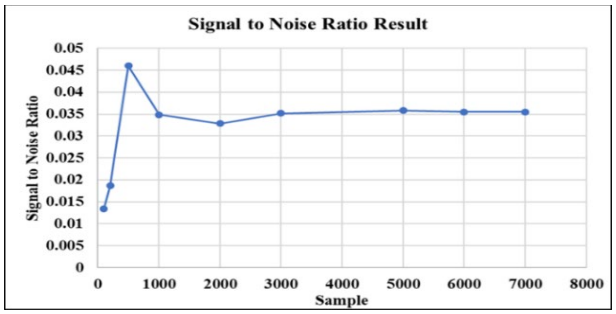

Fig. 17. Signal to Noise Ratio when one output is shared by encryption engine and a digitalized load.

For traditional side-channel attack implementations, when the correct key guess is made, we can easily observe a SNR of the predicted power as 0.4 or 0.5 which could help confirm the key guess. In our simulations the load current represents the correct key guess related power and we can see the SNR is reduced by 10 times. With total 5.5% power overhead and 4.8% area overhead, the reduction of SNR for the correct key guess shows potentials in resisting side-channel information leakage.

IV. Conclusion

We presented a scalable DC/DC converter that can be distributed for multiple outputs for emerging heterogeneous SoCs. Due to the two-stage architecture and modularized circuit blocks, the converter can be easily scaled to different power levels with low design complexity. Load transient responses are improved as the converter provides more than 2 times faster load transitions and 7 times faster voltage scaling speed than other works. We also propose delay blocks working with circuit sharing that successfully lower the correlation coefficient between input and output to less than 0.1, hide the actual key related power trace and reduce the SNR of the encryption load by 10 times compared to unprotected cases. The proposed converter shows potentials in mitigating power side-channel attacks and solving power management issues for future SoCs.

Our future works include detailed modeling of the converter and exploring side-channel attack mitigations with a dynamic key insertion scheme and real encryption circuits.

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