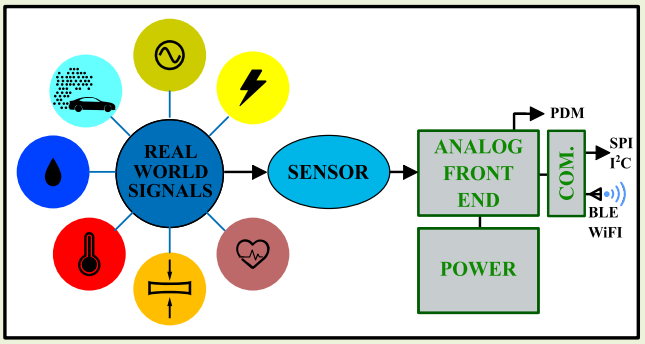
Trade-Offs in Sensor Systems Design: A Tutorial

Christos Sapsanis, *Student Member, IEEE*, Marios Sophocleous, *Member, IEEE*, Andreas G. Andreou, *Fellow, IEEE*, and Julius Georgiou, *Senior Member, IEEE*

***Abstract*—In this tutorial, we discuss trade-offs in sensor system design. With examples from engineered systems in our laboratories, we address design considerations at the different system levels, from the choice of a particular sensor to the signal conditioning circuits, the choice of data converter, and data communication physical interfaces. Fundamental concepts from communication and information theory, as well as practical considerations applied to specific case studies, are presented for sensor readout systems. In particular, we address both fundamental trade-offs such as choice of signal representation for signal conditioning and conversion, as well as practical and technological trade-offs such as place of quantization (signal data conversion) application demands and integration technologies. The tutorial deals with what is commonly referred to as the Analog Front End (AFE) up to the point where the physical signal is represented in digital symbols. Although the discussion focuses on all the processing steps of the AFE, a more system-level approach is further explored, including stand-alone system approaches and system communication. Major system trade-offs during system design are discussed, providing important methodology insights towards the design of sensory systems operating within demanding constraints.**



***Index Terms*—End-to-end sensor systems design, sensor interfaces, design trade-offs, signal to noise ratio.**

I. Introduction

SENSORY systems are pervasive in our everyday life. Today's typical smartphone is equipped with a wealth of passive and active sensory peripherals [1]. There are over a dozen sensors for scalar physical signals such as temperature, pressure, and humidity and half a dozen sensors for vector quantities as in cameras (light), microphones (sound) and inertial measurement units/accelerometer (inertia/acceleration), finger tracking (electromagnetic sensing). In sensory subsystems, the physical quantity of interest is transduced and processed by a series of functional blocks for storage and precise restitution of information; display a picture on the screen of the smartphone or extract relevant information for further action, sense the rotational motion of the phone and rotate displayed image to adapt to the user action.

Internet-of-Things [2] (IoT) and smart appliances also rely on a multitude of sensors to interact with the environment, including humans. Intelligent, cyber-physical systems are currently investigated in a variety of sectors, including intelligent manufacturing (robots that work safely with people in shared spaces), smart grid and utilities (systems for efficient and effective transmission and distribution of electric power), smart buildings, and infrastructure (active monitoring and control of buildings), transportation and mobility (vehicle to vehicle communications, autonomous vehicles) and medical devices with cognitive capabilities [3]. IoT devices are often considered the "edge" of an extensive, sophisticated cloud processing infrastructure. Autonomous operation and decision making coupled with real-time local processing before information transmission necessitates feature-driven "intelligent" sensing nodes with extreme energy efficiency.

The Amazon Echo, 4^{th} Generation depicted in Fig. 1 is an example of a state-of-the-art sensory system. The "teardown" [4] of the device shows a system architecture based on a small number of chips that communicate to each other via industry-standard interfaces and include four microphones as well as a light sensor. The microphones' audio analog-to-digital converters constitute the front end, while the two MediaTek processors (compute and radio-subsystem) and the SK Hynix memory constitute the back end. It is worth noting that the addition of the AI accelerator in one of the MediaTek

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Christos Sapsanis and Andreas G. Andreou are with the Department of Electrical and Computer Engineering, Johns Hopkins University, Baltimore, MD 21218 USA (e-mail: csapsanis@jhu.edu; andreou@jhu.edu).

Marios Sophocleous and Julius Georgiou are with the Holistic Electronics Research Laboratory, Department of Electrical and Computer Engineering, University of Cyprus, 1678 Nicosia, Cyprus (e-mail: sophocleous.marios@ucy.ac.cy; julio@ucy.ac.cy).

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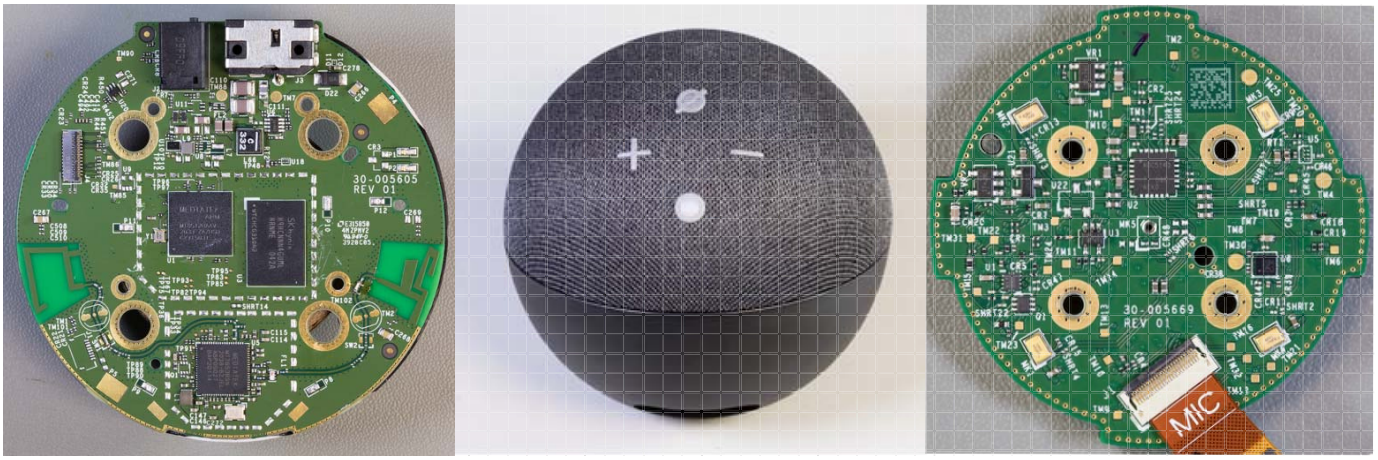

Fig. 1. The 4^{th} generation Amazon Echo, a smart appliance, exemplifies state of the art sensory system design. It is designed around standard industrial parts, for example microphones (sensors) and the TLV320ADC5140 Texas Instruments Quad-channel 768-kHz Burr-Brown audio analogue to digital converter [5]. Also, it includes a custom designed integrated circuit; the MediaTek processor, with embedded AI accelerator.

processor chips adds capabilities for local processing at the "edge" something that earlier generations of the device were lacking.

Key to the local processing in Amazon Echo, 4^{th} Generation is **insightful** information extraction as the signal proceeds to higher levels of processing. For example, questions that can be answered at the device itself through local processing: (i) *Is there something interesting in the environment*? -detection in a specific class of objects, is there a human or a pet in the room etc.,- (ii) *Where is it*? -localization- (iii) *What is it*? - identification, is that a human or a pet-. Recognition can proceed in the cloud using more complex models that include language in the case of speech recognition. The essence is about extracting a few bits of information at the right time and the right place, i.e. **in context**.

In this paper, we discuss trade-offs in sensor system engineering and give examples of practical design considerations and adopted solutions. To support the discussion, we provide extensive literature references to original sources from industrial system integrators and component manufacturers and classical textbooks to the topic. In Section II we summarize key fundamental concepts of information, information rate, and signal representations, where we also discuss noise models. The fundamental trade-off of "analog vs. digital" and power is also presented. Section III describes the architecture and its individual components of sensor systems emphasizing on specific trade-offs taking into account the theoretical foundations and fundamental concepts explained in section II. Section IV provides a brief overview of the most important characteristics and specifications needed when designing sensor systems. Sections V and VI are dedicated to provide implementation cases of sensor systems at the system level showing the trade-offs taken into account depending on the application.

II. Theoretical Foundations and Fundamental Concepts

Technology has evolved, but principles have not. Shannon's information theory [6] and communication theory enable the design of optimum systems using rigorous performance metrics. It also offers a principled approach to explore trade-offs in the design space. While most of the applications of information theory are in communications and coding, we have demonstrated its value in the design of microsystems [7], [8]. We have also applied the theory in the "microscopic" channel model for the transduction and processing in the blow-fly photoreceptor elucidating the physical mechanisms responsible for the limiting behavior of biological photoreceptors and the blowfly vision system [9].

The maximum number of bits per second, or channel capacity, of an analog channel is given by the following equation [6]:

$$\mathcal{C} = f_p \log_2 \left(1 + \frac{2P_{peak}}{\pi e N}\right) \tag{1}$$

where f_p is the bandwidth of the channel, P_{peak} is the instantaneous peak power of the signal, and N is the average power of the noise in the channel. Eq. 1 applies to linear systems under additive Gaussian noise conditions. It assumes a peak amplitude constraint, which is appropriate for sensors and electronic circuits that must operate within a certain physical transduction limit or voltage range to avoid distortion and clipping.

In sensory systems, the entire signal processing chain from the sensor, electronic interface/signal conditioning, and finally, data converter can be modeled as a cascade of linear channels in a network. The network architecture consisting of a series of point-to-point channels is mathematically tractable and provides a sufficiently rich framework for a wide range of applications.

Cascade Architecture The canonical channel model for a cascade channel architecture depicted in Fig. 2, is mathematically tractable and described by Equations 2 and 3 below. The signal power $X_n(f)$ at any stage n is transformed through a sequence of linear filters $\xi_i(f)$. The noise power $N_n(f)$ is the summed power of m independent, additive Gaussian noise sources $N_j(f)$ that are also transformed by sequences of linear

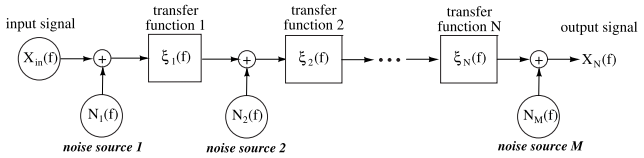

Fig. 2. Cascade architecture.

filters. Explicitly, the signal and noise at stage n are given by:

$$X_n(f) = \prod_{i=1}^{n} |\xi_i(f)|^2 X_{in}(f) \tag{2}$$

$$N_n(f) = \sum_{j=1}^{m} \prod_{i=k_j}^{n} |\xi_i(f)|^2 N_j(f) \tag{3}$$

where $X_{in}(f)$ is the power spectrum of the input signal, the noise $N_j(f)$ from independent source j enters at stage k_j, and the output signal is the last signal in the cascade $Y(f) \equiv X_N(f)$. The cascade network architecture was employed in conjunction with first principles physics and bio-physical models for the early visual system of the blowfly and silicon photoreceptors to determine their channel capacity and thus relate their functional performance to the implementation details [7]. In the cascade architecture of Fig. 2 one can extract information, and hence one could rigorously assess and evaluate trade-offs of intentional information extraction with respect to power, security, system complexity. In energy constraint systems such as smartphones and IoT, sensory systems deal with the efficient extraction of information from physical signals, such as sound, light, pressure. Hence, the design of the sensor subsystems often trades characteristics such as temporal resolution and spatial resolution SNR to power. A high information rate is the desired outcome of the processing, while the power consumption represents the cost. Hence, information rate divided by power is a reasonable metric where one often employs the optimizing criterion: maximize the number of $bits/sec/Watt$ or $bits/Joule$. Other cost measures are possible, such as size and weight, but they can often be related to the overall power consumption.

This section provides an overview of key ideas and concepts that have guided the design of sensor interfaces and sensory systems. Signal and Noise are fundamental to the design of systems. We review noise models with original references from the literature.

A. Physical and Electrical Signal Representations

Due to the significant advances in sensor technology and electronic circuitry, a more contemporary and comprehensive description of signal representation at the system level is necessary, and it is depicted in Fig. 3 where we also include the traditional analog and digital representations.

The four quadrants represent the four different types of available signals. Historically, analog signals, such as those coming from a photodiode, have been considered continuous in time and value (CVCT).

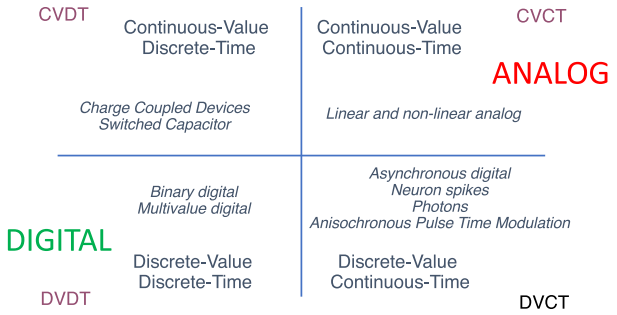

Fig. 3. Signal representation of physical and electrical quantities.

However, advanced sensors are today capable of detecting single photons [10], single biological molecules, or single neuron spikes. In those cases, although the time is still continuous, the physical signal value from the sensor is discrete. In the example of single-photon detectors as observed in Fig. 7 and Fig. 8 in [11], a single event in value is observed at a specific point in time; hence the value is no longer continuous (DVCT). On the other side of the spectrum, there are situations that the value of the signal is continuous, but the time is discrete, like the case of a switched capacitor. Even though the output value is continuous, the switches cause time quantization, and therefore the time is no longer continuous (CVDT). The remaining quadrant is the classical digital signals, both discrete in value and time. This kind of physical and electrical signal representation is a more comprehensive representation of the sensory systems of the 21^{st} century and provides a more accurate signal categorization, which is of immense importance when designing sensor interfaces.

Fig. 4 depicts a plot of signal to noise ratio (SNR) vs. power for an analog (Continuous Value Continuous Time-CVCT-), sampled data (Continuous Value Discrete Time-CVDT-), and a digital (Discrete Value Discrete Time-DVDT-) systems. Using the equations from [12], [13] the analog and sampled data system power consumption as a function of desired SNR is given by Eq. 4 and 5, respectively:

$$P_m = 4kTf_pSNR_{CVCT}[1 - \frac{f_s}{f_p} arctan(\frac{f_p}{f_s})] \tag{4}$$

and

$$P_m = 2kTf_pSNR_{CVDT}[1 - sinc(2\pi \frac{f_p}{f_s})] \tag{5}$$

For the digital system, the corresponding equation is:

$$P_m = \frac{kTf_s}{2} \log_2(1 + SNR_{DVDT})[\text{erfc}^{-1}(\frac{\epsilon}{4SNR_{DVDT}})]^2 \tag{6}$$

These equations are derived for idealized systems operating at the thermal noise limit.

The derived fundamental minimum power limit for CVCT and CVDT is somewhat problematic because every 10 dB increase in SNR incurs a ten-fold increase in power. This fact applies to amplifiers, filters, relaxation oscillators, and Analog-to-Digital Converters (ADC) because the analog part of the ADC is subjected to this constraint. Note that the derived equations in Fig. 4 are technology independent.

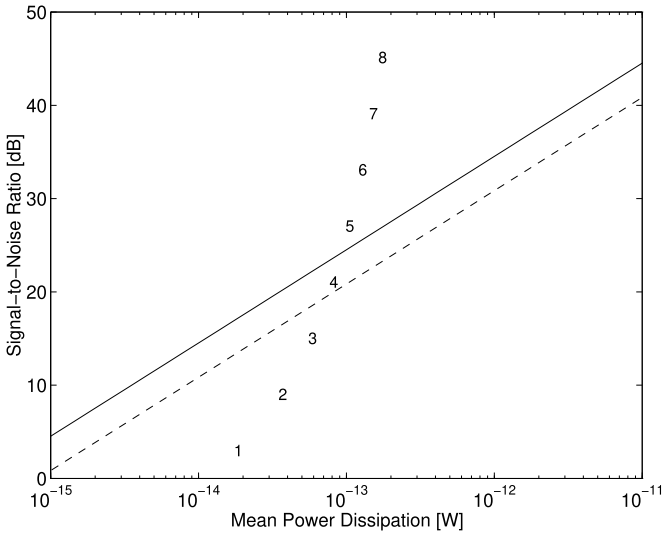

Fig. 4. Signal-to-noise ratio as a function of mean power ($f_p = 0.5 f_s = 100$ MHz, $\epsilon = 1E-12$). CVCT (analog) solid, CVDT (analog sampled data) dashed, DVDT (digital) number of bits.

Fundamental System Design Trade-off: Fig. 4 allows a system designer to explore a fundamental trade-off in sensor system design. The question often asked is how much of the processing can be conducted in "analog" and how much in "digital" (digital in this case is synonymous with DVDT). If energy efficiency is a design criterion, there is a crossover where DVDT processing is advantageous over CVCT "analog" processing. The three plots in Fig. 4 suggest that for low S/N, analog and analog sampled data circuits are more efficient than digital with the breakpoint at about 4 to 5 bits. Hence signal models and noise models are necessary to explore such fundamental trade-offs.

B. Noise Models

Noise is any unwanted information reducing the quality of the signal and, hence, setting a limit of the minimum level of a detectable signal. Although noise behavior is random, since the instantaneous amplitude is typically unpredictable, it can often be modeled as a Gaussian random process. Each component in the system introduces noise. Despite the randomness, most noise sources in circuits exhibit a constant average power. Although each application can face multiple noise sources, from a device level perspective, the noise can be either inherent due to the system components or external due to environmental interference [14].

The input-referred noise (e_n) of a device is a theoretical measure of the total device noise and allows comparison between different components, for instance, sensors, operational amplifiers, and transistors. Noise Spectral Density (NSD) (denoted $S(f)$) of a random noise signal is equal to the average normalized noise power over a 1-Hz bandwidth, in units of $(\frac{V^2}{Hz})$ for a voltage noise spectrum and units of $(\frac{A^2}{Hz})$ for a current noise spectrum. The voltage spectral density, $V_n^2(f)$, and the current spectral density, $I_n^2(f)$, are often referred to as the *Power Spectral Densities*. Since the operation of the system is for a specific frequency range, the integration of the noise density can be extracted for that region constituting the V_{rms} value. Because the dominant noise is thermal, a simplification of the calculation can be achieved by using the area of a rectangle; the height of noise density level for thermal noise for the frequency range of interest as explained in Eq. 7:

$$V_{rms} = e_n \cdot \sqrt{\Delta f} \tag{7}$$

For example, if the $e_n = 5\ nV/\sqrt{Hz}$ for a 10 kHz bandwidth, then $V_{rms} = 500\ nV$. This is a result of using an ideal filter to constrain the bandwidth of interest. A more accurate estimation should also include the filter's effect, which does not provide a brick-wall response.

Thermal noise is produced from the random thermal movement of electrons within a conductor. The noise in a resistor, also known as the *Johnson noise* is given by Eq. 8:

$$S_I(f) = \frac{4kT}{R} \quad [A^2/Hz]. \tag{8}$$

where k is the Boltzman constant (J/K), T the temperature (K), R the resistor value (Ω).

Shot noise describes the fluctuations that arise in a current crossing a barrier in which the discrete charge carriers pass independently of each other. The general model for shot noise is:

$$S_I(f) = 2\ qI \quad [A^2/Hz], \tag{9}$$

where I is the current through a potential barrier (A). For example, the noise in a photodiode detector is given by Eq. 9.

1) Thermal Noise in MOS Transistors-Above the Threshold: The thermal noise spectral density of a Metal Oxide Semiconductor (MOS) transistor [15] is constant as a function of frequency, which classifies it as a *white noise*. In the saturation region of operation, the thermal noise in a transistor is given by:

$$S_I(f) = 4\ kT(\frac{2}{3}gm) = \frac{8kT\,g_m}{3} \quad [A^2/Hz]. \tag{10}$$

while in the Ohmic region is:

$$S_I(f) = \frac{4kT}{R_{fet}} \quad [A^2/Hz], \tag{11}$$

where g_m is the intrinsic transconductance (Siemens) and R_{fet} is the resistance of the MOS device in the ohmic regime (Ω).

2) Thermal Noise in MOS Transistors-Below Threshold: In MOS transistors operating below the threshold, the white noise is often modeled as a *shot noise* source. For a MOS transistor in subthreshold saturation, I_d is the drain current (A), and the noise current spectral density is simply:

$$S_I(f) = 2\ qI_d \quad [A^2/Hz], \tag{12}$$

In ohmic subthreshold operation, the decrease in V_{ds} signifies the rise of an additional barrier between drain and channel, and the noise was shown [16] to approximate twice the value of Eq. 12:

$$S_I(f) = 2\ qI_d(1 + e^{\frac{-V_{ds}}{V_t}}) \quad [A^2/Hz]. \tag{13}$$

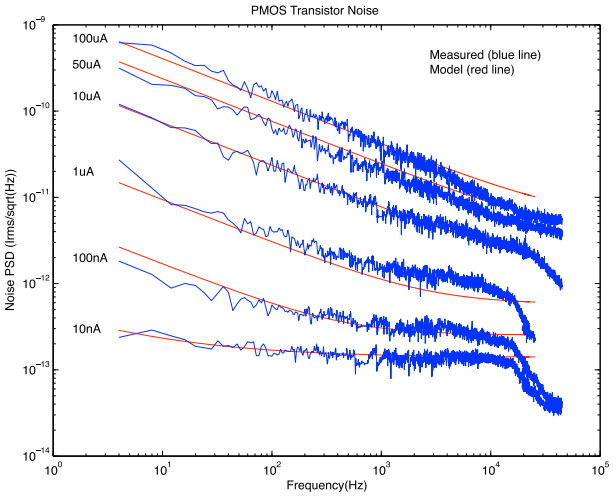

Fig. 5. Typical noise characteristics for a p-type MOS transistor. At low currents -low bandwidth- the device operates in sub-threshold region and the noise is thermal noise. At higher currents (above threshold operation) flicker noise dominates. For the data shown here $K_f = 3.12 \times 10^{20}$ and $A_f = 0.99$.

3) Flicker Noise in MOS Transistors: In MOS devices, flicker noise occurs due to electrons trapping at the Si-SiO_2 interface. This noise type relies highly on the fabrication technology. Flicker Noise, also known as $1/f$ noise because of its frequency-dependent characteristic, dominates at low frequencies and is more significant in transistors operating with larger bias currents and smaller gate area [17]. It is characterized in both the saturation and ohmic regions, at above and below current threshold levels, as it can be obtained from Eq. 14:

$$S_I(f) = \frac{K_f g_m^2}{C_{ox} W L f^{A_f}} \qquad [A^2/Hz]. \tag{14}$$

where K_f ($10^{-25} V^2 F$) and A_f (unitless and typically 1) are process-dependent parameters, C_{ox} is the gate oxide capacitance (F), W and L the width and length of the transistor respectively.

Fundamental Design Trade-off: Fig. 5 allows a system designer to explore a fundamental trade-off in amplifier design that could be part of the sensor signal processing chain in chip level designs (ASICs). For a given bandwidth, one necessitates the devices to operate at a given current. One can bias a single transistor above the threshold where $1/f$ noise dominates or employ multiple transistors in parallel to get the desired current while operating in a sub-threshold where the "excess" $1/f$ is minimal. The added bonus when doing the latter is that the overall thermal noise is reduced by approximately a factor of $\sqrt{N}$ where N is the number of MOS transistors in parallel. This trade-off attains lower overall noise at the cost of added complexity and area. Reducing the input equivalent noise can be accomplished using discrete components for board-level design by connecting devices in parallel and summing the currents from individual transistors or operational amplifiers through a resistor summing network [18]. Moreover, lower mobility in pMOS transistors is also translated into lower flicker noise compared to nMOS, which can be up to two orders of magnitude [19].

4) kT/C Noise: The sum of all of the thermal noise fluctuations in all transistors of a given circuit over the entire frequency spectrum is simply equal to the value $\frac{kT}{C}$. Using the Equipartition Theorem of Statistical Mechanics, one can define the voltage on a capacitor as a degree of freedom of the system (since its energy is equal to $\frac{CV^2}{2}$), i.e., the energy stored in the variable V is proportional to V^2. Each degree of energy of the system has a fluctuation energy of $\frac{kT}{2}$; therefore, the voltage noise in a system with a single capacitor, which equals the mean square fluctuation of the voltage (ΔV^2), is:

$$\frac{C\Delta V^2}{2} = \frac{kT}{2} \tag{15}$$

or

$$\Delta V^2 = \frac{kT}{C} \tag{16}$$

This result indicates that the total thermal noise in a system is determined only by the temperature and capacitance of the system. Since the resistance is directly proportional to the noise per unit bandwidth but inversely proportional to the system's bandwidth, the total noise (the product of these two quantities) is independent of R.

The $\frac{kT}{C}$ value is generally accepted as the expected noise power of any capacitive circuit connected to a capacitor. However, as shown in [20], the analysis that leads to it only holds for the steady-state case. Therefore, in circuits such as Active Pixel Sensors in CMOS imagers with a reset transistor operating in sub-threshold for which this condition is not met, a temporal analysis of the noise is more appropriate and will yield an expected noise power of less than half the $\frac{kT}{C}$ value.

5) Electromagnetic Interference (EMI): The external noise or electromagnetic interference (EMI) can be transferred either from an external device (source) to the device under test (victim) or in between sub-circuits of the same instrument. As for the different devices, unintentional energy is radiated through electromagnetic fields inducing noise in the receiving device. As for the same device, the noise can be coupled in a conductive way or through capacitive and inductive coupling, also referred as crosstalk. The conducted noise occurs between connected wires, such as those picking up the measured signal. Crosstalk can occur between unconnected wires placed in parallel creating high values for parasitic capacitance and mutual inductance. Based on the activity and signal strength of the signals, these wires can induce noise from one to another. Typical noise sources of EMI within the same device can be the power supply wires and switching DC/DC converters. Excellent discussion on proper design practices can be found in [14] and [21].

6) Fabrication Technologies Noise Constraints: The chosen fabrication technology can define the component characteristics required for each application.

Fabrication Technologies related Trade-off: Fig. 6 shows the relationships between input-referred noise, power and input bias current for three common Operational Amplifier technologies. Hence, the choice of fabrication technology depends highly on the application specifications and constraints. Table I shows these technology characteristics in a tabulated format. Depending on which characteristic is the most important for

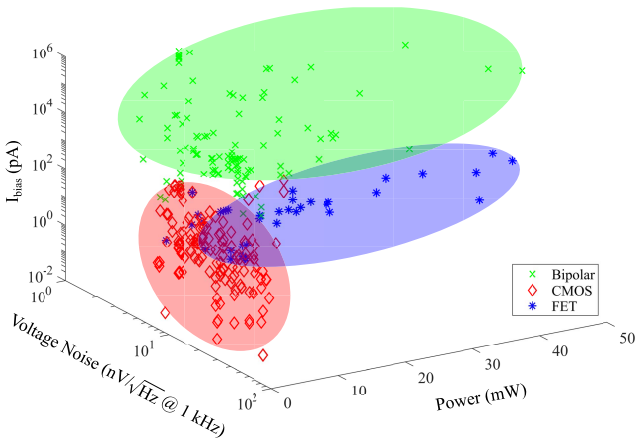

Fig. 6. Current technology characteristics of operational amplifiers. This figure is generated by extracting the relevant information from data sheets of commercial operational amplifier manufacturers.

TABLE I
CHARACTERISTICS OF OPAMP TECHNOLOGIES

Technology	Power	I_{bias}	Noise
CMOS	Very Low	Mid-High	Very High
FET	High	Very Low	Low
BJT	Mid	Very High	Mid

the specific application, one can wisely choose the most appropriate technology. For example, CMOS technology is the most attractive if interested in extremely low power, but the noise is not of major concern.

III. SENSOR SYSTEM ARCHITECTURE AND SUB-SYSTEMS

Throughout the years, typical systems available in the market shrunk in size dramatically, moving from occupying an entire room (IBM 7700) in the '60s to having the size of a US quarter (STM Sensortile) today. Sensor systems did not just evolve in terms of size but also in terms of capabilities and performance. The definition and understanding of the aforementioned theoretical foundations and fundamental concepts allowed the design of such systems to be more precise, minimize noise levels, accommodate multiple sensors whilst decreasing in size and cost. Traditionally, sensor systems are partitioned into the Sensor itself, an Analog Front End (AFE), a Digital Back-End (DBE) with an additional Power Management (PM) subsystem present in autonomous and wireless sensory IoT applications, as for example in [22].

- **Sensor**: The sensors transform the physical quantity of interest into an electrical signal. Depending on their output, sensors can be separated into direct and modulated. Direct sensors produce a direct electrical output such as voltage or current. Modulated sensors change their electrical properties, and modulation is required to extract that information.
- **Analog Front-End (AFE)**: This subsystem is the electronic interface to the sensor itself. It includes electronic circuits that are designed to match the physical characteristics of the sensor as well as provide appropriate excitation, bias, and auxiliary signals necessary for converting the energy in the physical signal efficiently and with minimal additional noise into the electrical signal. The final step in a typical AFE is quantizing the electrical signal and encoding it into a physical interface for transmission to the systems for storage and processing.
- **Digital Back-End (DBE)**: This functional block takes as input the data obtained from the AFE that are encoded into a serial physical interface (for example the Serial Peripheral Interface -SPI-) to an embedded processor to facilitate storage in digital media, and extract information either locally or in the cloud. Hence, DBE often incorporates physical radio interfaces such as Bluetooth, WiFi, Near Field Communications, etc.
- **Power Management (PM)**: This functional block is an essential subsystem of autonomous and wireless sensory systems, such as [23] and includes circuits for energy harvesting, storage, and power conditioning.

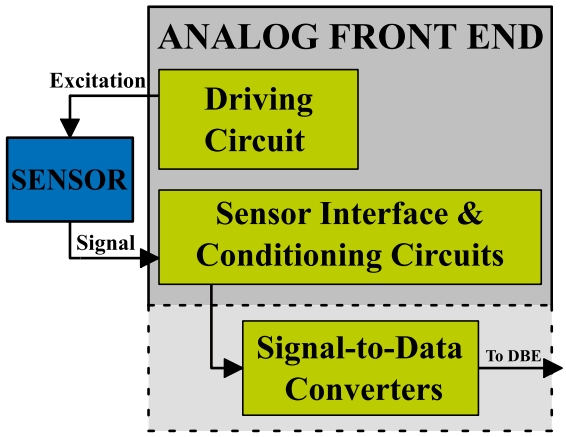

Fig. 7. System level description of a typical sensor system.

AFE is defined as the subsystem that converts the physical signals from the sensor into a symbol that can be processed in the DBE of the sensor readout system. AFEs can vary in architecture, but almost always, they include the following building blocks (Fig. 7):

- **Driving or Excitation Circuits**: Driving or Excitation circuits are responsible for providing the sensor with the required signals, i.e., drive the sensor, mostly in cases when the sensor is modulated and only changes its electrical properties under certain electrical conditions. These circuits can be similar for various sensors that operate under the same principle. However, optimization is of the essence when their specifications can affect the sensor's performance.
- **Sensor Interface and Conditioning Circuits**: These circuits are a critical component of the AFE. They are very specific to each sensor type, and they are even more specific to the actual sensor used and the application of the system. The measuring circuits focus on converting the change in the sensor's electrical properties (if the sensor does not provide an electrical signal on its own) into an electrical signal. Since signals from the sensors are generally small, a significant amplification is required. Amplification can be challenging since boosting a noisy

signal can also add further noise that can significantly deteriorate the measurement quality.

- **Signal-to-Data Converters**: A collection of circuits that is mostly analog whose function is to quantize the electrical signals into a representation that is robust to communication over a long distance. While ADCs are often used in this subsystem, other forms of quantization such as Pulse Density Modulation are also used, which has shown significant improvement in the resolution and accuracy of the measuring circuits. Although this block is not necessarily part of the AFE, it is included within the sensor front-end in most commercially available sensors, making it capable of providing digital output using specific protocols, such as I^2C, SPI, $RS485$.

A. Driving/Excitation Circuits

The first building block of the AFE is the driving or excitation circuits block. These circuits are highly dependent on the sensor type and principle of operation. Once the application requirements are defined in terms of what needs to be driven, the technical specifications and performance of the circuits should be defined. Driving or excitation circuits generate the required signals to send to the sensors. The clarity of the signals is of great importance for accurate measurements [24].

1) Voltage Sources: Multiple sensors require driving voltages of specific amplitude, frequency, and shape [25]. In some cases, voltage sweeps towards a specific direction might be needed, whereas in some special cases, a cyclic sweeping of voltages might be of interest [26]. It should be noted that in a sensor readout system, the DBE is responsible for knowing and deciding when to supply those driving voltages whilst the amplitude of them can be up to a point controlled directly by the controller or through the software [21].

Performance vs. Cost Trade-off: The simplest form of the voltage signal is the static Direct Current (DC) voltages. These voltages are in most cases supplied by the Digital-to-Analog Converter (DAC) from the DBE. This is important to know since this will be a valuable parameter for the selection of the DAC since higher resolution and accuracy of the signal mean a higher number of bits on the DAC and accuracy of the reference voltage inside the DAC [27].

Performance vs. Complexity Trade-off: In some situations where the sweeping or the rate of change of the voltage signals is low, the DAC might be capable of making these changes fast enough. When signals of arbitrary shapes are needed, the most common solution is using a function generator or an arbitrary waveform generator (AWG). Function generators and AWGs are usually designed to the Integrated Circuit (IC) level or as bench-top instruments [28]. Their operation is most commonly based on Direct Digital Synthesis (DDS), which is a method that takes digital signals and converts them into the equivalent analog signal shape. There is also the option of using Phase-Locked-Loops (PLL) to generate the required signal. However, DDS has superior frequency agility, lower phase noise, and more flexibility in controlling the output phase across the frequency spectrum [29]. Finally, since both the DAC and the function generator are not instruments designed to provide high currents, the signals are buffered to avoid voltage drops. These circuits are defined as dependent sources because the output relies on their input [30], [31]. There are two main categories of dependent voltage sources, the Voltage Controlled Voltage Sources (VCVS) and the Current Controlled Voltage Sources (CCVS). If the input of the circuits is voltage and that voltage defines the output voltage, then this is a VCVS, and when the input is current, it is a CCVS [32].

2) Current Sources: Similar to the dependent voltage sources, dependent current sources are separated into two categories: the Voltage Controlled Current Sources (VCCS) and the Current Controlled Current Sources (CCCS). Since the majority of DACs have voltages as output, most current sources are dependent sources [32]. DC current sources can be achieved using OpAmps, taking advantage of their fundamental property to equate the voltage at the two inputs when in a feedback configuration. An even simpler source can be realized by the use of a transistor in the saturation phase. However, high accuracy sources might be of more interest to sensor driving circuits [33]. Alternating Current (AC) current sources, on the other hand, are much more difficult to achieve. The most popular approach to designing an AC current source is VCCS, and the reason is that the generation or arbitrary voltage signal, as explained above, is achievable using a signal generator.

Load Range vs. Bandwidth Trade-off: VCCSs can be realized by employing multiple discrete components or a single Application Specific Integrated Circuit (ASIC). The general performance of ASIC-based VCCS dominates both in terms of bandwidth and maximum driving load reaching up to 100 MHz and more than 20 MΩ, respectively. These two parameters are probably the most important ones when trying to identify the optimum approach to choose. It should be clarified that current sources are circuits that auto-adjust the voltage on the load to maintain the chosen current. Hence, power supplies of the circuits come as limitations on this for high current, and high loads [30], [31], [33].

Performance vs. Complexity vs. Power Consumption Trade-off: Fig. 8 illustrates three popular AC VCCS circuits. The top three - Fig. 8 (a), (b), (c) - are all based on the Howland current source, which is considered to be of high accuracy and high-quality factor. The input is an AC voltage signal, and the ratio of that input to the value of the resistor gives the current amplitude to the load. Fig. 8 (a) depicts the basic configuration of the Howland current source whilst Fig. 8 (b) and (c) show the improved versions of the same. The extra resistor in the feedback loop can be utilized to balance the bridge more optimally, while the OpAmp in the top right circuit is used to increase the impedance of the loop and force the current through the load. Fig. 8 (d) and (e) depict the Tietze Current Source and the load-in-the-loop Current Source, respectively. The main disadvantage of the load-in-the-loop is that although it is simple, it becomes unstable with capacitive loads. Additionally, in all of the aforementioned Current Sources (CS), the choice of components is vital [34]–[37]. For example, in all three CS, the amplifier is assumed to be ideal; however, only if the OpAmp's characteristics are chosen carefully, this assumption can be valid. Some important OpAmps characteristics for CS are high input impedance, low input

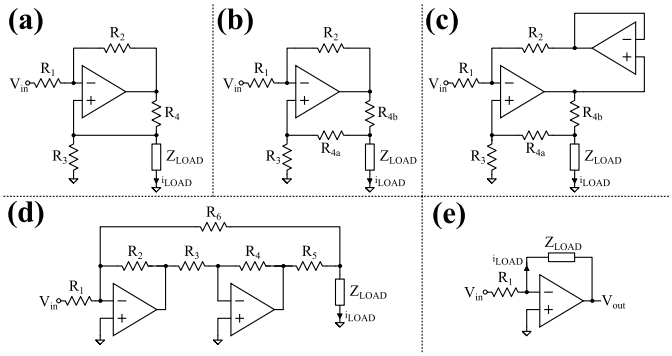

Fig. 8. AC current sources (a) Howland current source-inverting (b) Improved howland current source-inverting, (c) Improved howland current source-dual inverting, (d) Tietze current source, (e) Load-in-the-loop current source.

bias current, and voltage offset, while the bandwidth should be sufficient for the application's frequency range. Additionally, the resistor values should be optimized for the application with less than 0.1% tolerance. Higher values decrease power consumption and improve load range, while lower values decrease thermal noise. All of these Voltage-mode VCCS can reach up to 50 MΩ of output impedance when the bridge is appropriately balanced, and the load can be both grounded or floating [38], [39].

B. Measuring Circuits

The most typical electrical parameter driven to the signal-to-data converter is voltage. Hence, in almost all cases, the preferred output of any measuring is voltage. However, due to the wide range of available sensor types and operating principles, measuring circuits are required to convert several electrical parameters of sensors into a voltage signal. This can be achieved using a plethora of measuring circuits with their inherent trade-offs [40]. Thus, the selection of the proper circuit is a challenge.

Single vs. Multistage Amplification Trade-off: Since sensor signals are generally very low, there are situations that a single OpAmp might not be able to provide enough amplification and a cascade of OpAmps need to be used [14], [25]. Attention must be paid to the resulting bandwidth when cascaded amplification is employed. Multistage is usually used to expand bandwidth since the gain of each stage can be lowered, hence increasing bandwidth with a constant Gain Bandwidth Product (GBP). On the other hand, multistage gives higher power consumption and higher noise in comparison to a single-stage cascode topology. The downside of the single cascode topology is the output voltage swing and high output impedance; hence a second stage is introduced with lower gain, higher output voltage swing, and lower output impedance. Moreover, multistage introduces stability problems and may require to increase the distance between the poles in order to have enough phase margin [41]. However, the Noise Figure [42] of cascaded circuits is mainly affected by the noise of the first stage. Hence, if the signal has low amplitude, the first stage of the measuring circuit is a low-noise amplifier, also called pre-amplifier. Pre-amplifiers are responsible for signal amplification and increasing the SNR of the signal by adding the minimum possible intrinsic noise to the inevitable sensor noise. Hence, the noise parameters, RMS and peak-to-peak should be used and be comparable and lower to the corresponding noise measures of the sensor. With multistage architectures, one has to beware of input offset propagation issues that may saturate subsequent amplifiers if the appropriate offset removal techniques [43] are not employed.

1) Voltmeter Circuits: Voltmeters are one of the simplest measuring circuits depending on multiple input signal characteristics such as voltage range, signal to noise ratio, noise bandwidth, signal frequency and bandwidth. In almost all cases, sensor signals range from several hundreds of millivolts down to the picovolts range. Apparently, a significant amplification is required. The simplest way to amplify a sensor signal is to use a voltage amplifier in a negative feedback topology in inverting and non-inverting configuration. These two configurations can be used when a single point's voltage is measured and compared to the ground [24].

Numerous sensors require the measurement of the voltage difference between two points when none of them is grounded [44]. This case is significantly different from the previous one. The most common technique to measure the potential difference between two points is the Instrumentation Amplifier (IA), when a single output is required. They are usually constructed from three OpAmps, and a single resistor defines the gain of the IA, R_{GAIN} that can either be externally changed or some ICs have internal resistors that the designer can choose [45]–[47]. A major advantage of using IAs, is the extremely high Common Mode Rejection Ratio (CMRR). CMRR is the ability of the IA to cancel out any signal common to both input terminals; hence common external noise to the two inputs is automatically removed. CMRR is frequency-dependent and decreases as the frequency increases. Hence, this characteristic of the OpAmps is essential, especially at higher frequencies. Moreover, it has to be noted that OpAmps configured in the non-inverting configuration produce higher output offset voltage due to the CMRR, whilst the output offset voltage is lower in the inverting configuration. Another option is the difference amplifier, which is part of IA and similar to the inverting amplifier. However, the positive input of the OpAmp has a potential divider to the ground, and the gain of the circuit now takes into account the input voltage of the positive terminal [48]. There is also the option of using a fully differential amplifier capable of measuring the difference between the two inputs but has two outputs where each one is the exact opposite of the other.

IA vs. Difference vs. Fully Differential Trade-off: The application specifications govern the decision as to which circuit to use. The difference amplifier is a mainstream and low-cost circuit but is limited in terms of input impedance (≈1 GΩ) and bandwidth (≈10 MHz depending on the parasitic capacitance of the feedback loop) and from the fact that the two inputs of the OpAmp might have different input impedances affecting the measurements. Fully differential amplifiers have a much higher bandwidth (>100 MHz) but suffer from even lower input impedances (≈100 MΩ) and the mismatch of input impedance at the two terminals [49].

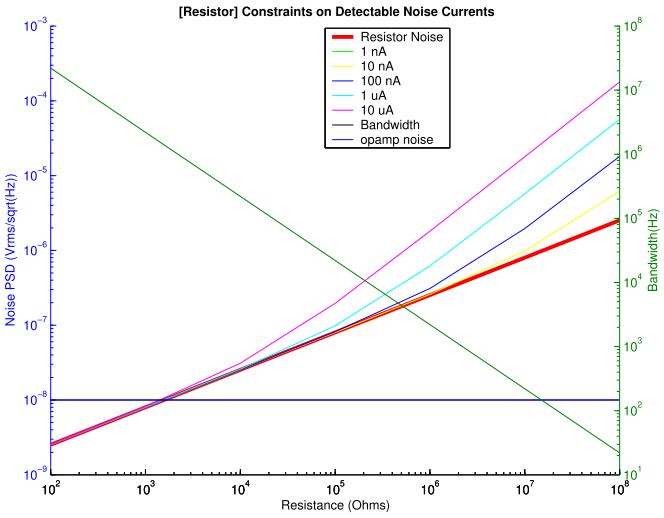

Fig. 9. Noise PSD (left) and Bandwidth (right) trade-offs as a function of the resistor in ammeter circuits.

IAs are probably the best approach to most sensing applications since they have the highest input impedance from all three (up to 10^{15} Ω), they have matched input impedance for both inputs, since the inputs are directly connected to the positive inputs of the two OpAmps inside it, but it is constrained in the bandwidth. Commercially available IAs can reach up to 10 MHz in bandwidth at most [47].

2) Ammeter Circuits: The second most common electrical parameter measured out of a sensor is current. Similarly to voltage, current characteristics can define the specifications for the AFE. The simplest version of an ammeter is the shunt ammeter [24]. This topology can only be used towards the ground.

Input Impedance vs. Noise Trade-off: In cases where the current must be measured at the high side, other approaches should be adopted. The simplest approach is the differential amplifier. However, this method has a major disadvantage: the circuit's input impedance depends on the resistor values used in the circuit, which implies a major trade-off. Higher resistance values give higher input impedance and hence higher accuracy. However, thermal noise is simultaneously increased, and ultimately the noise performance of the circuit is not limited by the baseline voltage noise of the OpAmp but rather by the external components. As the resistance increases, the thermal voltage noise contribution of the resistor increases, potentially swamping the thermal noise contribution of the sensor. From this perspective, one would be inclined to use even larger resistors to measure smaller currents; however, because of the capacitances implicit in the circuit, a large R can severely limit the bandwidth of the measurement. This trade-off is depicted in Fig. 9.

Linear vs. Logarithmic Trade-off: Other approaches to improve the performance of the measuring circuits are the use of a capacitor instead of a resistor in the feedback loop as shown in Fig. 10 (a). In some cases, the input resistor is also replaced by a capacitor to lower thermal noise with the expense of only measuring AC currents. However, in such cases, the designer should focus on eliminating any DC current flowing through the capacitor as it will saturate the OpAmp [50]. Moreover, in situations where a much wider current range needs to be measured, logarithmic topologies using diodes can also be used at the expense of lower sensitivities, as shown in Fig. 10 (b).

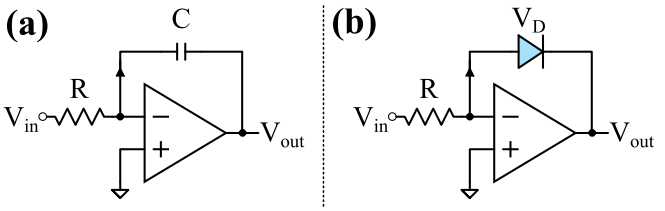

Fig. 10. Ammeter topologies: (a) Capacitive feedback ammeter, (b) Logarithmic feedback ammeter.

C. Signal Conditioning

1) Filtering: Filtering is the stage of removing the unwanted elements from the signal under interest, which are considered noise in a frequency-dependent manner. Filters are generally placed after the measuring circuit stage to suppress the noise in the frequency bands of no interest to increase the signal-to-noise ratio. The passband is the frequency region where the signal remains intact while the stopband is removed. The transition band is the in-between frequency region where the power intensity of the signal is attenuated moving from passband to stopband. For an ideal filter, this transition is sharp, brick-wall response, the passband has a fixed amplitude response, and the stopband is zero. A real filter tries to approximate this response with multiple trade-offs, such as passband flatness, roll-off rate, and pulse-response fidelity. The frequency where the attenuation is half of the intensity of the passband region (3dB point) is the cut-off frequency (f_c). The response curve shows the filter behavior using the attenuation ratio (V_{out}/V_{in}) versus frequency. Based on the pass and stop bands formation, the filter types are:

- low-pass/high-pass: passes/rejects and rejects/passes frequencies lower and higher than the selected cut-off frequency, respectively.
- band-pass/band-stop (notch): allows/rejects frequencies within a specific range and rejects/allows the region outside it.

a) Quality factor: The quality factor Q of a filter measures the filter's ability to select the frequency range where the information is included. A low Q filter provides more bandwidth and smooth roll-off, while a high Q has a peak in the area of the cut-off frequency leading to a sharper roll-off and, thus, to a more selective filter. The order of filters in a cascaded scheme can rely on the Q per stage. For example, the high Q filter should be set first with a decreasing order in the next stages in low-noise designs to provide the sharpest roll-off in the beginning. For a general-purpose design, the Q should be in increasing order to initially provide an attenuated version of the signal. So, any increase in the following stages will not pose any concern for a larger voltage supply range to avoid clipping.

b) Group Delay: Group delay is the time that a signal takes to pass through a device. Since the signal consists

of multiple sinusoidal components based on Fourier Theory, it can be defined as the change in phase over the corresponding frequency range. If the delay for each component is different, then the signal is distorted. Thus, a constant group delay is an essential consideration during the analog conditioning and the digital filtering steps.

Analog vs. Digital Filtering Domain Trade-offs: The filtering can be conducted in both analog and digital domains. Analog and Digital filters can both attenuate the noise, but their behavior is not equivalent. Their use is based on the application. Analog filtering operates before the ADC, setting the system requirements. More specifically, an anti-aliasing filter is only available in the analog domain. Setting a cut-off frequency that keeps the signal's information minimizes the requirements for conversion and data acquisition. Other uses are as dc block (high pass filter) or bypass (low pass filter to the supply) bypass. On the contrary, digital filters can approach the ideal specifications and accuracy of any response curve. Digital filtering is programmable, relying on the filter coefficients and processor clock speed. The result is repeatable, whereas the analog filter characteristics rely on the components' variability, environmental effects, and aging. A digital class of filters, finite impulse response (FIR), provides constant group delay. This can also happen for analog (Bessel), but this characteristic is not inherent as for the FIR. Moreover, digital has an inherent delay. The preference of analog filters is not related to their performance but as a function that the digital cannot provide. They are used complementarily to the digital filters and lower their complexity.

Passive vs. Active Filters Trade-offs: The analog filters can be categorized as passive or active based on the utilized components used in their construction. The passive filters incorporate only passive components (resistors, capacitors, and inductors), whereas the active ones also include operational amplifiers (OpAmp) but not inductors, leading to more compact designs. In contradiction with passive, the active filters dissipate power and can drive other stages due to the low impedance of the OpAmp. In addition, the active filters have the ability of signal amplification, while the passive reduces the signal's energy. The passive filters are less complex in design. Active filters have an upper limit which is related to the OpAmp's bandwidth. On the other hand, passive filters theoretically have no limitation, but due to parasitic capacitance and inductance, there is an upper limit too, which can be hundreds of MHz. As for the lower limit, the active filters can approach a frequency close to 0 Hz. As for system-level, active filtering is employed for signal conditioning, and passive can be used for voltage regulation and harmonic elimination.

Sallen Key vs. Multiple Feedback Trade-offs: Active filters can vary from a simple RC to more complex topologies separating them into single-pole or multi-pole filters. Cascading single-pole filters attenuate the signal level in the area of interest. Thus, multi-pole filter topologies are preferable in reducing this effect and approach a more ideal behavior and sharper roll-off. The values of the components can provide more flexibility in adjusting the curve in the mid-range frequencies. The most popular two-pole filter topologies are Sallen-Key (SK) and Multiple Feedback (MFB) [51]. Fig. 11 shows the schematics for the two topologies in low filter configuration. The MFB topology is insignificantly affected by component variations, can provide amplification along with filtering but inverts the signal. Oppositely, SK is selected as a unity-gain filter and is resilient on the OpAmp non-idealities.

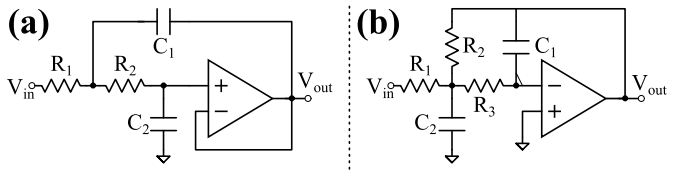

Fig. 11. Lowpass active filter topologies (a) Sallen-key and (b) MFB and bandpass filter.

Active Filter Type Trade-offs: The aforementioned topologies will have a specific response based on the selected components. The designer should specify the requirements of the filter in the digital domain, such as passband flatness, the upper bound of stopband region and cut-off frequency, and time-domain response, which incorporate multiple trade-offs. There are three main types of responses:

- *Bessel*: constant group delay for all the area of interest and, hence, a pulse response without overshoot or ringing. This benefit comes at the penalty of increased attenuation in the passband, importantly earlier than the cut-off frequency.
- *Chebyshev*: the sharpest roll-off as a trade-off for a rippled passband attenuation and highly nonlinear phase. The number of cycles of ripple in the passband is equivalent to the filter order.
- *Butterworth*: the flattest attenuation behavior passband region, which comes at the expense of a reasonably wide transition region.

Fig. 12 illustrates the behavior for 6^{th} order filter from each category for a cut-off frequency at 10 kHz. These graphs show the extreme cases, but a mixture of characteristics can lead to the filter's response partially combining a Butterworth with one of the other two categories.

2) Multiplexing: There are cases where the same measuring circuit can be used for more than one sensor, or the sensor exists in the system multiple times. The AFE should be connected to multiple sensors on command from the DBE. This can be achieved with the use of analog multiplexers. Multiplexers are essentially high-speed, digitally-controlled switches that can connect a single input to multiple outputs, one at a time, which will depend on the control command. Additionally, multiplexers can use multiple inputs and connect to multiple outputs depending on the control commands. Currently, there are many commercially-available multiplexing ICs with different features allowing optimized designs. It has to be noted that specialized multiplexers are also available such as digital multiplexers and port expanders, i.e., $GPIO$, I^2C, SPI. Multiplexers can be employed either for multiple sensors using the same measuring circuit or as a way to isolate the non-operating sensors from the rest of the electronic circuits. The second case avoids any potential interference or unwanted current paths since the sensors are connected through the MUT in the case of multisensor arrays.

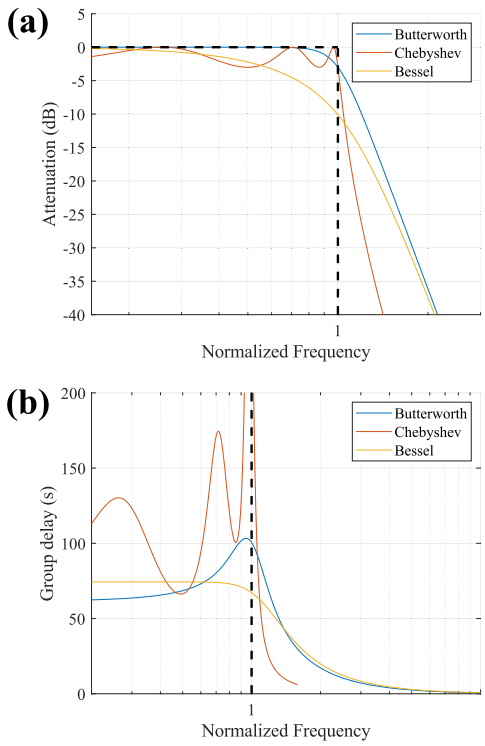

Fig. 12. Low-pass active filter response comparison: (a) Attenuation, (b) Group delay.

Performance vs. Size Trade-off: Analog multiplexers are digitally controlled switches to connect a specific sensor to the corresponding circuit. Several types of switches range from mechanical switches to Metal Oxide Semiconductor Field Effect Transistors (MOSFETs). Mechanical switches are bulky, slow and they significantly deteriorate with time. On the other hand, MOSFETs are small, fast, and have longer lifetimes. Both types of switches have low resistances when connected, not affecting the rest of the circuits; however, they have a major difference. Mechanical switches or relays feature several orders of magnitude lower currents when in the open position compared to MOSFET switches. This characteristic is of immense importance when multiple sensors are present, and leakage currents can cause interference between the sensors.

3) Isolation: Although power isolation is not the focus of this tutorial, there are cases where signal and ground isolation of the sensors on the AFE is highly important. Taking a multisensor array that includes several electrochemical sensors immersed in the MUT, signal, and ground isolation is a necessity.

Performance vs. Complexity Trade-off: Since all of the sensors are connected through the tested medium, they should be isolated from all parts of the AFE. There are several types of isolation of signals, such as optical isolation or mechanical isolation. Multiplexers can also be used as isolation, but they are not as effective as the mechanical or optical ones.

D. Analog to Digital Converter (ADC)

The conversion of the analog signal into digital is essential for further processing and storage of the information. Although the general trend of the AFE nowadays is shifting towards the direct conversion of the analog signal to pulse width modulation using either analog-based switching circuits or digital timers [52], [53], ADCs are still a common and important component of a sensor system. This section encompasses multiple considerations around this operation. The selection of the appropriate ADC depends highly on the sensor type, sensor, and application.

1) Sampling Rate & Aliasing Effect: The sampling frequency is the ADC's throughput and expressed in SPS. During sampling, a common issue is the aliasing effect, which is the misidentification of a signal frequency, meaning that the high frequency alias appears to be a lower frequency. As explained above, the signal is band-limited using filters to retain only the meaningful information. Based on the Nyquist–Shannon sampling theorem, a complete reconstruction of a band-limited signal can be achieved from its digital samples if the highest frequency is equal or less than the Nyquist frequency: $f_n = 2 \cdot f_{max}$ [54]. Thus, this filter can also be called anti-aliasing since it tackles that issue.

The realization of an RC filter with a sharp roll-off can conclude a high-order topology. Hence, a typical solution is to relax these constraints and sample at a frequency with a higher rate than the Nyquist (oversampling). A rule of thumb is to sample ten times higher than this constraint to achieve faithful reproduction of the original signal, especially for the high-frequency part of the bandwidth. Moreover, the high power intensity of the signal in the frequency spectrum can be in lower frequencies from the f_c, meaning there is no distortion in practice even in sampling at Nyquist frequency.

2) Resolution & Oversampling/Averaging: The ADC resolution is the number N of digital bits with the corresponding digitized levels to be 2^N. The least significant bit (LSB) is the smallest analog voltage required to cause a change in the digital output and is defined in Eq. 17:

$$V_{LSB} = \frac{V_{ref}}{2^N} \tag{17}$$

where V_{ref} is the analog reference voltage (V), with which the analog input signal is compared to generate the digital output. In other words, V_{LSB} is the minimum detectable analog value. The SPS encompasses the resolution information since the sample is typically the bits of the digital word.

If a higher resolution is needed, the oversampling and averaging technique can be employed at the cost of reduced throughput. Higher resolution ADCs are available at the expense of higher cost. Oversampling is sampling at a higher rate than Nyquist frequency and expressed as $f_{os} = K \cdot f_n$, where K is the oversampling integer. The resolution increase by W additional bits is related to $K = 4^W$. The resulted digital value ($D_{ov,av}$) for the K sampled values, D_{sam_i}, is expressed in Eq. 18:

$$D_{ov,av} = \frac{\sum_{i=1}^{K} D_{sam_i}}{2^W} \tag{18}$$

In other words, one sample is saved for every 4^W conversions. An additive benefit from this technique is the quantization noise reduction and can be effective when the noise is modeled as white noise since averaging reduces it significantly [55].

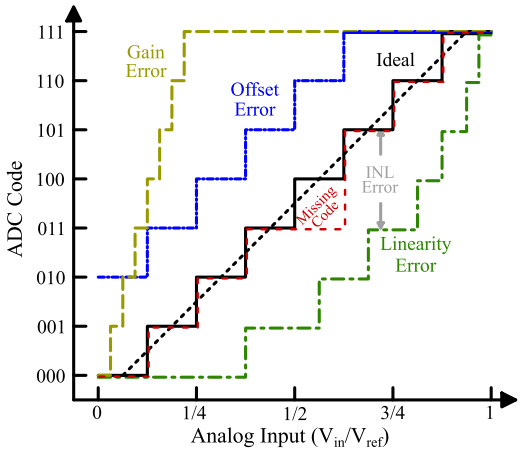

Fig. 13. Common transfer characteristics errors in a 3-bit ADC.

3) Accuracy: Accuracy is defined as the closeness of the measured value to the actual value. There are multiple metrics available to determine the deviation from the ideal operation. The ADC transfer function from analog to digital, as illustrated in Fig. 13, is the graph around which all the metrics are accessed [56].

Except for the metrics for DC accuracy, the effective number of bits (ENOB) is a measure of the dynamic range and can determine the accuracy of the measuring system [57]. Moreover, the SINAD (signal, noise, and distortion) is the ratio of the fundamental's frequency signal power level to the noise plus distortion power level. The maximum theoretically achievable SINAD of an ideal ADC, where ENOB is related equally to the resolution, is described in Eq. 19:

$$SINAD(dB) = (6.02 \cdot ENOB) + 1.76 \tag{19}$$

Thus, the resolution is related to the accuracy, but they are distinctly different. In practice, the SINAD and the ENOB can be estimated by supplying a sinusoidal wave to the whole system and extracting the FFT.

Performance vs. ADC Architecture Trade-off: The resolution and sampling speed of the application are the primary constraints to determine the appropriate ADC topology. Table II provides a comparison between the different ADC architectures showing the upper and lower bounds of each topology available in the market [58]. Another type of ADCs is the integrating or otherwise slope ADCs such as Dual-Slope and Multi-slope [59]. The basic idea of a single-slope ADC is to use an integrator to generate a sawtooth waveform and then compare it with the analog input using a comparator. A digital counter is used to measure the time taken for the sawtooth waveform to exceed the input signal voltage level. Integrating ADCs are mostly used when high resolutions are required; however, due to the time-based conversion, there is always a trade-off between resolution and response times since higher resolutions result in slow responses and vice versa. A similar type of ADC is the timer-based ADC. The most commonly used timer-based ADC is the 555 timer in an astable mode. Similar to the integrating ADC, the 555 timer generates a positive pulse while the pulse width is inversely proportional to the difference in voltage between the input and a reference

TABLE II
ADC ARCHITECTURES CHARACTERISTICS

Topology	Resolution (bits)	Sampling Rate (SPS)
ΣΔ	16 - 32	Slow to Medium (1 - 2M)
SAR	8 - 16	Medium (5k - 15M)
Pipeline	8 - 16	Ultra Fast (1M - 3G)

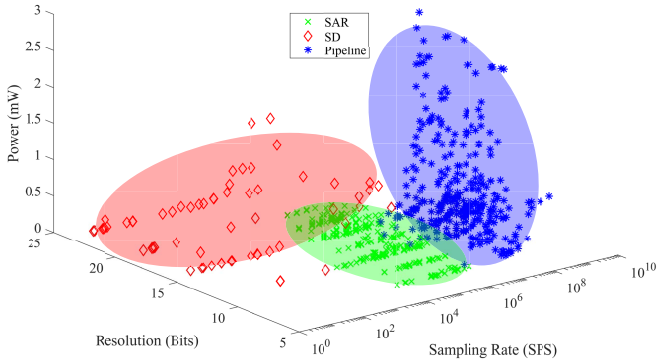

Fig. 14. Commercial ADC components features vs Architectures. This figure is generated by extracting the relevant information from data sheets of commercial ADC manufacturers.

at a charged capacitor. The most popular architecture is the Successive Approximation Register (SAR). The main reason is the underlying, highly efficient binary search algorithm implemented in hardware. It achieves low power consumption, high sampling speeds, and mid to high resolution.

The oversampling ADC family is commonly used for achieving noise shaping and high resolution. More specifically, $\Sigma\Delta$ ADC consists of a $\Sigma\Delta$ modulator and the digital filter. The modulation performs a higher sampling rate than the Nyquist rate. Thus, the quantization noise remains the same but spread in the broader bandwidth but reduced in the frequencies of interest. The modulator acts as a low-pass and a high-pass filter for the signal and quantization noise, respectively [60].

The Pipeline ADC can be selected when an ultra-high-speed sampling rate is essential. The high conversion speed is achieved using an N-step conversion, in which the residue per conversion is passed down from the previous stage. It can be considered more hardware efficient compared to Flash [61].

A comparison graph between commercial ADC specifications (Power, Sampling Rate, and Resolution) versus the architecture can provide an overview of the state of the commercially available components as depicted in Fig. 14.

Moreover, a typical figure of merit (FOM) [62] as defined in Eq. 20, can provide another quantifiable comparison for critical measures in between different architectures:

$$FOM(J/conv) = \frac{Power}{f_s \cdot 2^{ENOB}} \tag{20}$$

An alternative derivation of a FOM based on information theory was derived in [63] and explains the empirical data in the classical Walden paper [62].

E. Communication

1) Wired: There are multiple wired communication protocols for programming devices and acquiring data. The Serial

Peripheral Interface (SPI) and Inter-Integrated Circuit (I^2C) are the most commonly used. The SPI consists of four signals: chip select (CS), clock (SCK), Data Out (SDO), and Data In (SDI), based only on data direction or also based on the controller and peripheral to PICO and POCI [64]. Moreover, I^2C is also used and needs only two signals, Serial Clock Line (SCL) and Serial Data Line (SDA).

SPI vs. I^2C Trade-offs: Every I^2C device has a unique identification number (address) to achieve the communication. Hence, the data transfer does not include only the pure data. I^2C can be used in designs where minimum wire complexity is required or can withstand reduced bandwidth [65]. When higher speeds are required, a parallel transfer is a leading solution, in which each bit of the data word is using a pin. SPI can be used in a distributed network of sensors when control over the A/D conversion is required through the CS signal. The SPI's daisy chain configuration can be selected. The data are transferred from the register of one ADC to another. This fact allows data communication via one line at the expense of acquisition speed. Another option is to use the typical SPI controller-multi peripheral configuration, which is less complex at the expense of multiple digital ports for CS. Both setups are depicted in Fig. 15.

2) Wireless: The use of wireless communication has become a necessity nowadays since it eliminates the need for wired connectivity. They act as peripherals to a central unit to acquire the data for further processing.

Data Rate vs. Range vs. Power Trade-off: There are multiple options available, as outlined in Table III. There is a trade-off between the data rate, transmission range, network type, and power. Bluetooth is probably the most common wireless technology used, especially in closed spaces and when data transfer rates are relatively low. The most common application is sensor nodes monitoring air quality and environmental parameters. This technology is mostly favored when power consumption is important, usually in battery-powered sensing systems. In situations where higher data transfer rates are required, and a much higher number of nodes is needed, Zigbee is usually preferred. On the other hand, for extremely high rates, such as video transmission, WiFi is probably the best choice; however, the mesh network capability is not feasible, and it consumes much higher power. In applications where the range is the deciding factor, LoRa features a significant advantage compared to the other technologies. Since wireless transmission will be the highest portion of the power consumption, the decision should be application-specific for an optimized design.

F. Biasing, Power Source, and Management

Powering and proper biasing of the system's components are essential for the operation and longevity of the device. It is common to have multiple components operating in different voltage ranges and need a specific voltage as a reference. Battery-powered devices are safe, portable, and convenient in use, do not add hum noise, and can be ideal if not excessive power is needed.

1) Power Sources: Energy storage devices are components capable of storing energy and providing electrical energy when required. The most common type of energy storage is batteries. An electric battery is an electrochemical energy storage device consisting of one or more cells supplying "mobile energy" to electrical devices. Batteries can be classified as primary or single-use, which can only be discharged (irreversible chemical reaction), and secondary or rechargeable, which repeat the charge and discharge cycle (reversible chemical reaction) multiple times during a lifetime.

TABLE IV
SPECIFICATIONS OF VARIOUS BATTERY TECHNOLOGIES

Battery Type	Energy density (Wh/kg)	Voltage (V)
Lithium Ion	90–160	3.3 - 3.8
Lithium Polymer	130–150	3.7
Alcaline	85–190	1.5
Nickel-Cadmium	50–70	1.2
Nickel-Metal Hybride	70—100	1.2

TABLE V
POWER DENSITY FOR ENERGY HARVESTING TECHNOLOGIES

Energy Source	Technology	Power Density
Radio	RF	0.1 vW/cm^2
Mechanical	Piezoelectric Electromagnetic Electrostatic Triboelectric	0.1 mW/cm^2
Light	Photovoltaic	0.01–10 mW/cm^2
Thermal	Thermoelectric Pyroelectric	1–10 mW/cm^2

Voltage vs. Capacity vs. Size Trade-off The main considerations for selecting the battery are the voltage level, the discharge rate, the size/weight, and rechargeability based on the requirement of the application. Table IV shows the characteristics of various battery technologies that allow to choose the best technology for the application [66].

2) Energy Harvesting Technologies: The field of energy harvesters or scavengers has significantly evolved since the beginning of the 21^{st} century as an alternative energy source [67]. They are mainly used in applications where the system is inaccessible and has insufficient battery capacity. Thus, energy harvesters are used to power up the electronic system without a battery fully or to recharge the available one extending the system's operational lifetime. The use of supercapacitors can resolve issues related to peak power inadequacy.

Power Density vs. Technology Trade-off: There are numerous types of energy harvesters [68] ranging from the most common types such as miniaturized photovoltaic cells to vibration energy harvesters, which can be found nowadays even in standard wristwatches. Impedance matching considerations are critical for maximizing the conversion efficiency of the source to the harvested energy [69], [70].

The choice of the most appropriate energy harvesting technology is driven by the electronic system's application and power needs. A comparison of various technologies is summarized in Table V [71]. Except for harvested power level, size and power harvesting continuity can also be critical factors for choosing the most applicable technology [72].

3) Power Management: A voltage regulator is designed to take a variable voltage input and provide a constant output voltage. They are typically used for sourcing or sinking a significant amount of current. Except for maintaining a specific

TABLE III
COMMON WIRELESS TECHNOLOGY STANDARDS

Technology	Data Rate	Maximum Range	Network Type	Operating Freq.	Power
Bluetooth 3.0	Up to 24 Mbps	100 m	Peer to Peer	2.4 GHz	Medium to High: [0, 20] dBm
Bluetooth 4.0	0.25 – 1 Mbps	100 m	Peer / Mesh	2.4 GHz	Low to Medium: [-20, 5] dBm
Bluetooth 5.0	0.5 – 2 Mbps	1 km	Peer / Mesh	2.4 GHz	Low to Medium: [-20, 10] dBm
Zigbee	40 - 250 kbps	300 m	Mesh	2.4 GHz	Ultra Low to High: [-20, 20] dBm
Wifi	11 / 54 / 600 Mbps	100 m	Peer to Peer	2.4 or 5 GHz	High to Ultra High: [10, 35] dBm
LoRa	25 - 50 kbps	15 km	Mesh	433 or 863 or 915 MHz	Medium to High: [0, 20] dBm

voltage level different from the power supply, they act as a noise and protection buffer to the circuit.

Linear vs. Switching Voltage Regulator Trade-off: Voltage regulators are classified as linear and switching [73]. The linear regulator conducts only buck (step-down) DC-DC conversion and, thus, the input voltage should be some amount higher than the output. A low-dropout (LDO) regulator is commonly used since its input and output values are close. The linear regulators' category has low complexity, low noise, and low cost. The disadvantage is power inefficiency due to constant power dissipation as heat, requiring a heat sink. The switching regulators are named after the rapid switch of a series element on and off. Their main advantages are low power consumption, low area, and wide input voltage as input/output, capable of buck, boost (step-up), and buck-boost conversion. Their drawbacks are the higher complexity, cost, and noise compared to linear.

4) Biasing: A voltage reference can provide higher precision and stable output but a constrained supply/sink current. It is used in precision analog circuitry where a standard value is needed to measure voltage against it, e.g., ADCs, DACs, comparators.

Shunt vs. Series Voltage Reference There are two types: shunt and series. The shunt is a simple design that operates in a specific range of currents. They show superior stability and can operate with high supply voltages. The series is selected when there is a need for supplying a larger amount of current, power efficiency, and the supply voltage varies widely [74].

IV. SENSORY SYSTEM CHARACTERISTICS

Sensor interfaces and readout sub-systems involve specifications and definitions that guide the system design. These definitions can be useful for the AFE design with an optimized trade-off between complexity, cost, size, and performance for a specific application.

- **Range & Sensitivity**: The sensitivity of a sensor is defined as the ratio of the change in the output to a unit change of the sensed parameter. The sensor's range is defined as the difference between the maximum and minimum value of the sensed parameter that the sensor can detect. This fact includes both the magnitude of the difference and the absolute values. These two characteristics combined are of utmost importance since they define the sensor signal range to be read by AFE.
- **Resolution, Accuracy & Precision**: The resolution of the sensor is defined as the smallest change in the sensed parameter that the sensor can differentiate. Accuracy is defined as the difference between the measured and actual values. Precision is defined as the ability to reproduce repeatedly with a given accuracy. These three characteristics of the sensor, along with the application's specifications, are enough to pinpoint the correct measuring circuits and proper signal conditioning to be used. For example, if the sensor's accuracy is sufficient for the application, then the trade-off between cost and performance can be shifted towards lower cost components since circuits with high accuracy are not necessary.

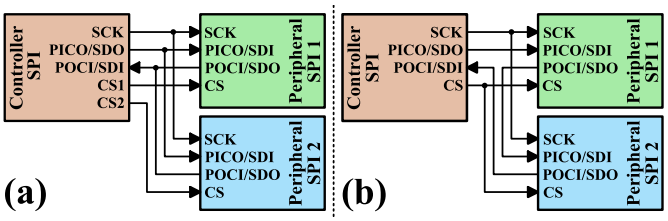

Fig. 15. SPI interconnection: (a) Typical and (b) Daisy chain.

- **Response Time**: The response time is defined as the time lag between the input and output. This feature is important because if the required response time from the system is relatively low, even if the sensor is capable of responding quickly, the use of low-pass filters might be prohibited.
- **Hysteresis & Linearity**: Hysteresis is defined as the incapability of the sensor's output to follow in the same way, the changes in the parameter of interest when the parameter is varied from low to high or high to low. Linearity shows how close to a linear relationship is between the sensor output and the parameter of interest. Nonlinearities in sensor output and highly hysteric behaviors will result in different sensor characteristics in different parameter ranges, which would make the design of the readout system much more complicated.
- **Temperature Effects, Zero Offset & Zero Drift**: This characteristic usually contains two types of information. One is the operating temperature of the sensor, and the second is the effect of the temperature on the sensor performance, usually expressed as temperature coefficient. Zero offset is defined as the non-zero output of a sensor when there is no input. Zero drift is defined as the departure of output from zero value over a period of time for no input. These attributes allow the AFE engineer to understand when the sensor is actually functioning within the manufacturer's specifications and how it is affected when at a specific value for a long time. Electronic components like Operational Amplifiers (OpAmps) have similar specifications, and if the application is demanding, then these characteristics of the measuring circuits should improve and not limit the capabilities of the sensor.

Fig. 16. Implemented capsule.

- **Signal-to-Noise Ratio (SNR) & Limit of Detection (LOD)**: These are critical parameters for AFE. SNR is defined as the ratio between the magnitudes of the signal and the noise at the output. LOD is defined as the lowest quantity of the sensed parameter that can be distinguished from the zero value of the sensed parameter. LOD is calculated based on the sensitivity of the sensor and the noise at zero input. If the application involved very low LODs, the noise has to be significantly decreased and the sensitivity increased. Additionally, to have more clear signals and improve the resolutions of the sensor, higher SNR values should be used. Although all of these parameters come from the sensor, the measuring circuits can either maintain the initial quality of the signal or deteriorate it if not designed accordingly. For example, noise generated by the electronics when not designed correctly can significantly deteriorate the quality of the signal and subsequently will have a negative effect on the measured LOD.

V. Sensor System Case Studies

Several case studies are described in this section, including design considerations for highly integrated readout systems and the practical issues involved.

A. Ingestible Capsule

The first case study focuses on the design of a fluorescent capsule for cancer detection in the small intestine, as illustrated in Fig. 16 [75]. The operating principle is that the patient is injected with a fluorescent dye that binds on cancerous cells in the small intestine and the capsule, using laser diodes excites the dye and records its fluorescent emission using photodiodes. If there are cancerous cells bound to the dye, they will emit light at a different frequency than the excitation frequency.

Other than the sensing difficulties of this approach, the application has stringent constraints requiring ultra-low power consumption. The battery should last for almost a day allowing the capsule to travel to and through the gastrointestinal tract. Furthermore, the total size of the capsule must be maintained within a certain range for it to be ingestible while including a complete, stand-alone system. Finally, the recorded data need to be transmitted from the capsule to an external device without the option of direct contact since the capsule should be waterproof. In this example, the AFE used was simple TIAs

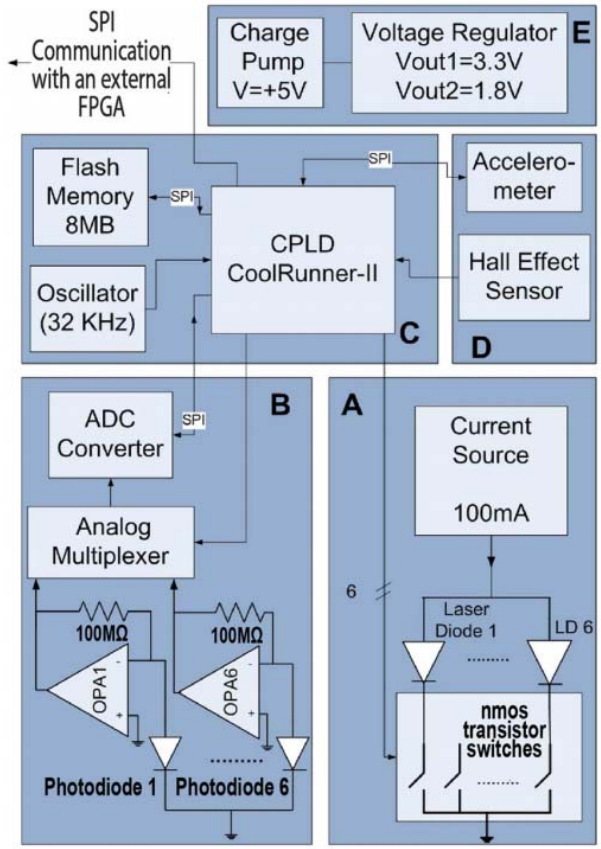

Fig. 17. System level description of the capsule.

for each of the six diodes to measure the current and a current source for the excitation of the laser diodes (Fig. 17).

Performance vs. Power Trade-off: There was a vital trade-off between power consumption and system performance in terms of sampling rates, given the capsule is sometimes stationary and other times might shoot forward during peristalsis, thus requiring a high maximum sampling rate. In order to maintain low power while satisfying a high spatial sampling resolution within the intestine, a dynamic sample rate was adopted. The repetition rate of the strobing excitation source, and the concurrent sampling rate of the photodiodes, was adjusted using information derived from an accelerometer. This decision was game-changing since the two most power-consuming components were the strobing illumination diodes and the flash memory module to which the data was stored [76].

Functionality vs Size Trade-off: Capsule size and the number of components in the system were also an important trade-off. In order to achieve the initiation of data transmission when the capsule was excreted, a Hall sensor was used as a switch, and the data were transmitted optically using the illumination laser diodes for optical communication, thus eliminating the need for extra peripherals [75].

B. Bioinspired MEMS Gyroscope

This case study is about the design of a bioinspired, microfluidic gyroscope for vestibular prosthesis [77]. The gyroscope's operation is based on the inertial of the internal

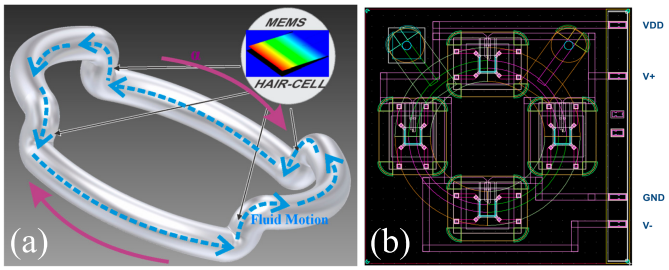

Fig. 18. Ultra-low power, hybrid MEMS gyroscope design, (a) microfluidic channels, (b) Actual layers of the design.

fluid within the microfluidic channels as shown in Fig. 18. This application's constraints and requirements were ultra-low power consumption, low-cost, and miniaturization since it was intended as an implantable device. Conventional MEMs gyroscopes rely on structures that vibrate continuously at around 100 kHz to enable the small MEMS masses to take advantage of the Coriolis Effect. Thus they require a high power consumption that is about 7 mW per axis. In order to design for much lower power consumption, a bioinspired approach was employed using passive structures. A donut-shaped microfluidic channel was filled with water, giving a larger inertial mass that did not need to be vibrated. The fluid flowed relative to the structure when the sensor was rotated, thus pushing the cantilevers either up or down. On the cantilevers, piezoresistive components were fabricated in such a way that two of them would be compressed, and the other two would be expanded.

Functionality vs. Complexity Trade off: In this case, since the sensor would be used as an implantable device, temperature compensation was not necessary given that it is in a controlled environment. The four-arm Wheatstone bridge implemented to maximize sensitivity does not require the complex driving electronic circuits of a vibration-based gyroscope nor the complex capacitance detection circuitry. The readout can be a simple instrumentation amplifier and a D/A converter.

Fabrication Technology vs. Cost Trade-off: Other than just functionalities, the aim was to maintain a low cost; hence the fabrication technology choice was important. A commercially-available, bulk-micromachining MEMS technology was used.

C. Soil Quality System

This case study concerns a low-cost sensing node capable of addressing all the requirements of direct soil quality monitoring while being suitable for implementation in Automated Decision-Making Systems (ADMS) of Precision Agriculture [22]. A solar panel powers the system, and it has total dimensions of 180 × 120 × 90 mm (Fig. 19). This case study's application constraints were low-cost, enabling its use for in-field sensor networks while having adequate performance to allow proper sensor measurements. This system features several design trade-offs.

Performance vs. Cost vs. Modularity Trade-off: Maximizing the performance of the AFE implies a significant cost increase. However, commercially-available ICs were utilized

Fig. 19. Soil quality monitoring system.

with multiple capabilities to minimize the cost while ensuring satisfactory performances in this system.

Versatility vs. Cost Trade-off: Although the AFE was initially designed based on multiple sensing principles, the system was designed in such a way to accommodate commercial sensors with multiple communication protocols such as I^2C and SPI. Bluetooth, WiFi, and LoRa communication technologies are supported, making the system IoT compatible while maintaining a low cost. The designed instrumentation is versatile enough to accommodate different sensors operating under the same principles with different sensitivities. All the modifications to the system can be done through software during sensor calibration. The sensing node consists of three main modules as shown in Fig. 20. Finally, the SI module is designed in such a way so that any required adjustments to fit different sensors can be performed by the controller without the need for any hardware change. This fact gives the system the capability to achieve maximum resolution and accuracy while adjusting for possible sensor differences and fabrication mismatches. The three modules are detachable, and the SI module can be completely independent of the rest.

Performance vs. Power Trade-off: Since environmental parameters in agriculture do not change at a fast pace, the node can switch from Active while taking measurements and data transmission to Sleep mode when not needed to minimize the node's power consumption. The power supplying circuits can be enabled or disabled from the controller. In order to avoid any unwanted interferences, the SI module is equipped with isolation switches that are controlled by the controller and are used to connect only one sensor at a time.

D. Heart Sounds Simultaneous Recording System

Heart sounds can reveal abnormalities related to the mechanical function of the heart valves. The stethoscope

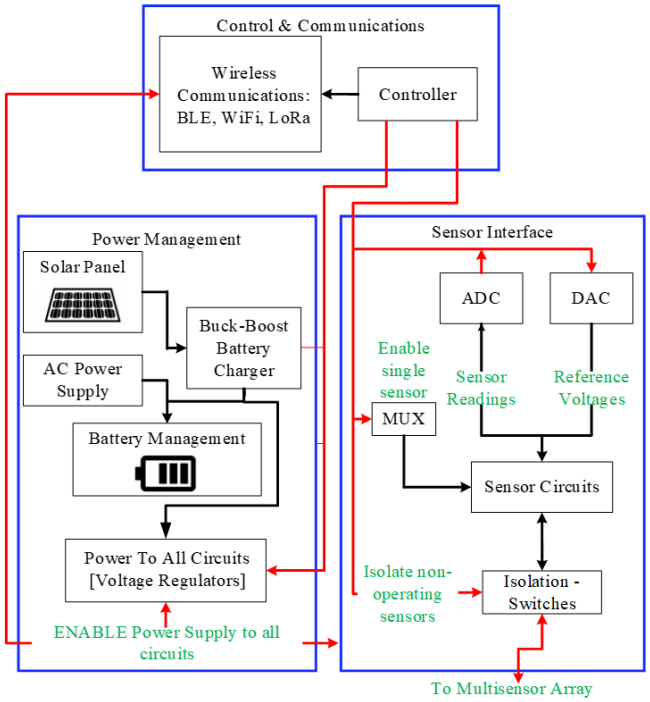

Fig. 20. Soil quality monitoring system architecture.

has been the apparatus for heart sound detection. Due to technology evolution, the stethoscope can evolve into a sensing node in a system that incorporates multiple identical and distributed sensors that can allow simultaneous sampling. The simultaneity can fuel studies in cardiac acoustic mapping, where spatial sound information is available for the heart sounds emanating from the chest. Stethovest is the device to conduct simultaneous recording from critical chest locations that can reveal valvular abnormalities [78]. Fig. 21 illustrates the Stethovest from a system level perspective.

System Architecture Design Trade-offs: The sensors are embedded in a wearable vest at specific locations, suggested by physicians for best-heard sites for abnormal sounds. The required sampling speed of the system is extracted from the speed of sound in human tissue (1500 m/s) and the sensor separation (minimum 3 cm) at 50 kSPS. The AFE readout channel is a custom design based on commercial off-the-shelf components. The pre-amplifier (PA) is selected with the view of low input-referred noise since this part will play the most crucial role for noise in the system at the expense of higher power consumption. The signal is then passed through a 4-pole Sallen Key low-pass filter to achieve sharp roll-off in the frequency under interest. The Bessel active filters topology is selected since it provides a constant group delay, so the signal phase will not be distorted. This point is critical since the entire system should provide an accurate phase between the channels. The signal is then amplified to match the ADC's input range, taking maximum advantage of its resolution. All the conditioned signals conclude to two 8ch-ADC arrays (USB-1608FS-Plus) of a maximum sampling rate of 50 kSPS per channel if all channels are in use. The internal clock of ADC Array A is shared with Array B to sample at the same time, avoiding the use of any external oscillator. The acquired signals are acquired through a laptop using USB communication. For a high data rate, wired communication is required. A Matlab interface is responsible for plotting and saving the data locally. The entire system is battery-powered for safety precautions and reduction of hum interference. The employed LDO is capable of supplying the expected current.

VI. Bio-Inspired Vision Systems

Biological sensory organs operate at performance levels set by fundamental physical limits, under severe constraints of size, weight, and energy resources; these are the same constraints that many synthetic sensor systems have to meet. Eyes are specialized sensory structures that extract information from the intensity, polarization, and spectral content of the light. Reliable and timely answers to the questions: Is there anything out there?, Where is it?, and eventually, What is it? are the goals of all processing that follows the photoreceptor mosaics in biological systems. This is in contrast to a charge-coupled device (CCD) or complementary metal-oxide semiconductor (CMOS) video and still cameras that have been developed for the precise measurement of the spatial-temporal light intensity and color distribution, often within a fixed time interval, for accurate communication and reproduction in electronic or printed media. In this article, we discuss bio-inspired image sensors, known as Dynamic Vision Sensors (DVS), designed for machine perception. DVS based cameras have evolved from early work in silicon retinas [79]–[81] for visible light and polarization [82], [83].

A. Dynamic Vision Sensor (DVS) Cameras

Cameras that are available or have been available for experimentation in the vision community Temporal Contrast Vision Sensor (TCVS) [84], ATIS [85] and DAVIS [86]. DVS-based cameras are anisochronous devices whose output is a timestamped pixel co-ordinates, pixel attributes such as color and polarization, and a timestamp that corresponds to the instance that data were captured. Inherent in their operation is frameless image acquisition, over a large dynamic range, low latency readout, and energy efficiency. In addition, ATIS and DAVIS provide frame-like output from an auxiliary Active Pixel Sensor circuitry included in the pixel. Experimental DVS devices reported in the literature but not available in the broader community for experimentation include the "Octapus" retina [87], the ALOHA DVS [88] and the temporal difference sensor [89].

B. Digital Dynamic Vision Sensors (DDVS) Cameras

The DVS devices discussed in the previous sections are biologically inspired sensors that efficiently use limited bandwidth by only encoding salient features and digitally transmitting through a spike/event-based code. As technology scales, more transistors packed into a smaller area directly translates to extra functionality. Furthermore, it is well established that for systems beyond visible imaging, a digital approach is the only scalable, energy-efficient solution. The same argument can be made for readout architectures that begin with pixels that provide quantized outputs such as Geiger mode avalanche photodiodes (single photon detectors analogous to

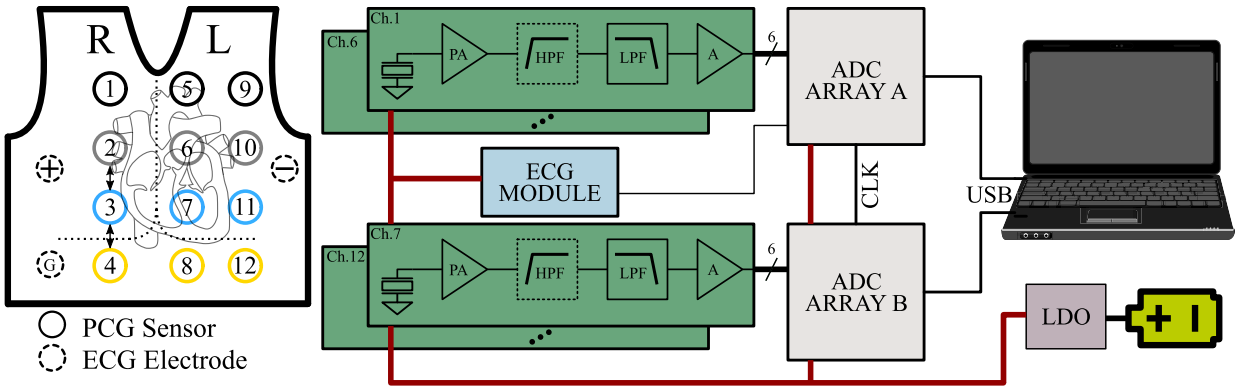

Fig. 21. Block diagram of stethovest.

	Scanned	Event-based
Number of Pixels	N x M	N x M
Frame Rate (FR) frames/s	10,000	-
Data Rate (bits/s)	24 x N x M x FR	Variable
Energy (pJ)	24 x N x M x 1 (per frame)	log2(M) + log2(N) x 1 (per event)
Latency = 1/FR (ms)	0.1 (per frame)	0.1 / (M * N) (per pixel)

Fig. 22. A comparison of frameless DVS to traditional framed based cameras. The sensor is assumed to be read out with 8-bits resolution. The physical dimensions of the die is assumed to be 1cm and the cost to transmit 1 bit of data across the die is 1pJ (charging and discharging the capacitance of 1cm long interconnect).

silicon rods) [90]. Thus, instead of the mostly analog approach of neuromorphic electronic systems, we want a mostly digital approach to leverage Moore's law scaling. The bio-inspired approach abstracts principles from biology such as local processing for information extraction, local gain control and asynchronous on demand, event based sampling, and pushes them into the digital domain [91], [92]. This is important as technology moves towards smaller process nodes where the transistors are optimized for digital rather than analog functionality [93].

Camera Technology Trade-offs: In choosing a visual sensor AFE involves trade-offs derived from the application domain. Fig. 22 summarizes the trade-offs between the two types of cameras.

C. Analysis of a Dynamic Vision Sensor AFE

Silicon photosensors transduce optical signals with information about visual stimuli into electrical signals, measured or communicated to other circuitry for further processing. This process involves several signal transformations, from incident photons, to absorbed photons, to excited hole-electron pairs, to collected hole-electron pairs, to current or voltage. We present a communication channel model to quantify the transmission and degradation of visual information in adaptive silicon photosensors.

Recent years have seen the widespread development and commercialization of bio-inspired systems. Integrated photosensors combine optical detection with electronics at the silicon level. Whereas CCD technology is incompatible with CMOS electronics, integrating circuitry with detectors in a

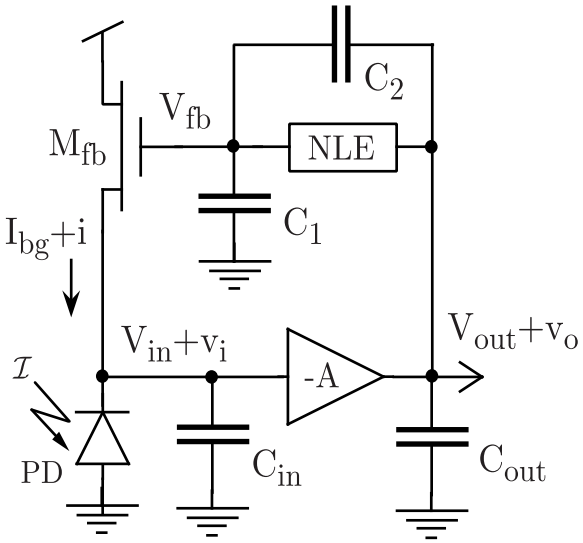

Fig. 23. Adaptive photoreceptor circuit of Delbrück and Mead.

standard CMOS process allows for computations to be performed on the image plane. We now consider the Delbrück silicon photoreceptor shown in Fig. 23, that was employed in one of the first DVS cameras. This circuit provides an analog output which has low gain for static signals and high gain for transient signals about an operating point. This adaptation strategy allows the output to represent a large dynamic range while retaining sensitivity to small inputs. We study the linearized behavior about an operating point. A slightly modified version of the latter circuit is employed Temporal Contrast Vision Sensor (TCVS) [84], and DAVIS [86].

The structure of the communication network architecture for the silicon adaptive photoreceptor is shown in Fig. 24. The transfer function H_{tr} of the circuit, from input photocurrent i to output voltage v_o, is given by

$$H_{tr} = \frac{A/G}{(\tau_i s + 1)(\tau_o s + 1) + \frac{Ag_{mn}}{G}\frac{g+sC_2}{g+s(C_1+C_2)}} \tag{21}$$

where A is the gain of the output amplifier, G is the conductance at the input node, τ_i is the time constant at the input node, τ_o is the time constant of the output amplifier, g_{mn} is the transconductance of transistor M_{fb}, and g is the conductance of the adaptive element NLE. The transfer function from

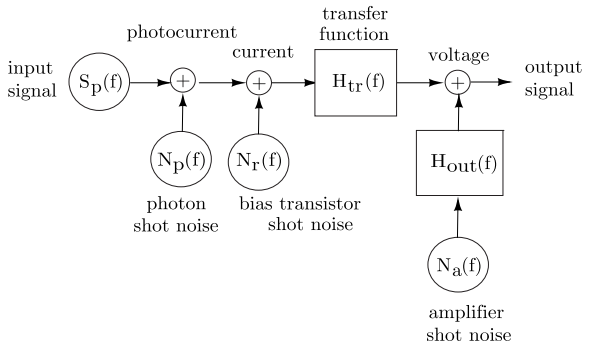

Fig. 24. A communication network architecture for the silicon photoreceptor. Signal transformations are modeled as filters linearized about an operating point, and noise sources are independent and additive.

current to voltage v_o at the output node is given by

$$H_{out} = \frac{B}{\tau_o s + 1} \tag{22}$$

where $1/B$ is the conductance at the output node. The parameters of these transfer functions will depend on the bias conditions as well as device and circuit parameters.

In this work, we use a minimal model for the noise of a MOS transistor which includes just the shot noise. This noise component will be independent of device parameters and specifics of the fabrication process. Each MOS transistor and diode will contribute current shot noise $N(f) = 2qI$ where q is the elementary charge, and I is the current through the transistor. At the input node, there will be photon shot noise and current shot noise contributed by the bias transistor, for a total of $4qI_{bg}$, where I_{bg} is the photocurrent determined by the background illumination. At the output node, noise will be contributed by all three transistors of the feedback amplifier, for a total of $6qI_b$, where I_b is the bias current for the amplifier. The noise contributed by the adaptive element is neglected since the current through the element is small. The total input-referred noise from these sources will be:

$$N_{tot}(f) = 4qI_{bg} + \left|\frac{H_{out}}{H_{tot}}\right|^2 6qI_b.$$

When the silicon photoreceptor is biased at high current densities, the noise sources at the input node dominate; otherwise current shot noise of the transistors in the feedback amplifier plays a significant role.

The transfer characteristics and noise power spectral density of the adaptive silicon photoreceptor are determined experimentally in Fig. 25. The input light was provided by an LED held in position with a custom-machined fixture over the packaged chip. The transfer characteristics from input light to output voltage were measured by having the LED was biased with a constant DC voltage plus a small AC signal. A spectrum analyzer computed the transfer function as the ratio of the power spectra of the output signal and the input signal. The LED was biased with a constant DC voltage only to measure noise characteristics. The noise power spectral density is the spectrum of the output signal for a constant input. Different levels of background light were obtained using neutral density filters placed in between the LED fixture and the chip.

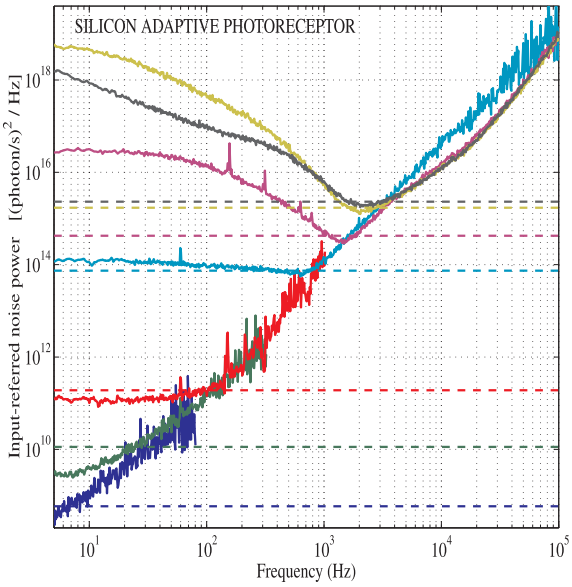

Fig. 25. Input-referred noise power for the silicon adaptive photoreceptor as a function of frequency, derived from our experimental data. The different traces represent various background light levels, corresponding to the (+) in Fig. 26. The dashed lines represent the total channel power (signal plus noise) after waterfilling for each operating point.

D. Fundamental Limits in Silicon Versus Biology

From the experimentally determined input-referred noise power densities shown in Fig. 25, we compute the information capacity for both the blowfly and silicon photoreceptor as a function of the incident light intensity. For the capacity to be well-defined, we must specify how to constrain the signal power. We assume a fixed contrast power of 0.1 for all light levels, where contrast is defined as the normalized intensity. The latter value of contrast is representative of natural scenes. Fig. 26 shows a quantitative comparison of the capacity of both the blowfly and silicon photoreceptors as a function of incident light intensity. The capacity for our model of the blowfly photoreceptor is shown as the solid black line, with empirical estimates from [94] shown as black "x"s. The capacity for the silicon photoreceptor model is shown in Fig. 26 along with empirical estimates from experimental data, shown as blue "+"s. The three solid curves are for different bias conditions: the red line shows the maximum capacity (obtained as the bias current increases without bound), the blue line shows the capacity when the silicon photoreceptor uses the same power as the blowfly photoreceptor, and the green line shows the capacity when the silicon photoreceptor is biased for minimum bit energy. Interestingly, the capacity of the blowfly photoreceptor is higher for lower light levels, but there is a cross-over point beyond which the silicon photoreceptor can achieve higher capacity. As indicated in Fig. 26 this cross-over is about 2×10^5 photons per second, or approximately as bright as a dimly lit room.

The model presented here allows the determination of the dominant noise sources, limiting the information transmission rates in silicon photoreceptors. The only sources modeled for the silicon photoreceptor are photon shot noise and current shot noise; additional noise sources account for the discrepancy between the model and the experimentally derived

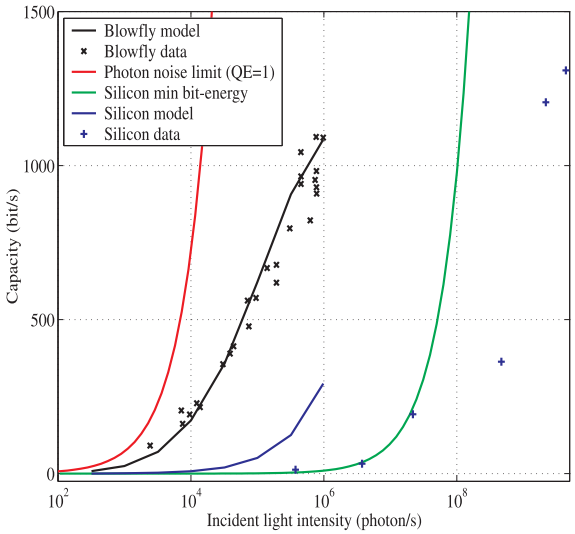

Fig. 26. Information capacity as a function of incident intensity for blowfly photoreceptor computed from our model (black) and estimated from experimental data (x's) [94], and for the silicon photoreceptor under two bias conditions: using the same power as the blowfly (blue), and when biased for minimum bit-energy (green). The experimentally derived information capacity of the silicon photoreceptor is shown in (+'s). Unmodeled noise sources account for the discrepancy between predicted and measured capacity. The photon noise limit is plotted in red.

capacity. Flicker noise in the MOS transistors, as discussed in an earlier section, shot noise from leakage currents, and instrumentation noise, not included in the theoretical model of the silicon photoreceptor, are likely to be the dominant sources of noise which limit the performance of the silicon photoreceptor.

VII. Conclusion

This tutorial has explored sensory systems' fundamental concepts and trade-offs, starting from the basics of sensory signal representations, noise models, and fundamental performance metrics. The basic building blocks of sensory systems readout are then discussed, from the driving circuits for sensor excitation to measuring circuits up to signal conditioning circuits. Fundamental and practical trade-offs often encountered in sensory system design are presented. The tutorial concludes with work from our labs on five sensory systems architectures used as concrete examples to discuss design trade-offs at the system level.

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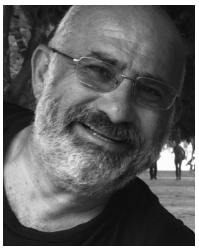
Christos Sapsanis (Student Member, IEEE) received the Diploma (combined B.Eng. and M.Eng.) degree in electrical and computer engineering (ECE) from the University of Patras, Greece, in 2013, and the M.S. degree in electrical engineering from the King Abdullah University of Science and Technology, Saudi Arabia, in 2015, under the King Abdullah Fellowship. He is currently pursuing the Ph.D. degree with the ECE Department, Johns Hopkins University. His research focuses on integrating fields, such as sensors, mixed-mode VLSI, embedded systems, signal processing, and machine learning for the realization of smart sensor systems. He was a recipient of the Andreas Mentzelopoulos Fellowship and a scholar of the Alexander S. Onassis Foundation.

Marios Sophocleous (Member, IEEE) received the M.Eng. degree in mechatronics from the University of Southampton and the Ph.D. degree in thick-film underground sensors from the University of Southampton in 2016. He has been a Special Scientist with the Holistic Electronic Research Laboratory, University of Cyprus, since 2016. He has coauthored more than 30 peer-reviewed journal and conference publications in very high-impact journals and major conferences, and served as a committee member multiple times. He was the Fulbright Schuman Fellowship 2021 Winner. He has been nominated for the Outstanding Young Engineer Award of the IEEE Instrumentation and Measurement Society in 2019 whilst he was the Young Scientist 2020 Finalist in Cyprus. He is a member of the Editorial Advisory Board of *Sensors and Actuators—A: Physical* journal and *Microelectronics International* journal whilst being a Lead Guest Editor of an IEEE SENSORS JOURNAL Special Issue.



Andreas G. Andreou (Fellow, IEEE) is currently a Professor of Electrical and Computer Engineering, Computer Science, and the Whitaker Biomedical Engineering Institute, Johns Hopkins University. He is also the Co-Founder of the Johns Hopkins University Center for Language and Speech Processing. His research focuses on the science and technology of sensory communication and computing machinery, that is, abstract and physical computational structures for sensory information processing, pattern analysis, and machine intelligence. Notable micro-systems achievements over the last 25 years, include a contrast sensitive silicon retina, the first CMOS polarization sensitive imager, silicon rods in standard foundry CMOS for single photon detection, and a large scale mixed analog–digital associative processor for character recognition. Significant algorithmic research contributions include the vocal tract normalization and heteroscedastic linear discriminant analysis for speech recognition, and algorithms for multimodal bio-inspired action recognition. In 1996, he was elected as an IEEE Fellow, for his contribution in energy efficient sensory microsystems.

Julius Georgiou (Senior Member, IEEE) received the M.Eng. degree in electrical and electronic engineering and the Ph.D. degree from Imperial College London, London, U.K., in 1998 and 2003, respectively. During the last two years of his Ph.D. studies, he was heavily involved in a technology startup company, Toumaz Technology, as the Head of Micropower Design. In 2004, he joined the Johns Hopkins University, Baltimore, MD, USA, as a Postdoctoral Fellow, before joining the University of Cyprus, Nicosia, Cyprus, as a Lecturer, in 2005. In 2009, he was promoted to an Assistant Professor. His research interests include low-power analog and digital ASICs, implantable biomedical devices, bioinspired electronic systems, brain–computer interfaces (BCIs), semiconductor device design, and inertial and optical sensors and related systems. Dr. Georgiou is a member of the IEEE Circuits and Systems Society, the BioCAS Technical Committee, and the IEEE Circuits and Systems Society Analog Signal Processing Technical Committee. He was the General Chair of the 2010 IEEE Biomedical Circuits and Systems Conference.