Implementation and Hardware-In-the-Loop Testing of A Wide-Area Damping Controller Based on Measurement-Driven Models

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***Abstract*—In an effort to suppress inter-area oscillations observed in the Continental Europe synchronous area system, a wide-area damping controller using a measurement-driven model was previously developed and validated by simulations. Targeting future field implementation, in this work, a hardware prototype of the controller is developed, and a hardware-in-the-loop (HIL) test setup is built to validate further the controller performance under realistic conditions considering random communication delay and occasional/persisting data loss, etc. Several auxiliary function modules, e.g., adaptive delay compensator, data buffer, and supervisory control, have been developed and integrated with the controller to improve its performance and reliability. The controller performance is validated in this HIL test setup using an actual oscillation event. Different delay compensation strategies and communication protocols are also investigated. The HIL test results have demonstrated that the developed controller effectively suppresses the target inter-area oscillations under various communication network uncertainties.**

***Index Terms*— Continental Europe synchronous area system, hardware implementation, hardware-in-the-loop (HIL), inter-area oscillations, wide-area damping controller (WADC).**

I. Introduction

While large power grid interconnections normally improve the resiliency and efficiency of transmission networks, inter-area oscillation events are becoming more frequent in power systems and pose a significant threat to system stability and security [1]. One of the recent events was the December 3rd, 2017 oscillation event in the Continental Europe synchronous area system. The oscillation mode of 0.293Hz between the north (Germany/Denmark) and the south (southern Italy) was excited by two consecutive generator disconnections [2].

With the rapid deployment of phasor measurement units (PMUs) in the past decades, wide-area damping controllers (WADCs) utilizing remote synchronized measurements have proved to be more effective in suppressing inter-area oscillations than local power system stabilizers due to higher observability and controllability [3], [4]. A variety of equipment can be utilized as actuators of the WADC schemes, such as generators, HVDC links, FACTS devices, and renewables [5]-[7]. Such a WADC was developed and demonstrated through simulations in [7]-[8], which is based on a measurement-driven-model design method to improve system damping with the capability to adapt to system operating conditions and is less reliant on the accuracy of power system models.

In this paper, as a continuation of the work in [7]-[8], the WADC was implemented in hardware and tested in a hardware-in-the-loop (HIL) setup. The objective was to evaluate the performance of the WADC under realistic operating conditions, such as measurement error, communication uncertainties, etc. In particular, the WADC has been implemented on the CompactRIO system, a general-purpose controller provided by National Instruments (NI) for prototyping [9]. An HIL testing platform, including a real-time simulator (OPAL-RT), was constructed to emulate realistic operating conditions with various types of communication network uncertainties and impairments. The hardware controller has been tested thoroughly in the HIL setup and was enhanced with several auxiliary function modules that were implemented and validated during the course of the testing to ensure satisfactory performance of the WADC under realistic operating conditions.

The rest of the paper is organized as follows: section II gives an overview of the HIL setup and the model for the continental Europe system on OPAL-RT. A brief introduction of the WADC and details of its hardware implementation are presented in section III. In section IV, the results of three representative HIL testing cases are presented to verify the performance of the WADC. Conclusions are made in section V.

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II. The Hardware-In-the-Loop Testing Setup

Compared with computer simulations, the HIL setup emulates a real-time operating environment for verifying the performance of the developed hardware WADC under realistic conditions, including measurement error/noise, varying time delay, and data package loss. In this section, an introduction of the HIL setup and details on the OPAL-RT ePHASORSIM model of the continental Europe model will be given.

A. Structure of the HIL Testing Setup

The HIL setup consists of an OPAL-RT real-time simulator, amplifiers, PMUs, a network switch, a communication network impairment simulator, and the WADC to be tested. An overview of its structure is shown in Fig. 1.

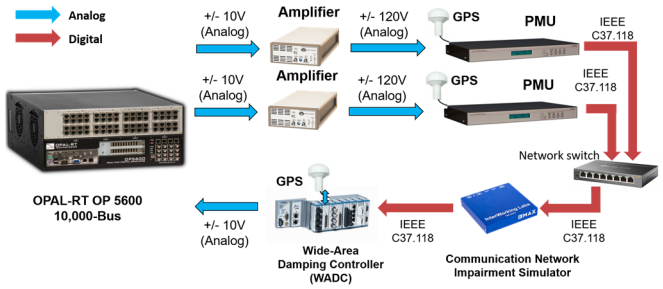


Figure 1. Overview of the HIL testing platform

The continental Europe interconnected grid is emulated in phasor domain on OPAL-RT real-time simulator. The Italian grid is modeled in detail, while dynamic equivalents are used for the rest of the system. The model consists of 2132 buses and was developed in OPAL-RT's ePHASORSIM module. The simulator converts the phasor results on selected buses into analog voltage waveform outputs in real-time. The outputs are connected to amplifiers that step up the 10V waveforms to 120V, mimicking the secondary windings of potential transformers. The PMUs calculate the frequency of the bus voltages and send the results to the WADC in the form of data packages compliant with the IEEE C37.118 standard [10]. Before the data reach the controller, there is a communication network simulator (KMAX) in the link [11]. It introduces network uncertainties such as random time delay, random data drop, etc., in a controlled manner. The control signals generated by the controller are converted to 10 V analog signals accepted by the input ports of the OPAL-RT, in which they are further fed into the actuators in the ePHASORSIM model to close the loop. In this work, for the Italian system, two synchronous condensers in south Italy were selected as actuators, and the frequency in south Italy was used as the feedback signal. Two PMUs in the HIL were dedicated to two different locations in southern Italy as a backup to each other.

B. Building the ePHASORSIM model on OPAL-RT

To emulate the continental Europe model on OPAL-RT, an ePHASORSIM model has been developed and tuned based on the offline dynamic model used in [7]. Several user-defined dynamic models for generation plants comprising generators, exciters, power system stabilizers, and governors, are constructed on the OpenModelica platform. The ePHASORSIM model has been validated against the offline dynamic simulation model, through both steady-state power flow and dynamic simulation results. Fig. 2 shows the comparison of the dynamic response of the system between the two simulation platforms, for the December 3rd oscillation event.

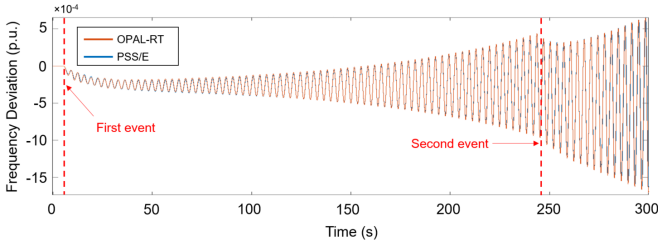


Figure 2. Comparison of frequency oscillations on OPAL-RT and PSS/E

With Prony analysis on the frequency responses, the two models (real-time and offline) are verified to have consistent dynamic responses with a damping of -0.41% at 0.293Hz after the first event and -0.628% at 0.292Hz after the second event.

III. Hardware Implementation of the Measurement-Based WADC

A. Basics of the WADC design

The WADC in this work is designed based on the system transfer function model identified with synchronized measurements during system disturbances [7]. Fig. 3 is a block diagram of the WADC in a power system.

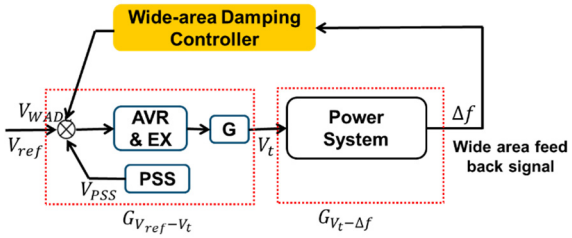


Figure 3. Power system with the WADC in the loop

where Δf represents the wide-area feedback signals to the WADC, and V_{ref} is the voltage reference of generator excitation system. The feedback signal is selected based on the result of FFT analysis that identifies bus locations with the highest magnitudes at the target oscillation frequency. The actuator locations are selected through the residue method [7], [8]. A basic structure of the transfer function model of the controller is as shown in Fig. 4.

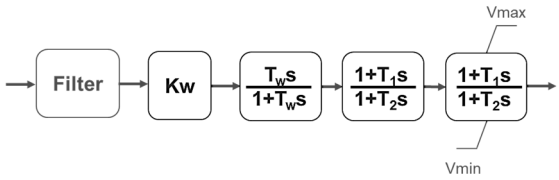


Figure 4. Transfer function block diagram of the controller

B. Hardware Implementation of the WADC

The WADC has been implemented on the NI CompactRIO system. In addition to the filters and lead-lag structures, several function modules are added to the hardware controller. An overview of the modules and their correlation is in Fig. 5.

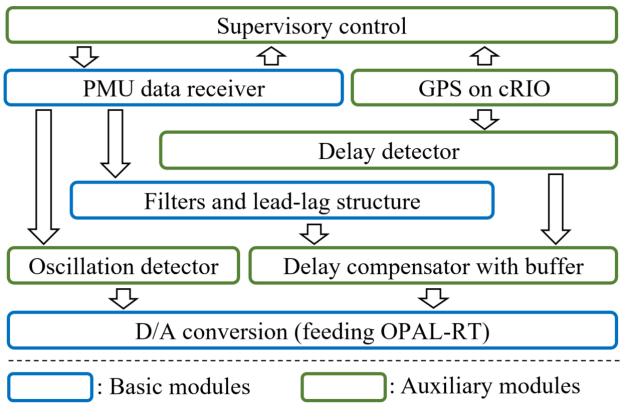


Figure 5. Structure and function modules of the WADC

The PMU data receiver, filter/lead-lag structure, and D/A conversion are basic modules for realizing the control. In addition, there are delay detector, delay compensator with buffer, and supervisory control as auxiliary function modules for improving the reliability and resiliency against uncertainties in realistic operating conditions. In this section, these function modules will be introduced in detail.

1) PMU data receiver: The PMU data receiver is based on the open-source real-time mediator "BabelFish" [12], [13]. It communicates with PMUs or PDCs compliant with the phasor measurement communication protocol IEEE C37.118-2011. It supports both TCP/IP and UDP/IP, but UDP/IP is recommended for the control purpose since the control algorithm is time-sensitive but more tolerable to data loss. More details can be found in section IV.C.

2) D/A conversion: The D/A module converts and conditions control commands, which are further fed into the OPAL-RT simulator as control signals for the actuators.

3) GPS synchronization: The GPS module in the controller converts the pulse-per-second (PPS) signal to accurate timestamps for the controller, which will be further used to determine the delay of the data packages and monitor the health of the PMU channels.

4) Delay detector: The delay detector monitors each data package for its delay by comparing the PMU timestamp attached to the measurement and the GPS timestamp from the WADC at the moment when the data package is used. The function shares the assessed delay with the delay compensator and the supervisory control module for further processing and control.

5) Delay compensator with data buffer: The delay compensator retrieves from the delay detector the actual delay of the packages and chooses the best set of compensation parameters to compensate for the angle shift caused by the delay. To reduce switching between compensation parameter sets, a buffer is used to stack incoming data and use only those mature around a preferred delay value without compromising the control effect, as shown in Fig. 6. In this work, the value is set to 500ms.

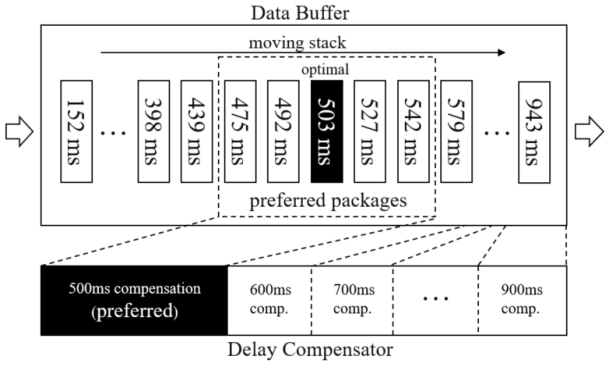


Figure 6. Delay compensator with data buffer

6) Supervisory control: The supervisory control module continually monitors the communication delay in all PMU channels and makes decisions to switch between the primary and backup PMUs as appropriate when the communication impairments are beyond the delay compensator's capability and may compromise the performance of the controller.

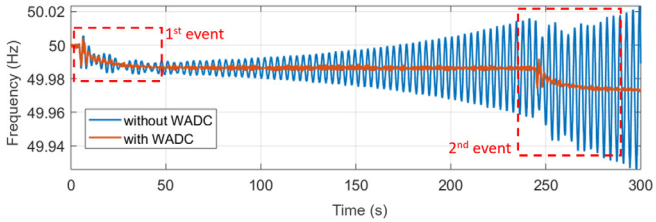
7) Oscillation detector: The oscillation detector module monitors the frequency deviation in a moving time window. When it detects and confirms an oscillation for a certain period, it will activate the control and alarm the operator. When the oscillation settles, it deactivates the control and moves to the standby mode after confirmation.

IV. Testing Results

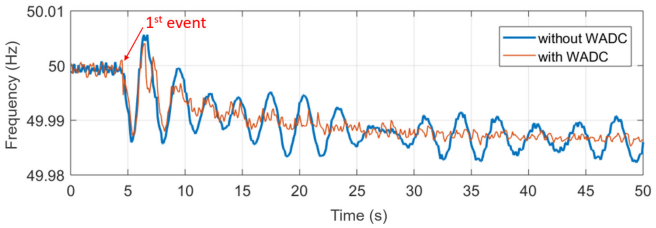
The WADC has been thoroughly tested on the HIL testing platform for its basic and auxiliary function modules. It has been improved based on the findings during the course of the testing. In this section, the results of three representative testing scenarios will be presented. First, a base case intended to verify the effectiveness of the controller in increasing the system damping will be given. Then, the second testing case will be dedicated to validating the controller's handling of varying communication delays with the delay compensation and data buffer module. The third testing case compares the controller's capability to tolerate data drops under different communication protocols (TCP/IP and UDP/IP) and gives recommendations based on the testing results.

A. Base Case

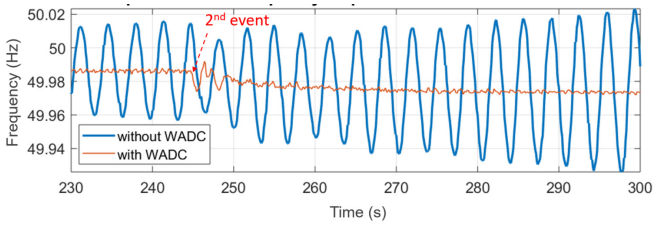
The base testing case is intended to demonstrate the basic performance of the damping controller under no additional communication network impairments. In the base case, the comparison is between the system with and without the WADC, under the two consecutive events that happened on December 3rd, 2017. The result is shown in Fig. 7, and the damping ratios in Table I are calculated through Prony analysis. Without the WADC, the oscillation grew, with damping ratios of -0.486% and -0.449% after the two events, respectively. When the WADC is enabled, the damping ratio increased to 12.326% and 12.051% during the two events, and the oscillations settled within 10 seconds. The WADC significantly improved the system damping and hence enhanced the stability as a result.



(a) Overview of the two consecutive events



(b) Details around the first event



(c) Details around the second event

Figure 7. Base case – Frequency response with and without the WADC

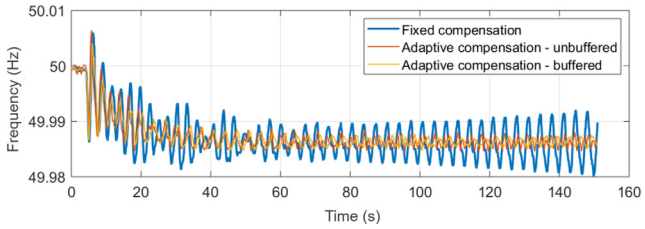
TABLE I COMPARISON OF DAMPING RATIOS W/ AND W/O WADC

Controller Presence	Damping Ratio (%)	
	1st event	*2nd event*
Without WADC	-0.486	-0.449
With WADC	12.326	12.051

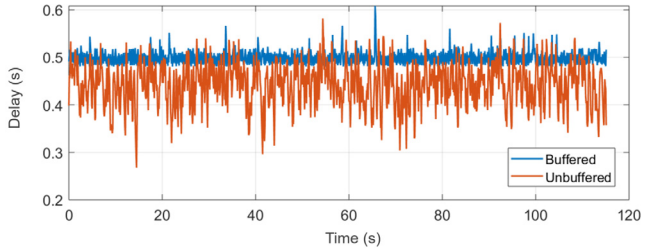
B. Delay Compensation and Data Buffer Test

To test the effectiveness of the delay compensation and data buffer module, the network simulator is configured to introduce random time delay into the communication link between the PMU and the WADC. The inherent delay in the HIL loop is around 150ms, and the random delay introduced by the network simulator has a Gaussian distribution (μ = 300ms, σ = 30ms). There are three delay compensation strategies in this test case, fixed compensation, adaptive compensation without data buffer, and adaptive compensation with the data buffer. The fixed compensation has a fixed compensation parameter set designed for the inherent 150ms delay. The adaptive compensation without data buffer automatically chooses the parameter set that best suits the actual delay of the package being used. The adaptive compensation with data buffer strategy reduces parameter switching, as described in section III.B.(4). Fig. 8. (a) presents the frequency response of the system with different delay compensation strategies, based on which the damping ratio can be calculated as in Table II. It can be noticed that the performance under the fixed compensation deteriorated with the random delay, leaving a negative damping ratio at the target mode. The adaptive compensation with and without buffer yielded similar damping performance.

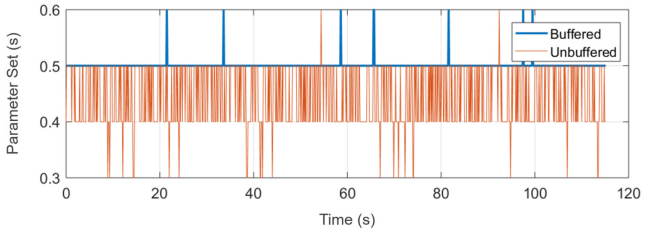
Fig. 8. (b) shows the actual delays of the measurement data used for control. The buffer case successfully kept the delay of the packages at around 500ms by waiting for them to mature in the buffer, except for a few instances where even the latest arrivals are already older than 500ms because of the network delay (blue spikes in the plot). As a result, the choice of compensation parameter set (the blue curve in Fig. 8. (c)) was kept at 500ms for most of the times, while the unbuffered case saw frequent switching among parameter sets of 300ms, 400ms, 500ms, and 600ms (the orange curve in Fig. 8. (c)). This well validated the purpose of the buffer, reducing compensation parameter switching while maintaining the good damping performance.



(a) Comparison of control performance with different compensations



(b) Delay of packages used for control



(c) Parameter sets chosen for measurements used for control

Figure 8. Results of the delay compensation and data buffer testing

TABLE II. COMPARISON OF DAMPING RATIO WITH DIFFERENT DELAY COMPENSATION STRATEGIES

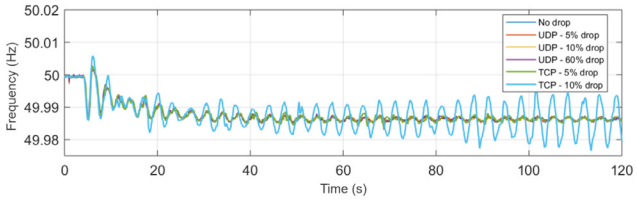
Compensation strategy	Damping Ratio (%)
Fixed compensation	-0.458
Adaptive comp. w/o buffer	6.483
Adaptive comp. w/ buffer	7.105

C. Data Drop and Communication Protocol Test

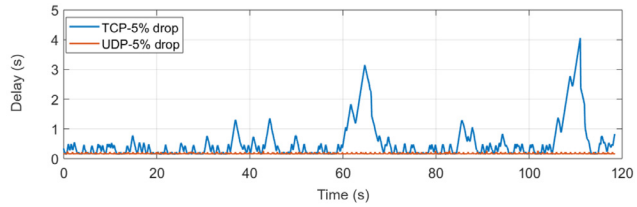
In addition to time delay, data drop is another common network uncertainty that may compromise the performance of the controller. In this test case, random data drop is introduced by the network simulator to investigate how the controller manages data loss under the TCP/IP (commonly used in PMUs for monitoring applications) and UDP/IP protocol. In the testing setup, the reporting rate of PMUs (30 times per second) is much higher than the control execution rate (10 times per second), facilitating the comparison of TCP/IP and UDP/IP under high data drop testing scenarios. Such practice is typical in control systems since it reduces the unnecessary delays caused by the pace mismatch and improves system reliability.

Fig. 9. (a) shows the frequency oscillation triggered by the 1st event with different communication protocols and data drop rates. With the UDP/IP, the performance of the controller kept almost identical in 5%, 10%, and 60% data drop cases. However, the performance with TCP/IP deteriorated under 5%, and the damping ratio turned negative when the data drop rate reached 10%. Fig. 9 (b) shows the actual delay of the packages used for control. It can be noticed that the data drop caused a drastic increase in the delay of the packages used for control in the TCP/IP case, hitting 4 seconds in the 5% case. The delay skyrocketed to 30 seconds in the 10% case. Such a level of delay will fail the controller or trigger the supervisory control module to switch to backup PMU channels available. However, the delays in 5% and 10% drop cases with UDP/IP are both kept near the inherent 150ms delay. This is because the UDP/IP prioritizes timely updates and ignores packages lost, while the TCP/IP induces extra cost to retransmit and ensure reliable transmission of the data.

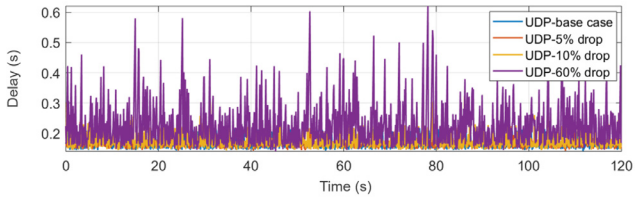
Fig. 9. (c) further shows a comparison of delays under UDP/IP with data drop rates from base case (0%), 5%, 10%, to 60%. It can be noted that the 0%, 5% case, and 10% case all saw delays very close to the inherent delay, which means the data drop caused little impact on the delay of packages used. Even with a data drop rate as high as 60%, the inflicted delays are lower than 600ms, mostly under 300ms. This is well within the delay compensator's capability to maintain the damping performance. Hence, the UDP/IP is recommended for a steadier data flow, especially in non-dedicated networks.



(a) Comparison of performance under different drop rates and protocols



(b) Delay seen by the WADC under 5% data drop



(c) Delay seen by the WADC in UDP test cases

Figure 9. Results of the data drop and protocol testing

V. Conclusions

To enable future field deployment of the measurement-driven-model-based WADC, hardware implementation of the controller and construction of the HIL testing platform have been accomplished. In addition to basic modules for realizing the control, auxiliary modules in the hardware WADC improve the controller's reliability and resiliency in realistic operating conditions. The HIL testing platform created a more comprehensive testing environment for the controller, introducing measurement errors and various types of uncertainties in the communication network. The effectiveness of the controller in increasing the system damping has been verified by thorough HIL testing. The controller was able to handle random time delays with adaptive delay compensation and data buffer, and it was more tolerant of high random data drop rates under the UDP/IP protocol than TCP/IP. The implementation of the WADC and the HIL testing composed an iterative design process that helped improve the design of the controller, as well as the HIL setup. The testing provided valuable findings and experience that could be leveraged in potential future field applications of the WADC. Future work will include the implementation of the online model identification module and field deployment at TERNA.

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