β-Ga_2O_3 FinFETs with ultra-low Hysteresis by Plasma-Free Metal-Assisted Chemical Etching

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Abstract—**In this work, β-Ga_2O_3 FinFETs with MOCVD grown epitaxial Si-doped channel layer on (010) semi-insulating β-Ga_2O_3 substrates are demonstrated. β-Ga_2O_3 fin channels with smooth sidewalls are produced by the plasma-free metal-assisted chemical etching (MacEtch) method. A specific on-resistance ($R_{on,sp}$) of 6.5 mΩ·cm^2 and a 370 V breakdown voltage are achieved. In addition, these MacEtch-formed FinFETs demonstrate DC transfer characteristics with near zero (9.7 mV) hysteresis. The effect of channel orientation on threshold voltage, subthreshold swing, hysteresis and breakdown voltages are also characterized. The FinFET with channel perpendicular to [102] direction is found to exhibit the lowest subthreshold swing and hysteresis.**

Beta-Gallium Oxide (β-Ga_2O_3) has drawn tremendous attention in power-electronics due to its ultra-wide band gap (4.8 eV),[1,2] high breakdown field (8 MV/cm), and reasonable 150 cm^2/V-s electron mobility,[3] leading to a 1721 Baliga's figure of merit. In addition to the high Baliga's figure of merit that outperforms SiC and GaN,[4–6] single crystalline bulk substrate with wide range of controllable *n*-type doping concentration[7,8] is also available for β-Ga_2O_3. Over the past decade, plenty of high power β-Ga_2O_3 devices, such as metal–semiconductor field-effect transistors (MESFETs),[9] metal–oxide–semiconductor field-effect transistors (MOSFETs),[10–13] vertical transistors[14–16] and Fin field-effect transistors (FinFETs),[17] with breakdown voltage (V_{br}) over 2.6 kV[18] and specific on-resistance ($R_{on,sp}$) down to 2 mΩ-cm^2 have been

demonstrated.[18] Nonetheless, the reported β-Ga_2O_3 transistors so far still suffer from low drive current and $R_{on,sp}$ compared to GaN devices. A solution to this issue is fabricating β-Ga_2O_3 transistors with high aspect ratio channels. Since $R_{on,sp}$ is normalized to device area for top-view, increasing channel aspect ratio would create an enhanced drive current but still remains low in device area, leading to a reduced $R_{on,sp}$.[19] Therefore, the development for transistors with high aspect ratios and smooth sidewalls is crucial for β-Ga_2O_3.

Although a β-Ga_2O_3 vertical transistor with an aspect ratio over 9.27 has been fabricated through reactive ion etching (RIE),[18] the high-energy ion induced damage and interface traps caused by RIE still degrades the device performance, leading to a limited 30 $cm^2/V{\cdot}s$ effective channel mobility.[20] In addition, the ion-induced damages typically result in notable hysteresis (200 mV – 2V) in all β-Ga_2O_3 transistors utilizing RIE process.[17,18] On the other hand, the plasma-free metal-assisted chemical etch (MacEtch) can produce a wide variety of 3D semiconductor structures with high aspect ratio and damage-free surfaces.[21–25] β-Ga_2O_3 fins with low interface trap density has previously been demonstrated by MacEtch,[26,27] and an almost hysteresis-free CV loop was achieved on the MacEtch-formed β-Ga_2O_3 MOSCAP structures, making it a promising etching technique for β-Ga_2O_3 transistor fabrication.

In this work, we demonstrate β-Ga_2O_3 FinFETs produced by MacEtch. The DC transfer and output characteristics, and breakdown voltage are fully characterized. The effect of channel orientation on threshold voltage (V_{th}), subthreshold swing (SS), hysteresis, and V_{br} are also studied.

Fig. 1 presents a schematic illustration of the process flow for β-Ga_2O_3 FinFET fabrication. First, a ~2 μm-thick lightly silicon-doped β-Ga_2O_3 film was grown on a (010) Fe-doped semi-insulating substrate by metalorganic chemical vapor deposition (MOCVD).[28,29] The doping concentration is around 4×10^{17} cm^{-3}. Then, channel and source/drain regions were defined through lithography followed by 30 nm Pt deposition by ebeam evaporation (Fig. 1). After standard lift-off process, the samples were immersed into a MacEtch solution consisting of a mixture of 49% HF and $K_2S_2O_8$,[27] to form fin-shaped channels and source/drain mesas (Fig. 1). Subsequently, the Pt was removed by aqua regia followed by 25 nm/20 nm Ti/Au films deposition with ebeam evaporation for source and drain contact. 20 nm of Al_2O_3 was then deposited through atomic layer deposition (ALD) process followed by 1 min of 490ºC rapid thermal annealing (RTA) with N_2 ambient to improve interface quality between Al_2O_3 and β-Ga_2O_3.[30] After the removal of Al_2O_3 on top of the source/drain mesa by HF, 25 nm/20 nm Ti/Au gold gate electrodes were then deposited on the high-k layer to form the gate stack. Finally, 1 min of 480ºC RTA under N_2 ambient was applied for source/drain ohmic contact formation.

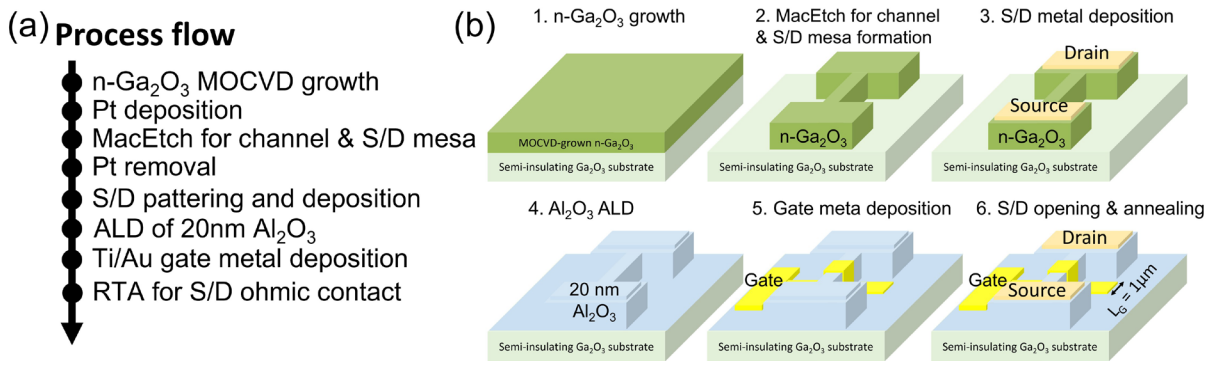

Fig. 1 (a) Process flow and (b) schematic diagram of β-Ga_2O_3 FinFET fabrication.

A trapezoid-like fin shape channel was first formed using the MacEtch process.[26] Fig. 2 (a) and (b) show the tilted-view and focused ion beam (FIB) cut cross-section SEM images of a fully fabricated β-Ga_2O_3 FinFET. Note that the source/drain mesa height of 3.57 μm is larger than the thickness of epitaxial n-type β-Ga_2O_3 film (2 μm), suggesting the fin channel consists of both the n-Ga_2O_3 epitaxial layer and the semi-insulating substrate. This divides the structure into two parts: a much wider triangular part at the bottom (highlighted in red, Fig. 2(b)) and a narrow fin on top (highlighted in blue). Due to the nature of carrier transport process in MacEtch,[25,27,31–33] β-Ga_2O_3 MacEtch is also found to be dependent on the doping concentration.[34] Therefore, the sharp transition line on the sidewall is indictive of the interface between the top n-Ga_2O_3 layer and the semi-insulating substrate. The active n-channel of the device is 142/570 nm in top/bottom width and ~ 1.5 μm in height, leading to an aspect ratio of 4.2:1 using the average fin width (Fig. 2(b)). Moreover, a smooth sidewall morphology can be observed on the MacEtch-formed structures (Fig.

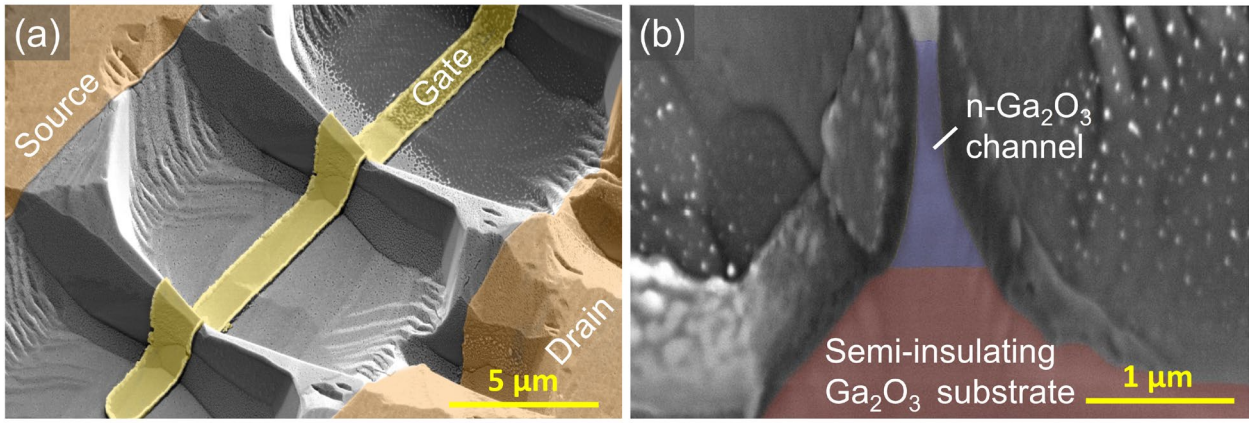

Fig. 2. (a) Tilted and (b) cross-section SEM images of β-Ga_2O_3 FinFETs formed by MacEtch. Note that the distance between source and drain is 5 μm and the SEM images are colored for identification. The tiny particles covering the FinFET in (b) are Au particles deposited after the IV measurement to reduce the charging issue and acquire SEM images with better-quality.

S1) compared to the rough sidewall produced by typical RIE processes. Note that the 1.5 μm fin height is smaller than the epitaxial n-Ga_2O_3 thickness (2 μm), suggesting the top parts of fins might be removed in the MacEtch process due to side etching.

Fig. 3(a) shows the DC transfer characteristics of the MacEtch-formed β-Ga_2O_3 FinFETs with 1 μm gate length (L_G) and 630 nm top fin width ($W_{fin,top}$) under V_{ds} = 5 V. At V_{gs} = 4 V, the drive current reaches 2.7×10^{-5} A/fin or 26.7 mA/mm when normalized to the bottom width of the active fin channels (blue region in Fig. 2(b)). The on/off ratio is ~10^5 with gate leakage current at 100 pA level, suggesting that a gate stack with good control and low leakage is formed. DC transfer characteristics of β-Ga_2O_3 FinFETs with different fin widths are shown in Fig. 3(b). With L_G = 1 μm and V_{ds} = 10 V, V_{th} values are found to be highly dependent on the fin dimension, causing the FinFETs to shift from depletion mode (normally on) to enhancement mode (normally off) as the fin width decreases. As expected, a more negative gate bias is required to deplete the channel and turn off the device with increasing fin width. The V_{th} dependence on fin width also provides a general guideline to design transistor operation mode depending on the applications. In addition to V_{th}, SS are extracted to be 93.6, 84.5, and 89.9 mV/dec. for 550, 330 and 200 nm $W_{fin,top}$, respectively. With $SS = \frac{kT}{q} ln10 \cdot (1 + \frac{C_D + q \cdot D_{it}}{C_{ox}})$,[35] where C_D, D_{it} and C_{ox} are the depletion capacitance, interface trap density and oxide capacitance, respectively, the upper bond of D_{it} in the MacEtch-formed β-Ga_2O_3 FinFETs is estimated to be around 1.4×10^{12} $cm^{-2} \cdot eV^{-1}$, which is not far from the CV measurement results of MacEtch-formed vertical MOSCAPs.[26] This indicates the MacEtch process does not damage the surface and has created an interface with superior D_{it} between Al_2O_3 and β-Ga_2O_3.

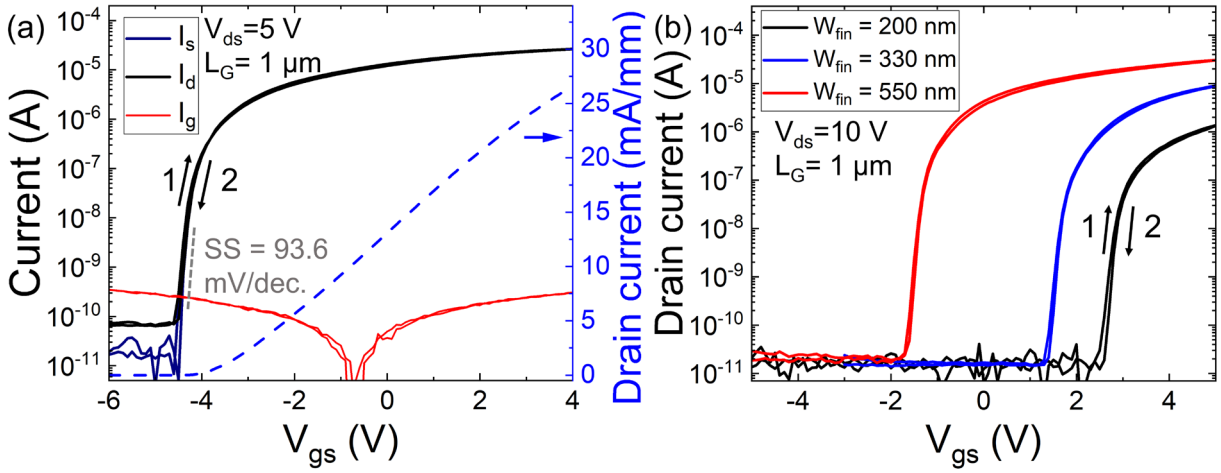

Fig. 3 (a) DC transfer characteristic of β-Ga_2O_3 FinFET in semi-log and linear scale. The channel orientation is 80° from [102] direction and $W_{fin,top}$ = 630 nm. (b) Transfer characteristic of β-Ga_2O_3 FinFETs with different $W_{fin,top}$ and channel perpendicular to [102] direction.

Note that all the transfer characteristics showed almost zero hysteresis (ΔV_{th} between voltage sweep 1 and 2 shown in Fig. 3(a)), which is unprecedented for β-Ga_2O_3 FETs with vertical sidewall structures. The largest hysteresis is only 9.7 mV clockwise, which is dramatically reduced compared to the 120 – 800 mV hysteresis of previously reported β-Ga_2O_3 FETs.[14,18,36,37] This nearly hysteresis-free characteristic could be attributed to the absence of RIE-induced ion damages and traps due to the MacEtch nature and is consistent with the CV results of MacEtch-formed β-Ga_2O_3 MOSCAPs.[26]

Fig. 4(a) shows the linear transfer characteristics at V_{ds} = 5 V for the β-Ga_2O_3 FinFET. The output characteristics with L_G = 1 μm and $W_{fin,top}$ = 630 nm is shown in Fig. 4(b). At V_{gs} = 2V and V_{ds} = 10V, a 24.4 mA/mm drain current is achieved. On resistance (R_{on}) can be extracted from the slope of low V_{ds} region. With the fin width extracted from the cross-section SEM images (blue region in Fig 2(b)), the R_{on} is estimated to be around 128.8 Ω-mm at V_{gs} = 2V. Thus, the $R_{on,sp}$ is around 6.5 mΩ-cm^2 when normalized to the distance between source and drain (5 μm). If we consider the source/drain contact transfer length (L_T) as 1μm, the $R_{on,sp}$ = R_{on} × gate width × (L_{SD}+2L_T) can be extracted as 9.1 mΩ-cm^2. Note that since the carrier concentration at source/drain is only from the intrinsic doping during the MOCVD growth (~4×10^{17} cm^{-3}), the 1 μm transfer length could be an overestimation. As a result, the 9.1 mΩ-cm^2 of $R_{on,sp}$ when considering L_T might also be overestimated. On the other hand, the $R_{on,sp}$ is expected to be further reduced though additional ion implantation to increase source/drain doping concentration, leading to a decreased contact resistivity and parasitic source/drain resistance.

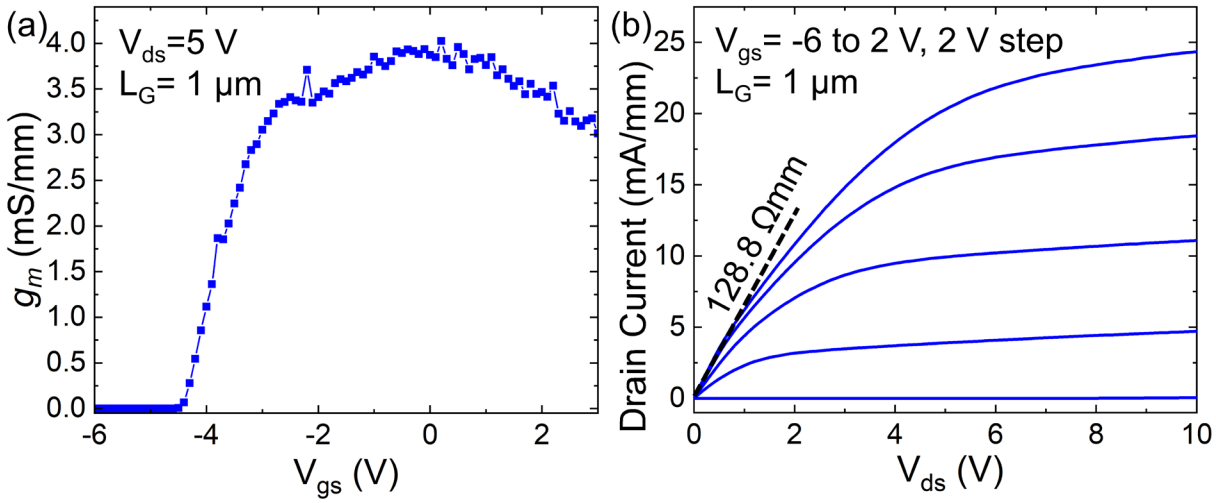

Fig. 4 (a) linear transfer characteristics and (b) output I-V characteristics of β-Ga_2O_3 FinFET. The channel orientation is 80° from [102] direction and $W_{fin,top}$ = 630 nm. Note that the g_m and current is normalized to the bottom width of active fin channel region (yellow-colored region in Fig.2 (b)).

With the asymmetric crystal structure of β-Ga_2O_3, it has also been reported that the channel orientation affects the β-Ga_2O_3 transistor characteristics.[18] The DC transfer characteristics of β-Ga_2O_3 FinFETs with ~ 750 nm $W_{fin,top}$ and different channel orientations are shown in Fig. 5(a). At V_{ds} = 10 V and V_{ov} = ~5 V, the drain currents are ~2×10^{-5}, 2.3×10^{-5} and 1.9×10^{-5} A for θ = 60°, 85°, and 90°, respectively. This shows all the drive current saturates at a similar level and suggests the channel mobility does not vary much with the orientation. Nonetheless, a clear voltage shift of the I_d-V_{gs} curves can be observed as the channel orientation changes. To further analyse this shift, the V_{th} of β-Ga_2O_3 FinFETs with similar $W_{fin,top}$ (~750 nm) and different channel orientations are extracted and plotted in Fig. 5(b). When θ, the angle between the channel direction and [102], is 60° (Fig. 5(b)), a -0.9 V V_{th} is observed. Then, the V_{th} becomes more negative as the fin rotates away from [102] direction and reaches its minimum at -6.9 V when the channel is counter-clockwise 90° from [102] direction. As the angle becomes larger than 90°, the V_{th} starts to increase again as the channel is more aligned with [102]. This V-shaped V_{th} distribution has also been reported in (001) β-Ga_2O_3 vertical transistors[18] and could be attributed to two reasons: first, as shown in our previous work,[26] the fin sidewalls become more vertical as the fin orientation approaching 90° from [102]. This leads to a wider channel width and thus a more negative bias to deplete the channel. Therefore, a most negative V_{th} at 90° is expected. On the other hand, the interface trap quantity on the sidewalls has also been reported to vary with the fin orientation.[26] As a result, this V_{th} trend might also imply that the interface traps on sidewalls decrease as the channel getting more perpendicular to [102] direction; and the sidewalls have the lowest interface trap

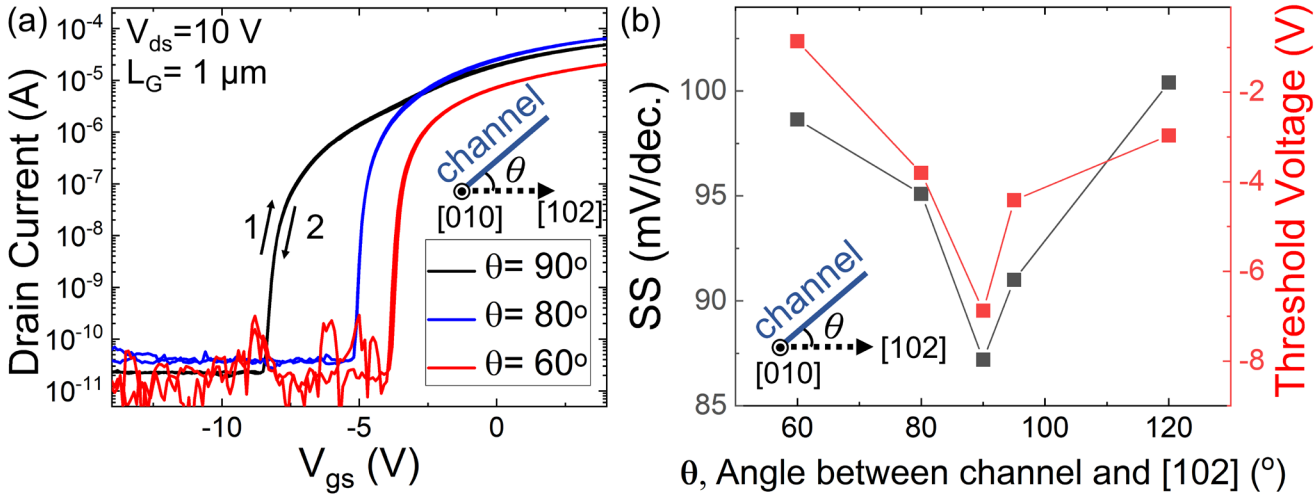

Fig. 5 (a) DC transfer characteristics of β-Ga_2O_3 FinFETs with different channel orientations. (b) Subthreshold swings and threshold voltages of β-Ga_2O_3 FinFETs vs θ, the angle between channel orientation and [102] direction. Note that $W_{fin,top}$ = 741, 735, 750, 724 and 747 nm for the devices with θ =60°, 80°, 90°, 85° and 120°, respectively.

density and negative interface charges, leading to the lowest V_{th}. It is also likely that these two factors both contribute to this V_{th} variation.

To further analyze the impact of these sidewall interface trap densities on the transistor performance, the SS of β-Ga_2O_3 FinFETs with different channel orientations are also extracted (Fig. 5(b)). SS decreases as the channel orientation rotates away from [102] and reaches its minimum value of 87.2 mV/dec. at θ =90°. Like the V_{th}, the SS vs fin orientation also shows a V-shaped distribution. The SS can be modeled as $SS = \frac{kT}{q} ln10 \cdot (1 + \frac{C_D + q \cdot D_{it}}{C_{ox}})$,[35] where C_D, D_{it} and C_{ox} are the depletion capacitance, interface trap density and oxide capacitance, respectively. Accordingly, the V-shaped distribution of SS suggests that the interface trap density could be the lowest on the MacEtch-formed sidewalls when θ =90°, consistent with the previous observation on V_{th}.

In addition to SS, the hysteresis of I_d-V_{gs} curves also reflects the device and interface quality of β-Ga_2O_3 FinFETs. Thus, We have examined the hysteresis for MacEtch-formed devices with different orientations. As shown in Fig. 6 (a), the hysteresis vs θ also demonstrate a similar V-shaped distribution with the minimum hysteresis (24 mV) at θ =90° (Fig. 6(a)). It was reported that the interface quality (i.e. D_{it}) had a direct impact on the hysteresis of the RIE-fabricated β-Ga_2O_3 FETs.[38] Therefore, this V-shape hysteresis might imply that sidewalls have the lowest D_{it} when the channel is perpendicular to [102] direction, in agreement with the previous results on V_{th} and SS.

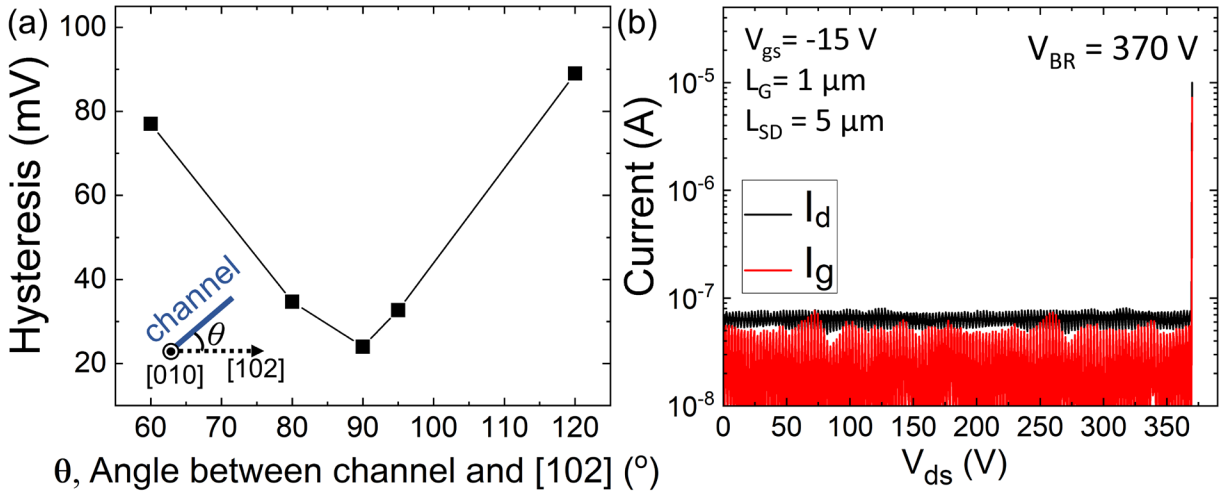

Fig. 6 (a) Hysteresis of β-Ga_2O_3 FinFETs vs θ, the angle between channel orientation and [102] direction. Note that $W_{fin,top}$ = 741, 735, 750, 724 and 747 nm for the devices with θ =60°, 80°, 90°, 85° and 120°, respectively. (b) three-terminal off-state I_d/I_g-V_{ds} characteristics and breakdown voltage of β-Ga_2O_3 FinFET ($W_{fin,top}$ = 630 nm, θ =80°).

Fig. 6 (b) shows the high-voltage off-state characterization of the β-Ga_2O_3 FinFETs (the same device as shown in Fig. 3 (a) and 4). A negative V_{gs} bias is applied to keep the device at off state. The gate and drain current remain low, at the detection limit of the tool, until breakdown at ~370V, where a spike in drain and gate current are observed. By assuming a one-dimensional electrical filed distribution ($E = V_{gd}/L_{GD}$), the electric field under the gate is estimated to be ~1.4 MV/cm when the breakdown occurs, which is smaller than the theoretical breakdown field of β-Ga_2O_3.[39] However, this simplified one-dimensional distribution is inaccurate for the FinFET structure. The simulated results show a significantly higher local electrical field occurs at the corner of the fin structure.[40] This could cause the breakdown to happen at a lower voltage compared to theoretical value. As a result, a greater breakdown voltage should be achieved in the future by incorporating field plate structures into the FinFETs[18,37].

Fig. 7(a) shows the average breakdown voltage of the FinFETs with different channel orientations. The V_{br} are within the range of 365 - 380 V and do not vary much with different θ, suggesting the interface properties might not play an important role in the breakdown mechanism. Fig. 7(b) shows the benchmark chart of reported β-Ga_2O_3 transistors in the literature. Note that the $R_{on,sp}$ values plotted are extracted from the slope for the family of curves at low V_{ds} region under V_{ov} = ~5V for all cited works. Then, the $R_{on,sp}$ are normalized to the area $W_g \times (L_{SD} + 2L_T)$ and plotted in Fig. 7(b). For those works not reporting L_T, and a 1 μm L_T is assumed for the calculation (raw data found in the cited work are plotted in Fig. S2 in the Supplementary Material). We believe this would provide a better reference point for benchmarking, since originally reported $R_{on,sp}$ in different papers are extracted with quite different V_{ov} (ranging from 3V to 100V).

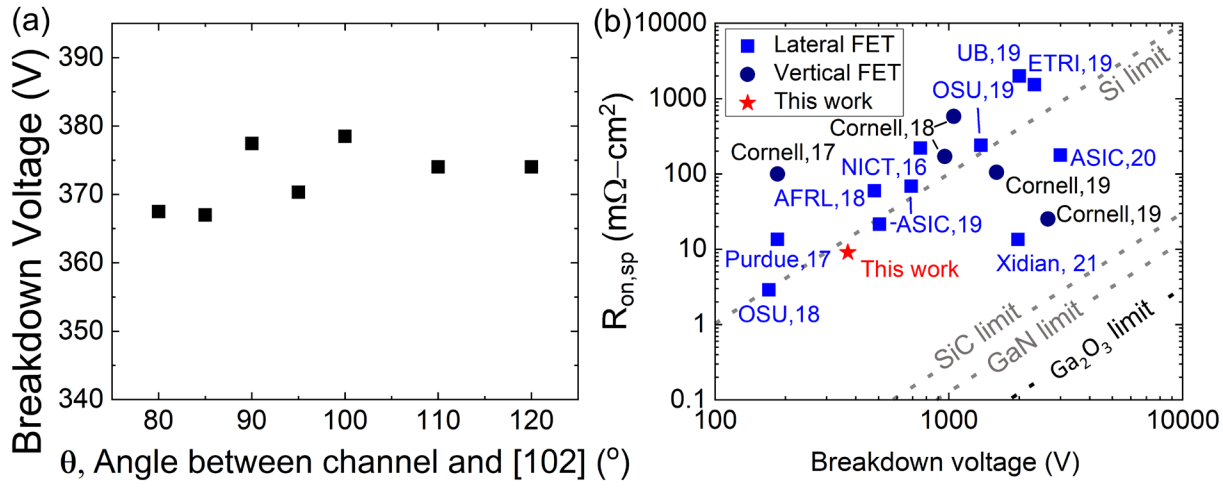

Fig. 7 (a) Breakdown voltages of β-Ga_2O_3 FinFETs vs θ, the angle between channel orientation and [102] direction. (b) $R_{on,sp}$ vs V_{br} benchmark plot of β-Ga_2O_3 FETs.[9,14,17,18,37,41–52]

An alternative version of benchmarking with originally reported $R_{on,sp}$ is also provided in Fig. S2. Here, the MacEtch-formed β-Ga_2O_3 FinFET demonstrates reasonable 370 V breakdown voltage and a 9.1 mΩ-cm^2 $R_{on,sp}$, which is relatively low compared to other reported β-Ga_2O_3 transistors. With the nearly zero hysteresis and comparable device performance, we believe this work represents a step towards three-dimensional β-Ga_2O_3-based power electronics with high quality interface.

In summary, β-Ga_2O_3 FinFETs, produced by MacEtch with channels of good aspect ratios and smooth sidewalls, are demonstrated. The devices show near hysteresis-free I_d-V_{gs} characteristics, presumably because of the absence of ion-induced damage, inherent to the MacEtch process. A 6.5 mΩ-cm^2 specific on-resistance and a 370 V breakdown voltage are achieved. The effect of channel orientation on V_{th}, SS, hysteresis, and breakdown voltages are also analysed. The results suggest the sidewalls possess the lowest interface trap density when channel is perpendicular to [102] direction and best suited for FinFETs.

SUPPLEMENTARY MATERIAL

Fig. S1 and S2 show the zoomed-in SEM image of the FinFET sidewall and the $R_{on,sp}$ raw data found in literature before normalization, respectively.

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DATA AVAILABILITY

The data that supports the findings of this study are available within the article and its supplementary material.

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