A 480-Multiplication-Factor 13.2-17.2 GHz Sub-sampling PLL Achieving 6.6 mW Power and -248.1 dB FoM Using a Proportionally Divided Charge Pump

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SSPLLs are superior for low phase noise high multiplication factor (M-factor) frequency synthesis, but require an extra frequency loop (FLL) to lock, which consumes inordinate power when M is large to ensure sufficient phase margin. This work presents a new SSPLL design (M=480) with a proportionally divided charge pump to break the power/stability tradeoff. It operates at 14.3GHz and achieves 6.6mW including the FLL, 153.4fs jitter and -248.1dB FoM, which is the best compared with PLLs with M>300.

Beyond-10GHz frequency synthesizers are ubiquitous building blocks for today's ever-growing wireless and wireline communication systems. To meet the stringent requirements on data rate and modulation schemes, the phase noise of the frequency synthesizers must be minimized. On the other hand, since low-noise and low-cost crystal oscillators operate at MHz range, a >10GHz frequency synthesizer demands a very large multiplication factor M (typically 400-1000), which poses new challenges. Although cascading PLLs helps reduce M per stage, it causes a significant power overhead and unwanted coupling between the two VCOs. Therefore, direct high M-factor frequency synthesis with low phase noise and low power consumption becomes a compelling approach.

Subsampling PLLs (SSPLLs) are superior for generating low phase noise signals, as the divider noise is eliminated, and further since the phase noise of the detector/charge pump (PD/CP) is not multiplied by M^2. The latter makes SSPLLs even more appealing when M is high since the PD/CP usually dominates the in-band phase noise. However, a divider-less SSPLL is prone to false frequency acquisition and external disturbances, which mandates adding an additional frequency lock loop (FLL) to output the correct frequency, as shown in Fig.1. With the dead-zone creation, the FLL-CP injects no current (and thereby no noise) to the

loop once the PLL is locked, thereby it has long been believed that the FLL-CP power can be minimized. However, for high M-factor SSPLLs, this can lead to severe stability issues. As illustrated in Fig.1, the loop transfer function of the FLL is the same as the subsampling loop, except that it is scaled by a constant number, i.e., loop gain ratio (LGR), which is defined as LGR = $M\times(K_{SS}/K_{FLL})$, where $K_{SS} = (I_{SS\text{-}CP}/V_{OV})\times 2A_{VCO}\times(T_{PUL}/T_{REF})$ and $K_{FLL} = I_{FLL\text{-}CP}/(2\pi)$ are the gain coefficients of the two PD/CPs. As apparent from the Bode plot, the LGR must be maintained close to unity to ensure a sufficient phase margin (PM) for both loops. However, a substantial amount of power needs to be allocated to the FLL-CP to meet this goal when M is high. Taking M=500 as an example, assuming the overdrive voltage V_{OV}=0.2V, the VCO amplitude A_{VCO}=0.4V and the fractional pulse width T_{PUL}/T_{REF} = 1/20, having LGR = 1 requires the FLL-CP current to be 628 times higher than the SS-CP current. By contrast, if the two CPs burns the same power, the LGR jumps up to 628, which pulls the PM of the FLL to below 10°, even though the subsampling loop has a better than 55° PM, as shown in Fig.4(a). To save power, [1] duty-cycled the FLL aggressively, at the cost of an increase in the re-acquisition time upon a sudden lock failure. In [2], the FLL was replaced by a 150μW disturbance correction loop, but its lock range is limited, so that the PLL may still lose lock with large disturbances.

This work presents a SSPLL operating from 13.2-to-17.2 GHz with a multiplication factor M = 480. It dissipates only 6.6 mW including the FLL and achieves an integrated jitter of 153.4 fs. This is made possible by a new subsampling charge pump/loop filter (SS-CP/LF) topology, which breaks the tradeoff between the loop stability and the power consumption.

The block diagram of the proposed SSPLL is provided in Fig.2. The subsampling loop employs two copies of the SS-CPs with a current split ratio of 1 : η. They are controlled by the same VCO sampler while injecting current into two distinct nodes of the loop filter. The second injection node is created by adding another RC leg (R'_3-C'_3) to the loop filter, where $R'_3=R'_1$ and $C'_3=C'_1$. Otherwise the FLL remains unaltered. With this new topology, the transfer functions of the subsampling loop and the FLL are re-examined in Fig.2. Clearly, with

the proposed loop design, the subsampling loop and the FFL share the same pole locations but distinct zero locations. In addition to downshifting the FLL loop gain magnitude by a factor of LGR, its zero is also left-shifted by (1+η) from the subsampling loop zero, i.e., $\omega_{z,FLL} = \omega_{z,SS}/(1+\eta)$, which alters the loop gain phase of the FLL and improve its PM. Since the loop gain magnitude falls at 40dB/dec before the zero, the SS-CP current split ratio is set to $1+\eta=(LGR)^{1/2}$ so that the FLL PM is comparable with the subsampling loop.

It is critical to emphasize that the proposed SS-CP/LF does not incur any power or area penalty. Suppose that all the loop components are identical for the two PLLs in Fig.1 and Fig.2 except the SS-CP and the loop filter. Since the SS-CP in Fig.2 is formed by splitting the Fig.1 SS-CP by a ratio of 1:η, the power consumption remains the same. To maintain the same loop bandwidth, it requires that the total loop capacitance and the zero frequencies of the two PLLs be equal. It can be approximated that $C_1'=C_3'=C_1/2$, $C_2'=C_2/(1+\eta)$ and $R_1'=R_3'=2(1+\eta)R_1$. As the loop capacitor (and VCO) occupies most space for a SSPLL, the proposed design does not cost extra area.

Fig.3 provides the schematic of the proposed SS-CP implementing a current ratio of η=4. In the main path, the sampled VCO waveform is converted to current by a source degenerated g_m stage for a better linearity. The current is mirrored into five copies, four of which (k=1~4) have their output nodes O<k> and dump nodes D<k> connected respectively to create one SS-CP, whereas the remaining copy (k=0) forms the other SS-CP. In each SS-CP, the dump node tracks the output node through a rail-to-rail unity gain buffer, which eliminates the disruptive charge redistribution from D<k> to O<k> in the steady state. Since no current flows through R_3' at the steady state, the dc voltages of all the O<k> and D<k> are identical once the PLL is locked, and so the split ratio η is only affected by the random transistor mismatch and can be made very accurate. In addition, a dummy path is included to prevent BFSK modulation of the VCO tank and to improve the reference spur.

The efficacy of the proposed SS-CP/LF topology can be validated using the hypothetical M=500 SSPLL from the previous discussion, as depicted in Fig.4. Suppose the PM of the (classical) subsampling loop has been

optimized for a predefined damping factor ζ_{SS}, and now the SS-CP needs to be split proportionally to compensate the FLL at a given LGR (set by the power budget). With no action taken, the FLL PM quickly falls below 20° as LGR increases, as shown in Fig. 4(a). However, if the SS-CP splits at $\eta=(LGR)^{1/2}-1$, the FLL PM is always better than the SSPLL for all LGRs, as depicted in Fig.4(b). In practice, it is desirable to keep a constant current split η while varying the LGR for power and noise optimization. Fig.4(c) plots the FLL PM at various LGRs for η=4, which is still better than 60° even when the LGR is as high as 625. This proves the flexibility and robustness of the proposed SS-CP/LF topology.

A prototype SSPLL is fabricated in the 28nm bulk CMOS process. Fig.7 shows the chip micrograph with an active area of 0.24mm^2. The PLL uses a Class-B LC VCO with an additional tail LC tank as a noise filter. The VCO consumes 2.4mW power, measures -108.5dBc/Hz phase noise at 1MHz offset and exhibits a tuning range of 26.5%. The PLL has a M-factor of 480 with an input reference frequency at 30MHz, sourced from a signal generator (R&S SMA100A) during the measurement. Fig.5 shows the measured phase noise spectrum after an on-chip divide-by-2 frequency divider. The PLL operates at 14.23GHz. The measured PN at 1MHz offset is -112dBc/Hz, which corresponds to -106dBc/Hz at the PLL output. The integrated jitter (1kHz-100MHz) is 153.4fs and the in-band PN is dominated by the reference. The reference spur is -62.3dBc when translated to 14.23GHz. The PLL consumes 6.6mW in total (excluding the output pad driver) and the power breakdown is given in Fig.7. Thanks to the proposed SS-CP/LF, the FLL power is substantially reduced.

Fig. 6 benchmarks the proposed SSPLL with recent prior-art beyond-10GHz PLLs with M-factor >300. It achieves the best jitter, FoM_{JIT} and $FoM_{JIT,M}$.

References:

[1] H. Liu et al., "16.1 A 265μW fractional-N digital PLL with seamless automatic switching subsampling/sampling feedback path and duty-cycled frequency-locked loop in 65nm CMOS," ISSCC, 2019, pp. 256-258.

[2] Y. Lim et al., "17.8 A 170MHz-lock-in-range and −253dB-FoM$_{jitter}$ 12-to-14.5GHz subsampling PLL with a 150μW frequency-disturbance-correcting Loop using a low-power unevenly spaced edge generator," ISSCC, 2020, pp. 280-282.

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[4] D. Liao et al., "An mm-Wave synthesizer with robust locking reference-sampling PLL and wide-range injection-locked VCO," in IEEE Journal of Solid-State Circuits, vol. 55, no. 3, pp. 536-546, March 2020.

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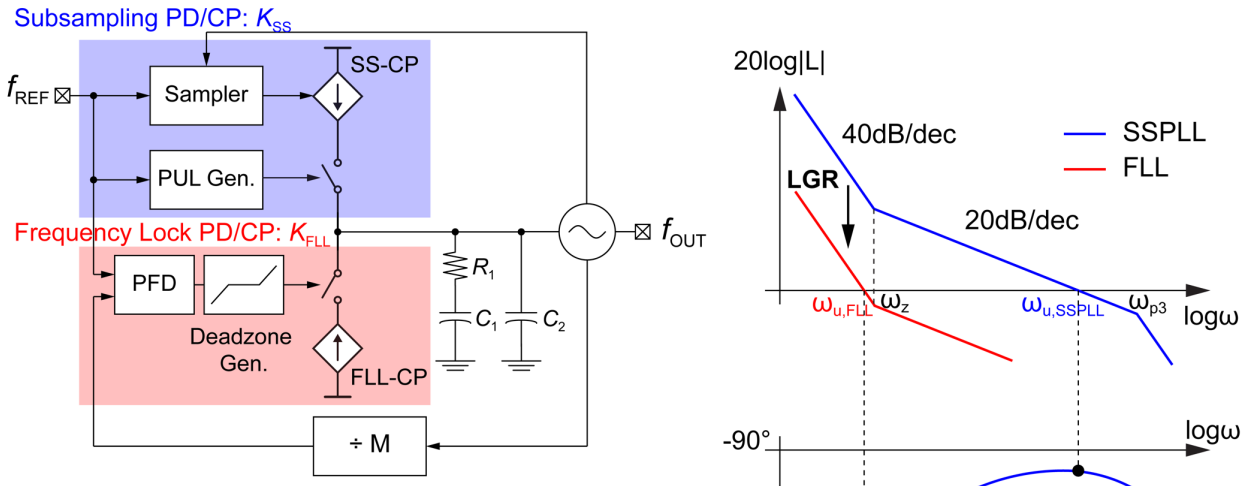
[6] A. Hussein et al., "19.3 A 50-to-66GHz 65nm CMOS all-digital fractional-N PLL with 220fsrms jitter," ISSCC, 2017, pp. 326-327.

[7] N. Markulic et al., "9.7 a self-calibrated 10Mb/s phase modulator with -37.4dB EVM based on a 10.1-to-12.4GHz, -246.6dB-FoM, fractional-N subsampling PLL," ISSCC, 2016, pp. 176-177.



Loop Transfer Function:

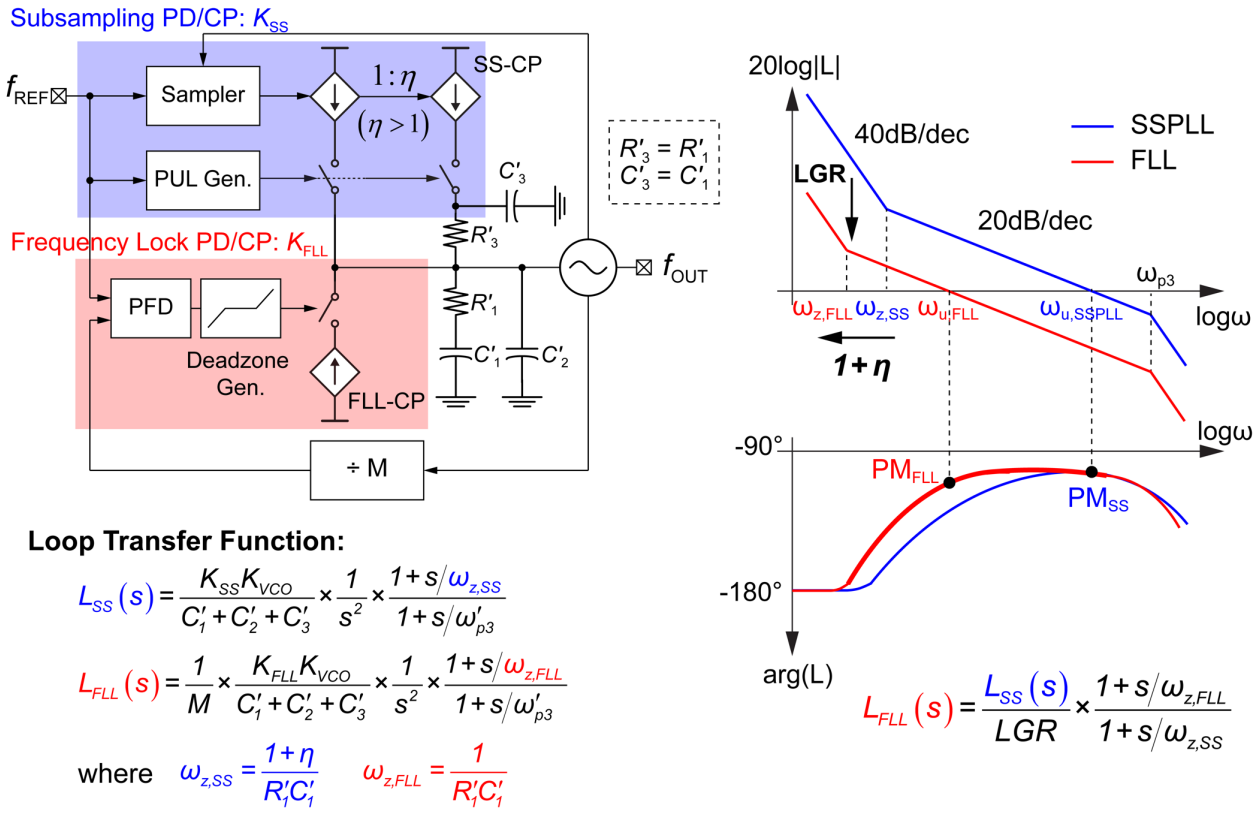
$$L_{SS}(s) = \frac{K_{SS}K_{VCO}}{C_1+C_2} \times \frac{1}{s^2} \times \frac{1+s/\omega_z}{1+s/\omega_{p3}} = K_{SS} \times L_0(s)$$

$$L_{FLL}(s) = \frac{1}{M} \times \frac{K_{FLL}K_{VCO}}{C_1+C_2} \times \frac{1}{s^2} \times \frac{1+s/\omega_z}{1+s/\omega_{p3}} = \frac{K_{FLL}}{M} \times L_0(s)$$

$$\rightarrow L_{FLL}(s) = \frac{L_{SS}(s)}{LGR} \quad \text{where} \quad LGR = M \times \frac{K_{SS}}{K_{FLL}}$$

$$L_{FLL}(s) = \frac{L_{SS}(s)}{LGR}$$

Fig.1: Classical SSPLL with frequency locked loop block diagram. The loop transfer functions exhibits stability issues for the FLL loop due to the mismatch in gain.



Loop Transfer Function:

$$L_{SS}(s) = \frac{K_{SS}K_{VCO}}{C'_1+C'_2+C'_3} \times \frac{1}{s^2} \times \frac{1+s/\omega_{z,SS}}{1+s/\omega'_{p3}}$$

$$L_{FLL}(s) = \frac{1}{M} \times \frac{K_{FLL}K_{VCO}}{C'_1+C'_2+C'_3} \times \frac{1}{s^2} \times \frac{1+s/\omega_{z,FLL}}{1+s/\omega'_{p3}}$$

where $\omega_{z,SS} = \frac{1+\eta}{R'_1C'_1}$ $\omega_{z,FLL} = \frac{1}{R'_1C'_1}$

$$L_{FLL}(s) = \frac{L_{SS}(s)}{LGR} \times \frac{1+s/\omega_{z,FLL}}{1+s/\omega_{z,SS}}$$

Fig.2: Proposed SSPLL with frequency locked loop, showing a new charge pump/loop filter topology to solve the stability and power trade-off.

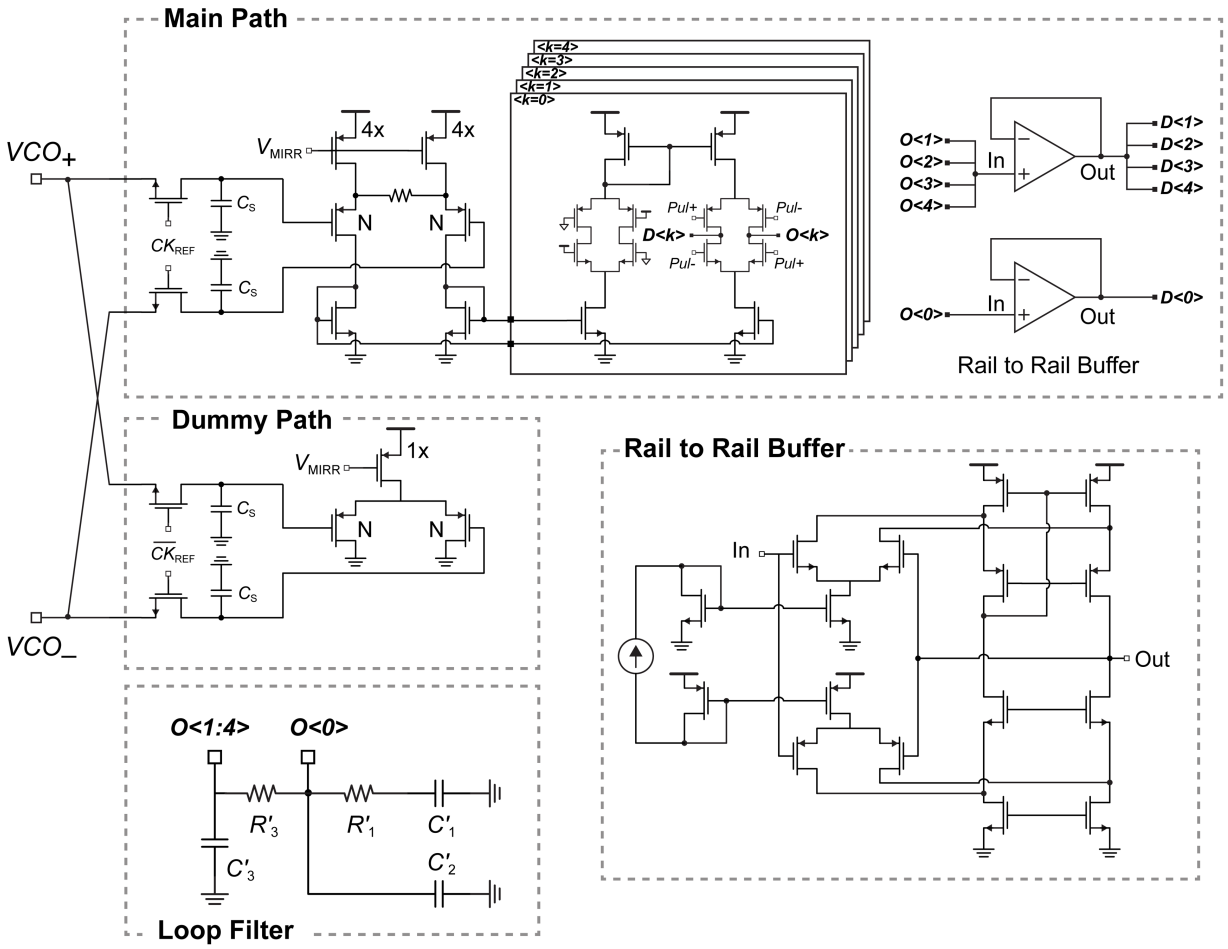
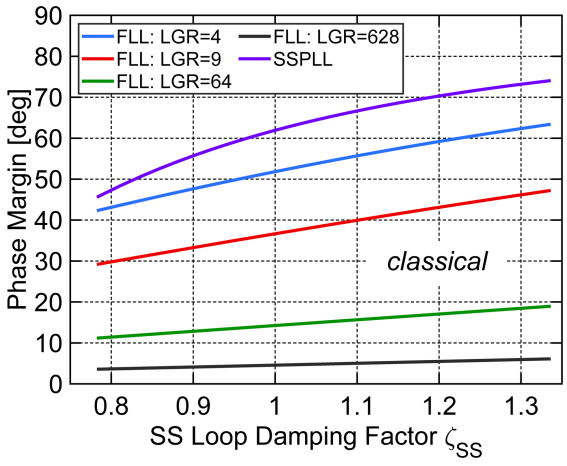


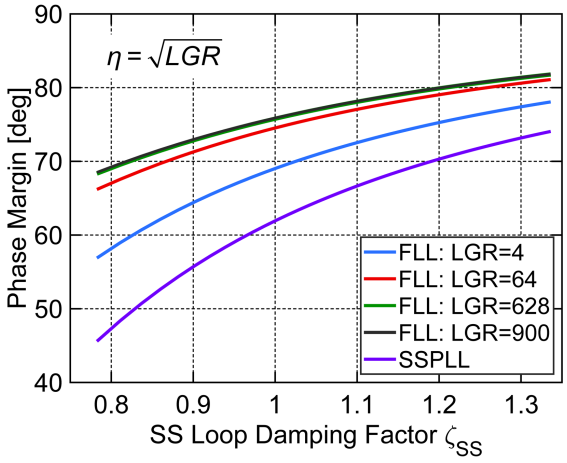
Fig.3: Schematic of the proportionally divided subsampling charge pump and loop filter, realizing a current ratio of η = 4.



LGR	CP Current Ratio $I_{FLL\text{-}CP}/I_{SS\text{-}CP}$
1	628
4	157
64	10
628	1.0
900	0.7

* M = 500

$A_{VCO} = 0.4\ V,\ V_{OV} = 0.2\ V,\ \frac{T_{PUL}}{T_{REF}} = \frac{1}{20}$



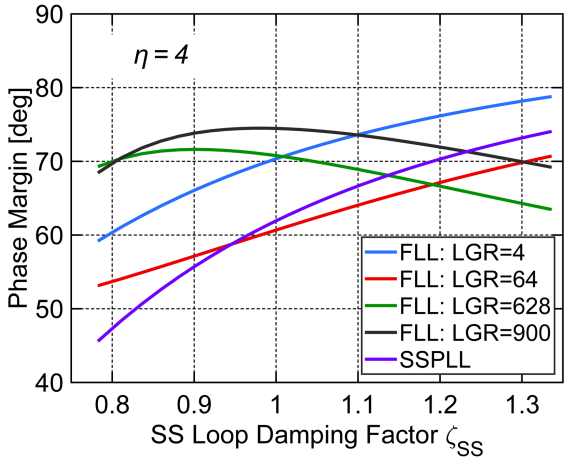


Fig.4: Phase margin of different SSPLL loop configurations. The proposed topology improves the stability and power of the frequency locked loop simultaneously.

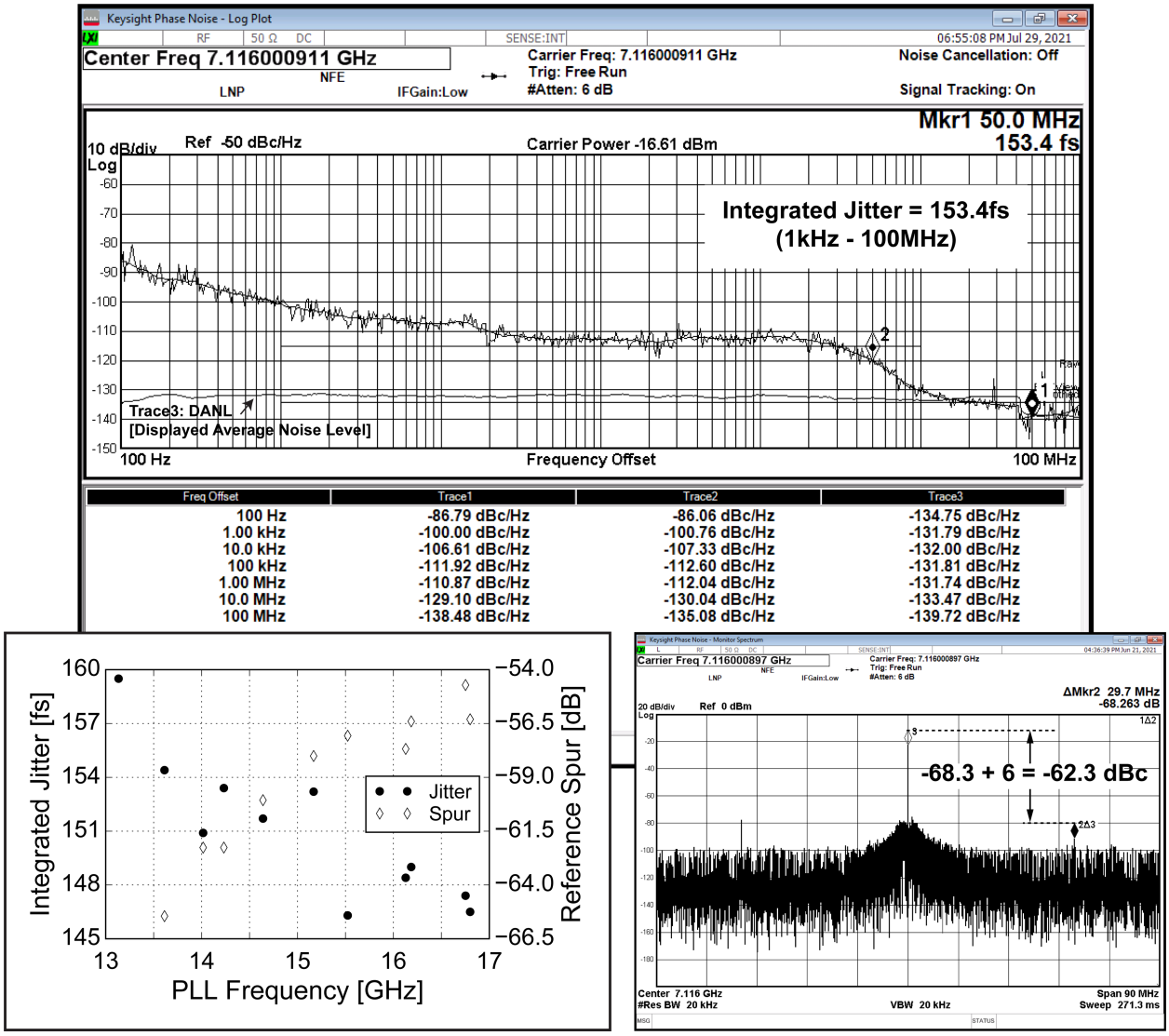


Fig.5: Measured phase noise and spur of the PLL output signal at the center frequency and across the tuning range (after an on-chip divide-by-2).

	This Work		VLSI'21 [3]	JSSC'20 [4]	ISSCC'18 [5]	ISSCC'17 [6]	ISSCC'16 [7]
COMS Tech.	**28 nm**		28 nm	45 nm	65 nm	65 nm	28 nm
Architecture	**Analog SSPLL**		Digital ROSPLL	Analog RSPLL + ILFM	Digital BBPLL	ADPLL	Analog SSPLL
f_{REF} [MHz]	**30**	**60**	50	80	52	100	40
f_{OUT} [GHz]	**13.2-16.5**		24-31	33.6-36	20.4-24.6	50.2-66.5	10.1-12.4
Multiplication Factor	**480**	**240**	576	448*	446	653	300
Power [mW]	**6.6**		11.55	20.6	19.7	46	5.6**
RMS jitter [fs] (Integration Range [Hz])	**153.4 (1k-100M)**	**116.5 (1k-100M)**	199 (10k-30M)	251 (10k-10M)	213 (10k-26M)	258.4 (1k-40M)	197.8 (10k-40M)
Reference Spur [dBc]	**-62.3**	**-57.2**	-65	-60	-	<-59.1	-69
PLL $\mathrm{FoM_{JIT}}$ [dB]	**-248.1**	**-250.5**	-243.3	-238.9	-240.5	-235.1	-246.6**
PLL $\mathrm{FoM_{JIT,M1}}$ [dB]	**-274.9**	**-274.3**	-270.9	-265.4	-267.0	-263.3	-271.3**
PLL $\mathrm{FoM_{JIT,M2}}$ [dB]	**-248.1**	**-247.5**	-241.1	-234.6	-238.1	-229.9	-245.4**
Area [$\mathrm{mm^2}$]	**0.24**		0.3	0.41	0.48	0.45	0.77

$\mathrm{FoM_{JIT}} = 10\log_{10}\left(\frac{\mathrm{Jitter}^2}{(1\mathrm{s})^2} \cdot \frac{\mathrm{Power}}{1\mathrm{mW}}\right)$ $\mathrm{FoM_{JIT,M1}} = \mathrm{FoM_{JIT}} - 10\log_{10}\left(\frac{f_{\mathrm{OUT}}}{f_{\mathrm{REF}}}\right)$ $\mathrm{FoM_{JIT,M2}} = \mathrm{FoM_{JIT}} + 10\log_{10}\left(\frac{f_{\mathrm{REF}}}{30\ \mathrm{MHz}}\right)$

$\mathrm{FoM_{JIT,M1/M2}}$ reported in K.M.Megawer ISSCC'18, J.Kim ISSCC'19, Z.Yang ISSCC'19 and etc., because the PN does not scale by $\mathrm{M^2}$ for crystals and signal generators especialy when f_{REF} <100 MHz.

* Use cascaded PLL.
** FLL power not included.

Fig.6: Performance comparison with high multiplication factor frequency synthesizers.

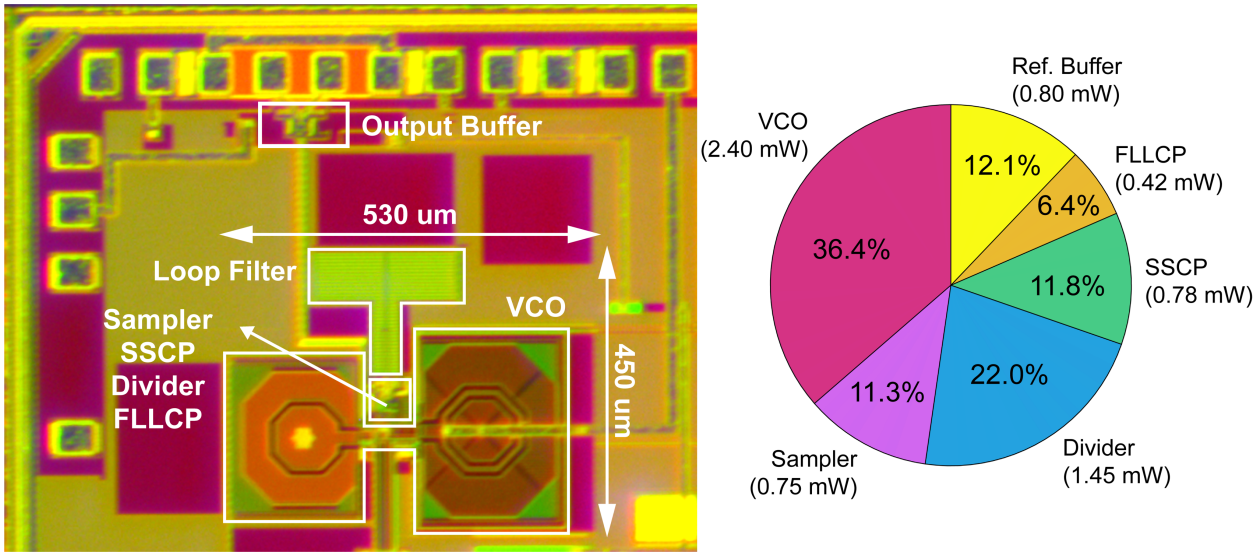


Fig.7: Chip micrograph and power consumption breakdown.

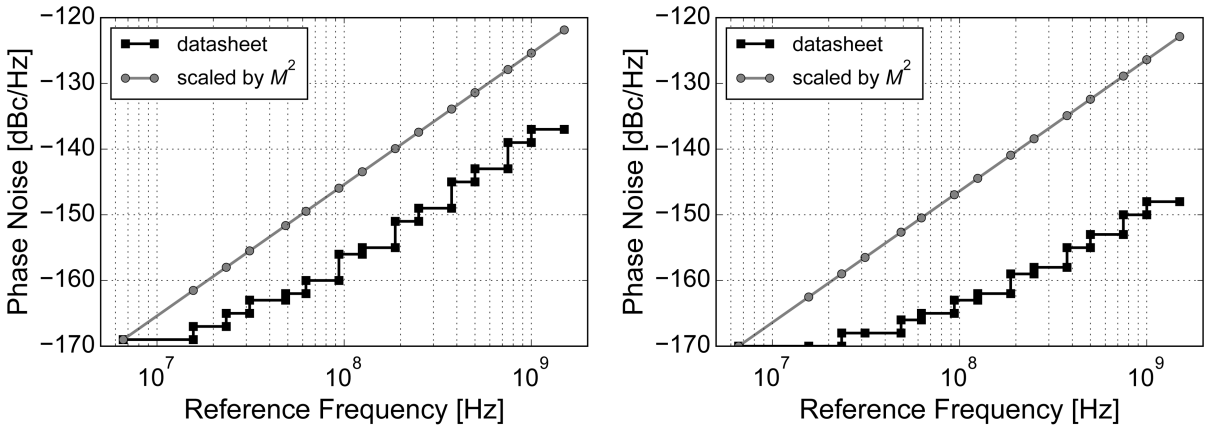


Fig.S1: Phase noise at 100kHz (left) and 1MHz (right) offset of the signal generator R&S SMA, which does not scale up by M^2. The datasheet is available online at https://www.rohde-schwarz.com/se/brochure-datasheet/sma100a/.