

A sleeve and bulk method for fabrication of photonic structures with features on multiple length scales

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Abstract. Traditional photonic structures such as photonic crystals utilize a) large arrays of small features with the same size and pitch and b) a small number of larger features such as diffraction outcouplers. In conventional nanofabrication, separate lithography and etch steps are used for small and large features in order to employ process parameters that lead to optimal pattern transfer and side-wall profiles for each feature-size category, thereby overcoming challenges associated with RIE lag. This approach cannot be scaled to more complex photonic structures such as those emerging from inverse design protocols. Those structures include features with a large range of sizes such that no distinction between small and large can be made. We develop a sleeve and bulk etch protocol that can be employed to simultaneously pattern features over a wide range of sizes while preserving the desired pattern transfer fidelity and sidewall profiles. This approach reduces the time required to develop a robust process flow, simplifies the fabrication of devices with wider ranges of feature sizes, and enables the fabrication of devices with increasingly complex structure.

Submitted to: *Nanotechnology*

1. Introduction

There is great interest in the development of on-chip quantum photonic platforms because they offer a potential path toward scaling to a large number of qubits while preserving the advantages of using photons for state initialization, manipulation, or readout.[1–4] The photonic elements that would comprise any such device often have features on very different length scales, including, for example, photonic crystals with holes of order 150nm and de-multiplexers or outcouplers of order microns.[5–10] To achieve the high fabrication quality required for high performance, features on different lengths scales are typically fabricated with separate etch processes. While this approach works well when all features can be classified into a few size categories, it begins to face challenges when device patterns have features spanning a wide range of sizes. This limitation is increasingly important with the emergence of inverse designed devices that contain abstract shapes with no distinct zones of regular feature size.[5; 11; 12]

We report development of a sleeve and bulk etch process for fabrication of nanomembrane devices with features on multiple length scales. We take as our test case photonic crystal devices in GaAs nanomembranes, which are well-established in optoelectronics.[13] From the point of view of quantum photonics, III-V devices provide the opportunity to incorporate InAs quantum dots and quantum dot molecules, which have excellent optical quality, as quantum emitters or the host for spin qubits.[6; 7; 9; 10; 14–16] Moreover, there has been extensive development for fabricating structures such as photonic crystal cavities, waveguides, and outcouplers in III-V materials.[9; 13] Two of the most important metrics of fabrication quality are high pattern

transfer fidelity and well-defined vertical sidewall profiles. Obtaining devices with both high pattern transfer fidelity and good sidewall profiles is challenging when fabricating features on multiple lengths scales because the depth of etch and the sidewall verticality obtained with Inductively Coupled Plasma (ICP) Reactive Ion Etching (RIE) can depend strongly on feature size.[13; 17] The dependence of etch rate on feature size, often called “RIE lag”, arises primarily from differences in the rates at which fresh etchant chemicals can be transferred into small features and etch byproducts removed. As a result of RIE lag, ICP etch recipes are traditionally optimized for production of a particular feature size. Two or more separate etch steps are then used to transfer the pattern for features of different size.[13]

The conventional approach of separate etch processes optimized for separate feature sizes provides good results when the features fall neatly into categories with similar size. This is often the case for manually- or analytically-designed devices such as the diffraction outcoupler shown in Fig. 1a.[18; 19]. Recently, a variety of more sophisticated optimization techniques have been employed to improve device performance, including the use of genetic algorithms and semi-analytical approaches.[20; 21] Even more sophisticated methods such as inverse design have enabled investigation of a wider range of design space and have produced devices with extremely small form factors and high performance.[22] As illustrated by the coupler shown in Fig. 1b, devices designed using methods such as inverse design often appear abstract and, more importantly, do not have features that can be easily classified as “small” or “large” for purposes of employing separately optimized etch processes. Even worse, individual objects can have sections of

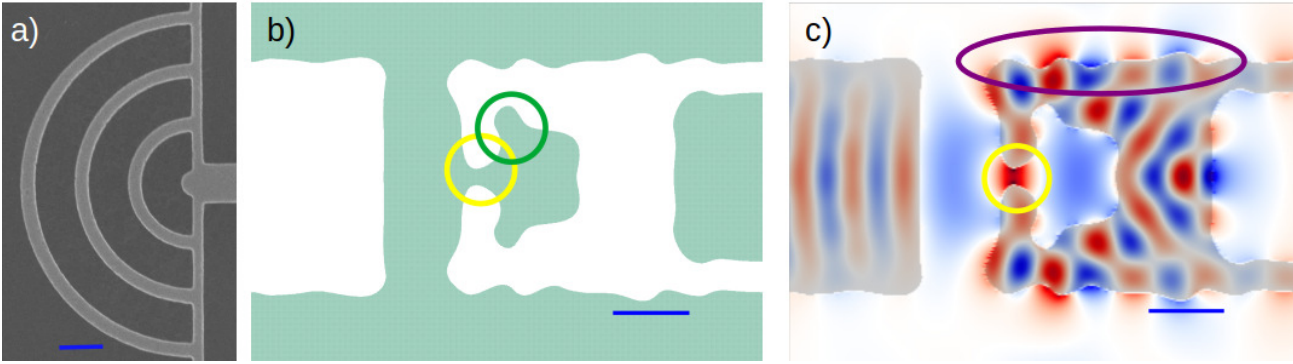


Figure 1. Representative device structures for a) traditionally designed photonic devices in which there is a clear distinction between small and large features (SEM image), and b) inverse designed photonic devices in which features span a wide range of sizes (GDS mask file). Difficult to fabricate tight corners and narrow necks are circled in green and yellow, respectively. c) FDTD simulations of the y-component of the electric field of the coupling mode of the inverse designed coupler shows the importance of profile sidewall in both ‘small’ and ‘large’ features. All scale bars are 500nm.

varying sizes. The majority of the coupler shown in Fig. 1b would be classified as ‘large’ ($\sim 500\text{nm}$), but it includes ‘small’ (sub-200nm) features as highlighted by the green and yellow circles. The importance of sidewall profile in these areas of varying size is illustrated by Fig. 1c, which shows Finite Difference Time Domain (FDTD) simulations of the electric field amplitude of this inverse designed coupler.[23] Both the ‘small’ region highlighted by the yellow circle and ‘large’ regions such as the outer edge indicated by the purple circle have high electric field amplitude, meaning that scattering from non-vertical sidewalls would introduce significant performance degradation. The traditional two-step large-or-small etch would force a choice between two bad outcomes: a) etch the feature in a single step, resulting in angled sidewalls at some locations due to RIE lag or b) splice the pattern between the large and small lithography and etch steps, resulting in line edge roughness due to alignment error. These limitations are important because the measured performance of photonic devices designed using methods such as inverse

design tends to fall short of the simulated performance, and this shortfall is typically attributed to fabrication imperfections such as reduced sidewall verticality.

Our approach is inspired by the sleeve and bulk electron beam lithography (EBL) technique that allows the boundary of a feature (sleeve) to be dosed with a more accurate and contrasting low current beam while maintaining a fast write speed with a higher beam current for the bulk of the pattern.[24] In our approach, we first define (by EBL) a thin sleeve that defines the boundary of any feature. We then etch this sleeve using a process designed to achieve good sidewall profile for small features. After the sleeve etch, a second set of lithography and etch steps remove the bulk of the material, leaving the sidewalls largely protected by resist. This second etch can be designed to target critical components such as photonic crystal holes because the specific etch parameters do not affect the sleeve-defined sidewalls, which were protected by resist. The end result is a process that requires two (and only two) lithography and etch steps to deterministically transfer

the pattern and achieve good sidewall profiles regardless of the range of feature sizes present in the device design. We first describe the approach and the range of parameters we considered when developing and optimizing the method. We then describe the flexibility and limits of this approach.

2. Process flow Overview

2.1. Sample

Each sample is epitaxially grown on a GaAs substrate using molecular beam epitaxy (MBE) recipes similar to those reported previously. As shown in Fig. 2a, the top 145nm GaAs nanomembrane is the platform for all photonic elements. The $Al_{0.75}Ga_{0.25}As$ layer below the nanomembrane serves as a sacrificial undercut layer. The thickness of the suspended nanomembrane is chosen to provide total internal reflection for the target wavelength, resulting in confinement of light along the growth (vertical) direction.[18] This suspended membrane approach is well-established for photonic elements designed using both traditional and inverse design methods.[18; 20] The suspended membrane offers an important process flexibility for the sleeve and bulk etch method. Specifically, the depth of ICP etch into the AlGaAs layer is not important because all of the AlGaAs beneath the fabricated device will eventually be removed.

2.2. Fabrication Steps

The sleeve and bulk fabrication method proceeds in 7 steps, which are schematically depicted in Fig. 3. Below we describe the constraints, range of process parameters considered, optimization strategy, and final parameters for each step of the method.

Here we provide an overview of the complete optimized process. Prior to step 1 we define metal alignment markers by EBL. In step 1 we lithographically define the sleeve. As seen in Fig. 3a, the feature is undersized by twice the expected ICP size bias, with both sides of the feature moved in by the bias. In step 2 the pattern is transferred into the material by ICP etch. The sleeve width is biased larger during this step resulting in the designed feature width. In step 3 the sleeve etch mask is removed. In step 4 the bulk etch mask is defined via EBL. Note that the alignment constraint is that the line edge must be interior to the sleeve, which protects the feature walls with resist and leaves the bulk unprotected. In step 5 we remove the bulk of the feature via ICP etch. We note, and discuss further below, that there is significant process flexibility in the etch conditions used to remove the bulk. This flexibility allows the second etch step to be separately optimized for the features that most significantly impact photonic performance. In our case we optimized the etch in step 5 for photonic crystal features. In step 6 the resist mask is removed. Note that pattern overlap between the sleeve etch and the bulk etch can result in deep trenches into the undercut layer. This is not an issue because in step 7 we remove the $Al_{0.75}Ga_{0.25}As$ undercut layer with an HF etch.

3. Process Development

3.1. Electron Beam Lithography

The sleeve and bulk approach requires ~ 45 nm scale precision in the alignment of multiple EBL lithography masks. The main requirement is for the bulk pattern boundary to be interior to the ~ 90 nm sleeve pattern. 45nm

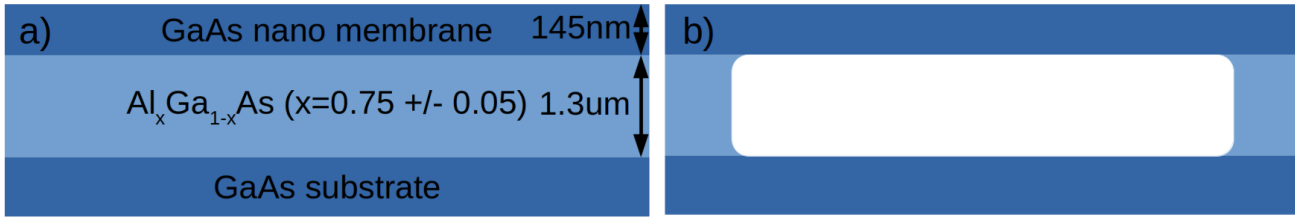


Figure 2. a) MBE-grown material stack consisting of a 145nm GaAs nanomembrane on top of a 1370nm $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ sacrificial undercut layer grown on a GaAs substrate. b) Representation of device after an HF wet etch removes the sacrificial $\text{Al}_{0.75}\text{Ga}_{0.25}\text{As}$ undercut layer, producing the air gap below the nanomembrane.

precision is well within the capabilities of most modern EBL systems; in fact, more precision is usually required for the alignment between photonic crystal elements and larger features such as beam waveguides and outcouplers when using traditional multi-etch methods. The sleeve and bulk approach is relatively insensitive to alignment error largely due to the width of the sleeve itself, which we discuss further below with respect to Fig. 3c. We have found that both etch pits and gold pads can be used as alignment marks to achieve the required precision.

The choice of resist thickness is very important to this process. Resist adhesion is a common problem for GaAs and high aspect (tall and narrow) resist features tend to fall over. The minimum size of sleeved features for a given resist thickness is limited because the resist between sleeves can only be so narrow before entering the high aspect regime where the resist pillar is not stable. On the other hand, small features etch slowly and have a reduced ICP etch selectivity, which requires a thicker resist profile in order to support longer etch times. We chose a resist spin speed of 3000RPM. A N=2 EBL multi-pass technique is used for the ICP etch mask to reduce line edge roughness. See the supplemental material for a detailed description of our EBL process parameters and further information on resist thickness and stability.

The sleeve write width for our optimized process is 62nm. While a thinner sleeve width would directly reduce the minimum feature size, we found that our sleeve writes with N=2 multi-pass became unreliable as the write width approached 30nm. We choose a width of 62nm to stay comfortably above this limit.

We note that we observe pattern size biasing during the ICP etch step. Specifically, and as described in more detail in the supplemental material, the features achieved after ICP etch are typically 30nm larger than the feature as defined by EBL. A sleeve width of 62 nm as defined by EBL thus results in an etched sleeve approximately 92 nm wide. The sleeve mask file is generated from the desired object geometry by creating a sleeve of width 62 nm that follows the contour of the outer perimeter of the desired object, but is inset from the outermost edge of the object by the etch bias of 15 nm. This ensures that the etched sleeve, including the bias, has the desired outer perimeter. The bulk mask is defined by the feature with the perimeter reduced to the center of the sleeve pattern. This method ensures that a) the sidewalls defined by the sleeve etch will be fully protected during the bulk etch and b) the bulk etch will remove all material from the center of the object even when there is imperfect alignment between the sleeve and bulk EBL lithography steps.

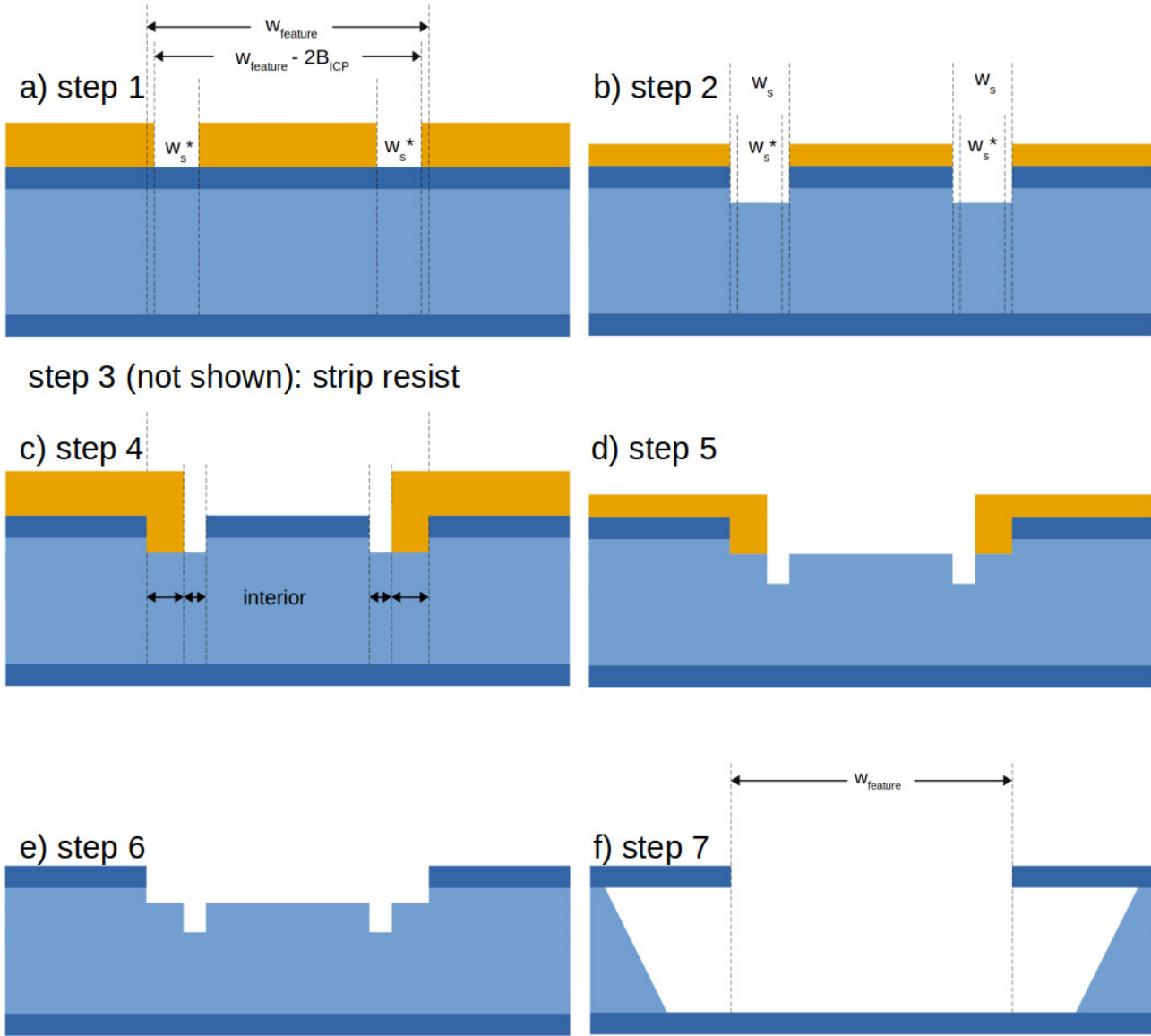


Figure 3. Schematic representation of lithography, etch and undercut steps in the sleeve and bulk fabrication process. w_{feature} represents the features intended width. B_{ICP} represents the biasing (in nm) of features which is dominated by the isotropic component of the ICP etch. w_s^* and w_s represent the written sleeve width and the resulting sleeve width which differ by twice the biasing. Dark blue represents the GaAs membrane and substrate, light blue represents the AlGaAs membrane, and yellow represents the resist mask. A detailed discussion of these process steps is found in Section 2.2.

3.2. ICP sleeve and bulk etches

The focus of this report is the sleeve and bulk two-step etch process. In the first step a sleeve defines the outer edge of all features larger than 310nm. This feature is then etched into the GaAs nanomembrane via Cl-ICP using etch conditions optimized for

the specific sleeve width. We describe the range of sleeve widths and etch conditions we evaluated below. In the second step the bulk is removed. The same etch conditions developed for the first step can be used because larger features etch faster and the sidewall as defined in the sleeve etch is protected by resist.

However, it is also possible to choose bulk etch conditions that are optimized for specific features such as the small regularly-sized holes in a photonic crystal. This provides significant flexibility for separate optimization of the etch for the features that most significantly impact photonic performance. The key point is that the specific etch recipe used in the second step does not matter as long as the bulk is removed. See the supplemental information for a detailed description of our etch optimization process.

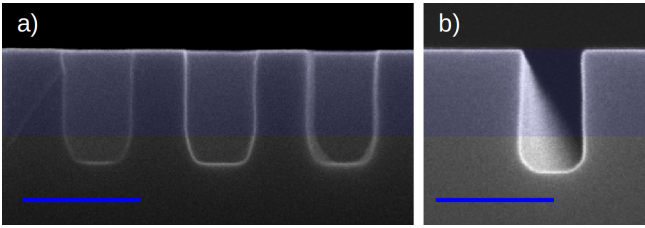


Figure 4. Etch of a) photonic crystal holes of radius 75nm etched using the bulk etch recipe, b) a straight sleeve of 90nm etched using the sleeve etch recipe. The blue shading indicates the thickness of the 145nm GaAs nanomembrane, and the scale bars each represent 200nm.

The final optimized process parameters for all etches were: 10sccm of Ar, 15sccm of BCl₃, chamber pressure of 6mTorr, ICP coil power of 500W, and bias power of 25W. The etch time for the sleeve etch was 2 minutes 40 seconds. The specific tool used was the "Plasma-Therm" model "Apex SLR." We optimized two different bulk etch conditions tailored to simultaneously remove the bulk and fabricate a photonic crystal elsewhere on the chip. We discuss the importance of this process flexibility below. The first bulk etch condition was optimized for a photonic crystal with band gap centered on 960nm, which has a lattice constant of 250nm and hole radii 0.3 times the lattice constant. This "960 bulk etch" has the same etch conditions as the sleeve etch, but an

etch time of 4 minutes 0 seconds. The second bulk etch was optimized for a photonic crystal with bandgap centered on 1550nm (500 nm lattice constant, hole radii 0.3 times the lattice constant). This "1550 bulk etch" uses the same etch conditions as the sleeve etch, including an etch time of 2 minutes 40 seconds. Both bulk etches tend to etch deeper into the undercut layer, but this layer is removed in a subsequent step. We found that we could not develop reliable mask dose and development conditions for etched sleeve widths of 65nm or lower. We found that etched sleeve widths of 120nm and larger showed an onset of a chamfer. Our final etched sleeve width, ~92nm, was chosen to be comfortably between these limits. We note that ~92nm is the width of the etched sleeve that results from an EBL write of width 62nm due to the ICP etch biasing discussed previously. Fig. 4 shows cross sectional images of the sidewall profiles obtained for a) photonic crystal holes of radius 75 nm (960nm design) using the 960 bulk etch and b) a 92nm sleeve using the sleeve etch.

Next, we demonstrate the importance of the sleeve and bulk etch method. In Fig. 5a we show the sidewall profile for one wall of a 10 μ m trench etched as a single feature using the optimized sleeve etch. The drastic difference in RIE lag for such a large feature results in significant sidewall angle and an unacceptably poor sidewall profile. This illustrates the impossibility of using a single optimized etch for both small and large features. In Fig. 5b we show a cross section of a 400nm radius feature after the edges have been defined by a sleeve etch. In Fig. 5c we show a cross section of a 400nm radius feature after both the sleeve and bulk etches have been completed. Note the sidewall profile within the blue highlighted region that indicates the thickness of the GaAs nanomembrane. The uneven etch

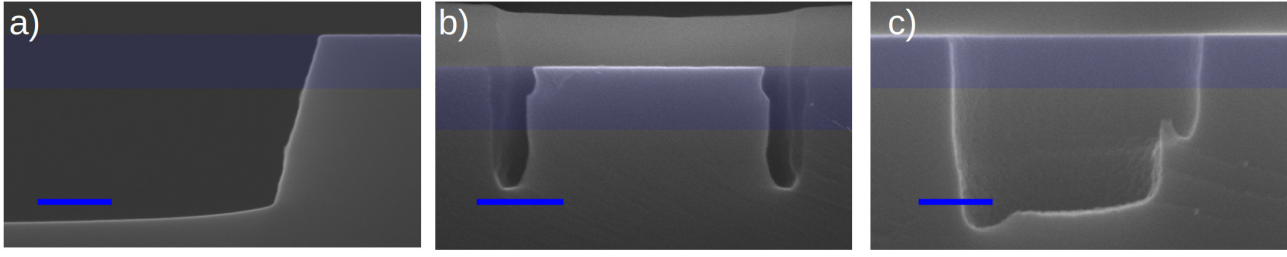


Figure 5. a) One side of a $10\mu\text{m}$ trench etched as a single feature using the sleeve etch recipe. b) a 400nm radius feature after the sleeve etch, c) a 400nm radius feature after both the sleeve and bulk etch. The blue shading indicates the thickness of the 145nm GaAs nanomembrane, and the scale bars each represent 200nm . The notching shown in b) is believed to be sonication damage and reduced sonication power has eliminated this defect. The 25nm alignment error in c) did not damage the device in the critical membrane layer, rather this error is in the undercut layer which is removed during the undercut.

depth apparent at the bottom of the feature is irrelevant because it is entirely within the AlGaAs undercut layer that will be removed in a subsequent step. Fig. 5c also illustrates the EBL alignment precision tolerance of the bulk and sleeve method: the asymmetry between the left and right sides of the bottom of the etched feature occurs because the bulk etch pattern was somewhat closer to the left edge of the object as defined by the sleeve etch, rather than being precisely centered. The feature within the nanomembrane is not affected by the limited alignment precision. We note that it is essential to etch the sleeve before the bulk, as discussed further in the supplemental material.

Finally, we assess the performance of the sleeve and bulk method when fabricating features that transition between the small and large regimes, i.e. features that transition from all-sleeve to sleeve-and-bulk. We take as our first test case a series of wedges with varying opening angles. The sharp point of all wedges is always defined and etched as all-sleeve and there is a transition to sleeve-then-bulk at a distance along the wedge that is determined by the opening angle. We observe no fabrication errors at the boundary between the all-sleeve

and sleeve-then-bulk regions of the pattern when fabricating wedges with an opening angle as small as 15 degrees. For wedges with an opening angle of 10 degrees or smaller we observe inconsistent results at the transition point. We believe this inconsistency originates from the reduced stability of the very narrow (high aspect ratio) resist that is supposed to protect the bulk in this region. This resist failure is somewhat a random issue and likely depends on sample handling; characteristic SEM images can be seen in the supplemental material. We take as our second, and more challenging, test case the inverse designed coupler whose design is shown in Fig. 1b.

In Fig. 6a we show the designed shape for such a device and the way in which the pattern is spliced into masks for sleeve (blue) and bulk (green) lithography and etch steps, note that the darker section of the mask file is the overlap between the sleeve and bulk layers. The yellow and green circles highlight two areas where the design contains features that transition between the all-sleeve and sleeve-and-bulk regimes. In Fig. 6b we show an example of such a device taken after the sleeve etch step. Fig. 6c shows an example of the same device after both the sleeve and

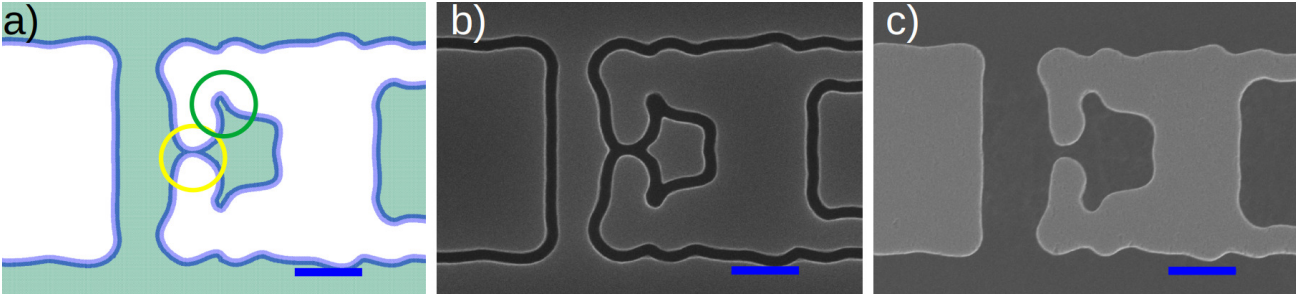


Figure 6. An inverse designed coupler a) GDS mask file showing the sleeve (blue) and bulk (green) layers, b) sleeve etch step, and c) final device after bulk etch step and HF undercut. Scale bars are 500nm.

bulk etches have been completed. The result demonstrates that there is no appreciable line-edge roughness in the transition regions and demonstrates the successful fabrication of inverse-designed device using the sleeve-and-bulk etch method.

3.3. Undercut wet etch

After defining the photonic elements via the sleeve and bulk ICP etches, the membrane was isolated from the substrate via a Hydrofluoric acid undercut etch. The required undercut etch can also be done using Hydrochloric acid. In either case, surface roughness due to the harsh wet etch conditions can be a concern, but we find this is usually mitigated by ensuring a sufficiently high crystal quality during MBE growth. To perform the undercut etch we first clean the sample with NMP at 80C. We then remove the undercut layer in the immediate vicinity of the photonic device with a partial etch in HF acid. The percent concentration of aluminum in the undercut layer strongly influences the etch rate in HF acid. We have found that too high of an Al concentration results in too rapid of an etch, and this violent etch process tends to damage the fragile membrane. Too low of an Al concentration results in an etch rate that becomes prohibitively slow. An

Al concentration in the range of 70-80% is accepted in literature[13] and we used 75%. After the undercut etch, a CO₂ critical point dryer was used in order to avoid membrane collapse due to surface tension of evaporating liquid. Others have found a gentle air dry from Methonol to be sufficient, but we used the critical point dryer for more reliable results.

3.4. Sample Cleaning

Resist removal and sample cleaning were important in the optimization of the etch parameters. In particular, for low SEM accelerating voltages the contrast between the resist residuals and the GaAs itself does not allow for accurate determination of feature size or sidewall profile. The top row of images in Fig. 7 shows samples that have not been cleaned; it is impossible to distinguish the resist residuals from the GaAs features. The bottom row of images in Fig. 7 show the same size features from the same sample after cleaning, which allows the clean pattern transfer and good sidewall profiles to be observed. To clean the samples we first removed the resist with a soak in NMP at 80C for a minimum of 2 hours with sonication for at least 15 minutes at the end of the soak. We found that it is extremely important to be consistent in the application of sonication.

When sonication powers or frequencies were too high we observed inconsistent destruction of samples that in some cases could be confused for rough chamfering due to destruction of resist during longer etches.

For removing hard carbon residuals we use a digital etch as recommended by [13], which includes 60s in 30% H_2O_2 , a 60s rinse in DI water, 60s in 22.5% KOH, and a second rinse in DI water for 60s. This digital etch is not necessary between the two ICP etch steps because the hard carbon residuals are largely localized to the etch features and the sidewall will be protected by the resist mask during the second ICP etch. Release and re-deposition of these hard carbon residuals on the sample surface can be avoided by using the sonication discussed above. We prefer to use only one digital etch cleaning at the end of all the etching steps and the HF undercut etch because it can damage the GaAs membrane either directly or through excessive oxidation enhancing damage during the HF undercut etch.

4. Photonic Device Performance

We test the efficacy of our method by comparing the optical performance of both inverse designed (Fig. 1b) and traditional grating (Fig. 1a) out-couplers fabricated with the sleeve and bulk method to those fabricated with a traditional single-step etch. In each case we fabricated and then measured the transmission through a coupler - waveguide - coupler device as a function of laser wavelength. By normalizing the transmission against the known reflectance of a silver mirror (Thorlabs P01), we extracted the spectral dependence of the in- and out-coupling efficiency of each coupler design and fabrication method. The results are presented

in Fig. 8. The blue and orange data show the measured performance of couplers fabricated with a single etch, using either the 960 or 1550 optimized bulk etch conditions. The green data reports the performance of the couplers fabricated using the sleeve and bulk etch. The data shows that the sleeve and bulk method results in a factor of 2 improvement in in- and out-coupling efficiency. In the case of the inverse designed coupler (Fig. 8a), the improved performance could be attributed to both improved sidewall profiles and improved pattern transfer fidelity in areas of rapidly changing feature size (e.g. circled areas in Fig. 6a). In the case of the traditional diffraction coupler, the feature sizes and separations are quite regular, which suggests that improved sidewall profile is the primary reason for better measured performance using the sleeve and bulk fabrication method.

5. Process Flexibility, Limits, and Advantages

The optimized sleeve and bulk etch method has several advantages in terms of process flexibility. First, the consistent local feature size (width) of the sleeve mask provides improved sidewall profile independent of overall (bulk) feature size or local curvature. Second, the sleeve and bulk method is tolerant to alignment errors as large as 45nm between the EBL masks for the two ICP etch steps. Third, the precise etch conditions for removal of the bulk are not critical: the sidewalls are protected by resist and the precise etch depth into the Al-GaAs undercut layer is not important so long as the etch is deeper than the membrane thickness. This allows the second (bulk) etch step to be optimized for simultaneous fabrication of important photonic feature elsewhere in a device. For example, photonic crystals and cavi-

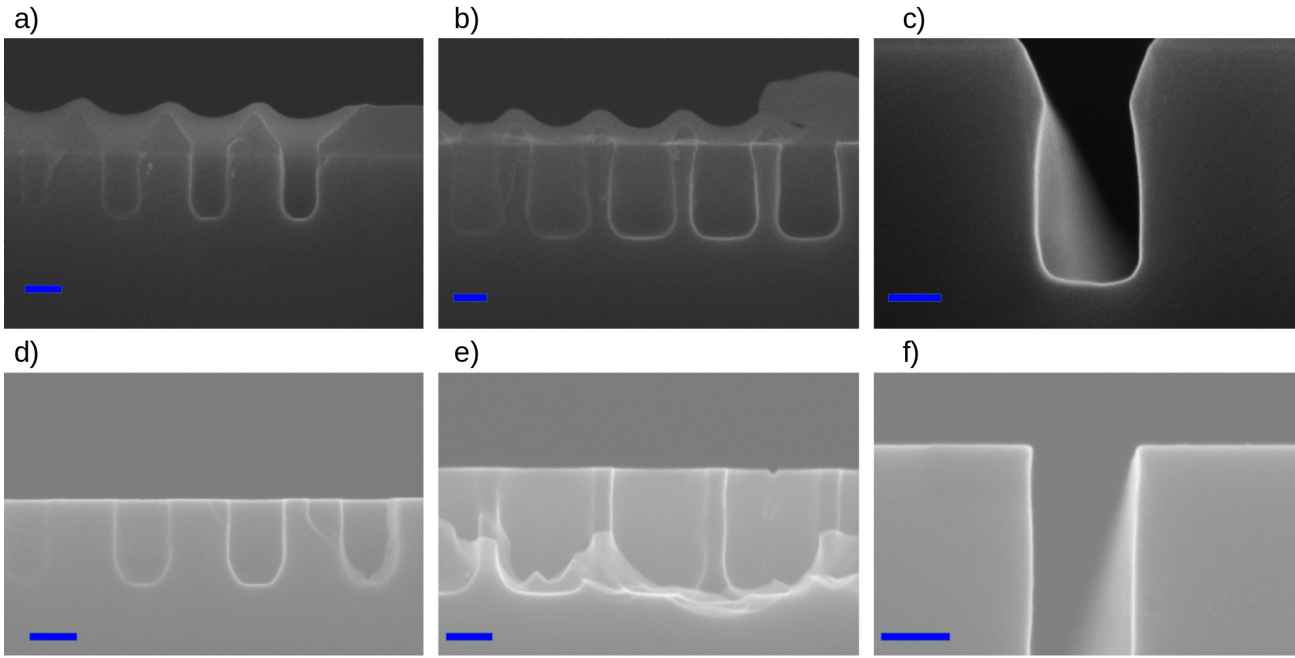


Figure 7. The same sample before (top) and after (bottom) resist removal. Left images (a, d) show undersized photonic crystal holes, center images (b, e) show large photonic crystal holes, and right images (c, f) show trenches 160nm wide (twice the sleeve width). The removal of the residuals by the cleaning process is critical for accurate assessment of etch quality. All scale bars are 100nm. Notice the sonication damage in the large photonic crystal holes (panel e).

ties are known to be very sensitive to the precision with which the hole radii and sidewalls are fabricated. To highlight this process flexibility, we optimized two bulk etches to simultaneously fabricate photonic crystals centered on wavelengths of 960nm or 1550nm and find that both of these bulk etch conditions work equally well for removing the bulk from sleeve-defined features.

The most significant limitation of the sleeve and bulk etch method we report here is for the fabrication of “intermediate size” features somewhat larger than twice the sleeve width. See the supplemental material for a detailed description of our analysis of the intermediate size regime. We find that features as large as 160nm can be reliably fabricated with the all-sleeve approach. For features larger than 310 nm, we find that the sleeve and bulk method works reliably. The dominant

failure mode for intermediate size features (between 160 and 310nm) is collapse of the thin strip of resist left between the two sleeves, which is intended to protect a very small bulk area. We note that these are not hard boundaries, but rather approximate measures of the bounds on feature sizes for which results are less reliable. We emphasize that the limitations we observe for the fabrication of intermediate size features apply only to features dominated by the particular feature size, such as trenches or circular holes. Importantly, the results shown in Fig. 6 demonstrate that the sleeve and bulk method can effectively fabricate structures even when they include intermediate size features in the transition from smaller to larger features. Specifically, Fig. 6a highlights locations in the pattern where there is a seamless transition from two sleeves to a single sleeve transition

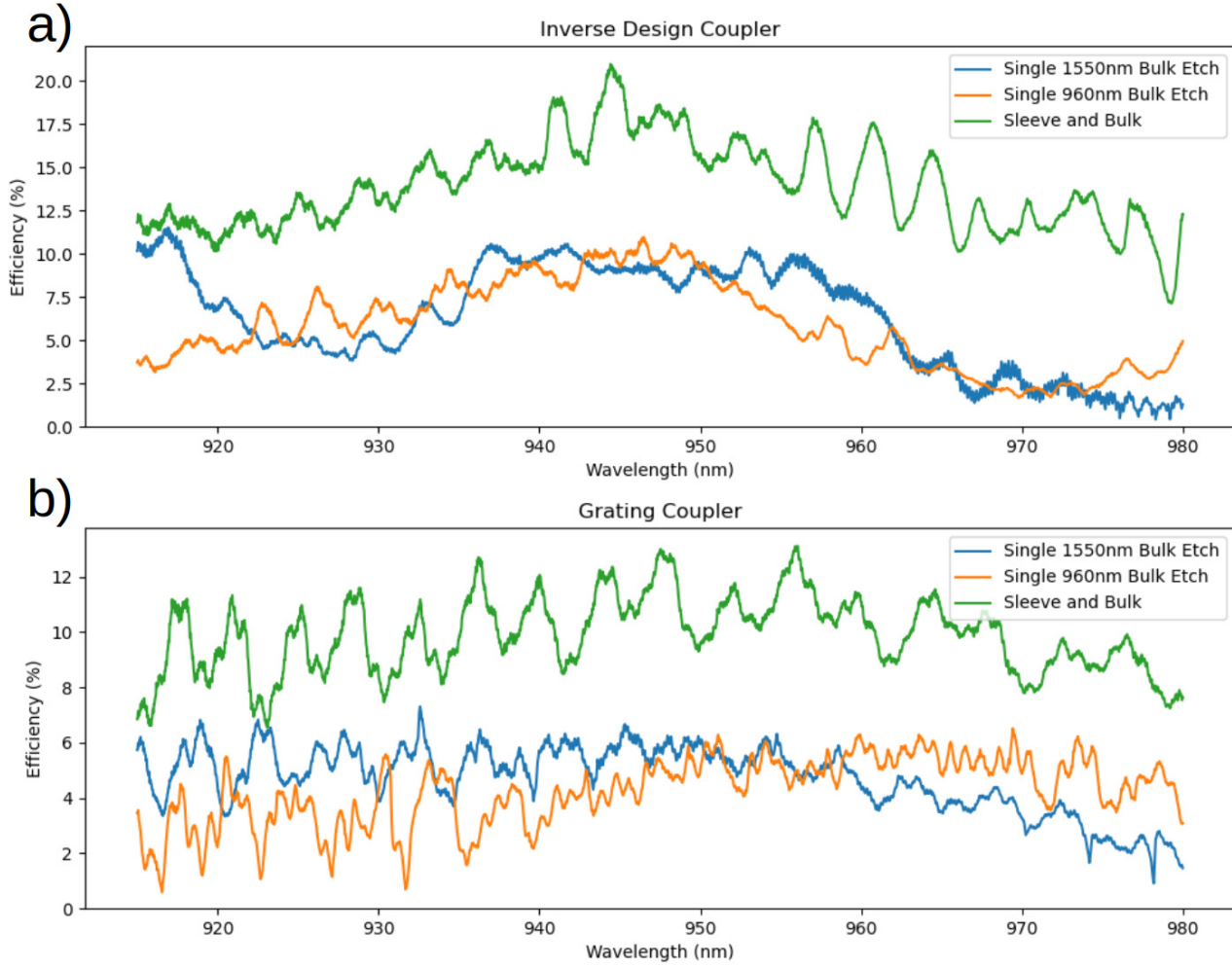


Figure 8. Transmission Data of a) inverse designed couplers and b) standard grating couplers. (green) devices fabricated using the sleeve and bulk etch and (blue) and (orange) devices fabricated in a single “all-bulk” etch using the 1550nm bulk etch and 960nm bulk etch recipes respectively. For both types of devices, inverse designed coupler or grating coupler, the sleeve and bulk technique (which does not specifically target either device type) shows an almost doubling of coupler transmission efficiency.

(yellow circle) and around a tight corner (green circle).

Perhaps the most important advantage of the sleeve and bulk method is that it can immediately be applied to new photonic element designs. For example, it is possible that the single-step etch conditions for either inverse-designed or diffraction couplers could be optimized to obtain coupling efficiencies comparable to what we obtained using the sleeve and bulk method (see Fig. 8). However, such etch optimization would be specific to the

exact size and shape of the target photonic element. Moreover, in the case of inverse designed elements that can contain a wide range of length scales and curvatures, such process optimization would likely require a large number of iterations to develop a mask file that compensates for the varying RIE lag at different points in the pattern in order to realize a structure, after etch, that has the target shape. In contrast, the sleeve and bulk method is largely insensitive to such details because the sleeve etch realizes good sidewall

profiles for near-arbitrary shapes. The data reported in Fig. 8 support this conclusion: the sleeve and bulk method outperforms single-step etches for two very different photonic elements (inverse design vs diffraction) without any additional optimization. We believe this process could also be adapted to improve inverse designed silicon photonic devices; for such an adaptation we recommend optimizing the bulk etch for maximum selectivity in order to stop the etch at the supporting layer, thereby avoiding over-etching into this layer when there is imperfect spatial overlap between the sleeve and bulk etches. [11; 12]

6. Conclusion

The traditional approach of using multiple etch processes optimized for different feature sizes in photonic devices can be highly effective, but it cannot be efficiently applied when devices contain features on many different length scales. This problem is expected to become increasingly important as methods such as inverse design are increasingly employed to design devices with improved performance deriving from increased complexity. We have developed a sleeve and bulk method that provides good pattern transfer fidelity and side wall profiles for almost all feature sizes using two, and only two, etch steps. We describe our development of this process, demonstrate that it can be used to fabricate devices with complex features that transition between size regimes, and quantify the performance limits. The optimized recipe we report thus provides a process that can be employed to fabricate increasingly complex photonic devices with features on multiple length scales.

7. Acknowledgements

This research was primarily supported by NSF through ENG-1839056. This research was partially supported by NSF through the University of Delaware Materials Research Science and Engineering Center, DMR-2011824.

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