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Epitaxial Bonding and Transfer Processes for Large-Scale Heterogeneously Integrated Electronic-Photonic Circuitry

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A process flow for the heterogeneous integration of III-V epitaxial material onto a silicon host wafer using CMOS-compatible materials and methods toward the goal of forming electronic-photonic circuitry is presented. Epitaxial structures for compound-semiconductor-based transistors are assembled on a silicon carrier wafer using a commercially-available polymer and then formed into distinct patterns for scalable processing. A CMOS-compatible metallization process is performed on the back side collector terminal of the aligned epitaxial structures, followed by a metal-eutectic bonding process that transfers the wafer-scale array of III-V material onto a separate silicon host wafer allowing the fabrication of both electronic and photonic devices on a single wafer. Characterization of the epitaxial bonding and transfer is performed to ensure material alignment is maintained without additional tooling and that the interconnect layer established between III-V collector and silicon host wafer performs as an ohmic contact, thermal path, and mechanical bond compatible with back-end-of-line (BEOL) integrated circuit processing. These processes are shown for GaAs-based light-emitting transistor (LET) epitaxial material to demonstrate that subsequent photonic devices and systems may be patterned into the integrated material allowing a direct electrical interconnect to embedded CMOS-based electronic systems for new functionalities as electronic-photonic integrated circuitry.

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The rapid maturation in photonic device designs has enabled large-scale optical communication systems that efficiently interlink electronic networks. This infrastructure has enabled broad access to electronic systems through establishing high-speed, low-power optical methods for signal transmission.[1,2] Advances in material designs, patterned component isolation, and improved packaging technology have led to high-performance photonic device designs,[3–5] thereby extending high speed performance, improving device thermal profiles, and allowing for electronic drive controls of optical links.[6–8] These discrete photonic devices route between electronic networks, but recent goals now look to establish fabrication methods for chip-scale photonic systems that interact closely with CMOS-based electronic integrated circuits (IC) either as on-chip optical links or as photonic processors.[9] Heterogeneous integration has also been viewed as critical for bringing active devices such as lasers into silicon photonic systems and for the enhancement of silicon in general with other materials for electronic and photonic functions. This desire stems from the scalability in established CMOS processing, where the process can be separated into separate front-end-of-line (FEOL) and back-end-of-line (BEOL) processes that allow for dense interconnection, self-aligning gate processes, and 3D vias that each have analogs to the electrical needs of photonics.[10–12] An integrated approach to photonics allows for better device thermal control and signal coherence,[13,14] but also establishes a method for forming a direct on-wafer connection allowing for the possibility of photonic and electronic devices that can interact across signal domains. The close pairing of electronic and photonic systems is then best enabled by establishing unified electronic-photonic integrated circuitry.[15]

In contrast to past proposals for all-optical circuitry,[16] new efforts in three-terminal photonic devices enable this progress toward electronic-photonic integrated circuitry that can be implemented in a wafer-scale manner.[17] The designs for light-emitting transistors (LET) and transistor lasers (TL) stem from heterojunction bipolar transistor (HBT) structures,[18] thereby allowing for three-terminal compound semiconductor transistor structures with photonic functionality to interconnect with and between FEOL-processed silicon CMOS, as shown in Figure 1. The goal depicted in this figure is the definition of precisely located III-V epitaxial material islands that may serve different electronic or photonic functions on a silicon host wafer in a wafer-scale process. Through the use of a carrier wafer and distinct III-V epitaxial wafers, material can be placed with coarse precision, thinned, patterned and dry etched to create precisely located islands, and bonded to a silicon host wafer prior to entering back end of line processing such that III-V material now is present on the silicon host wafer in locations required to effect a specific system function. When used to form interconnects, this can serve to network electronics and photonics directly as a three-dimensional chip stack, densifying the patterning of optical transceivers alongside their electrical controls. The fabrication of such a system requires new processes to establish a strong contact between electronic and photonic devices, as well as an investigation of contact metallization suitable for CMOS. Characterization related to these interconnects and of CMOS-compatible wafer-scale bonding is the fundamental step forward in achieving heterogeneous integration of III-V on Si.

Various methods for heterogeneously integrating III-V materials onto silicon have been pursued with aims of defining a scalable means for production. The recent goals of silicon photonics have enabled success in transfer of III-V materials onto SOI substrates[19,20] yet the bond itself resides over an insulating polymeric material (i.e. BCB) and requires sacrificial epitaxial layers to create devices, limiting performance. The costs and tradeoffs of device-level alignment before bonding, as with flip-chip bonding before it,[21] also strain the scalability of the technique. Additional work in bonding photonic materials employs low temperature hydrophilic bonding between oxidized materials,[22,23] yet this can impair the performance of photonic devices due to lattice mismatch of materials and constrains the flatness of both materials to ensure good contact. The presence of bond voids in such oxide-based bonding techniques also has the potential to limit the interplay between photonic and electronic device layers and accrue losses. Older epitaxial liftoff (ELO) methods for integration showed promise, but the strain induced on resulting devices by the use of black wax and harsh HF-based etching on AlGaAs compounds limited its commercial viability and constrained the choice of material system due to the need for a liftoff layer.[24] Other recent methods use adhesive bonding and dielectric coatings in achieving integration of III-V materials on silicon,[25,26] yet the thermal reliability of devices atop these interfaces remains an open question. The functioning of an integrated

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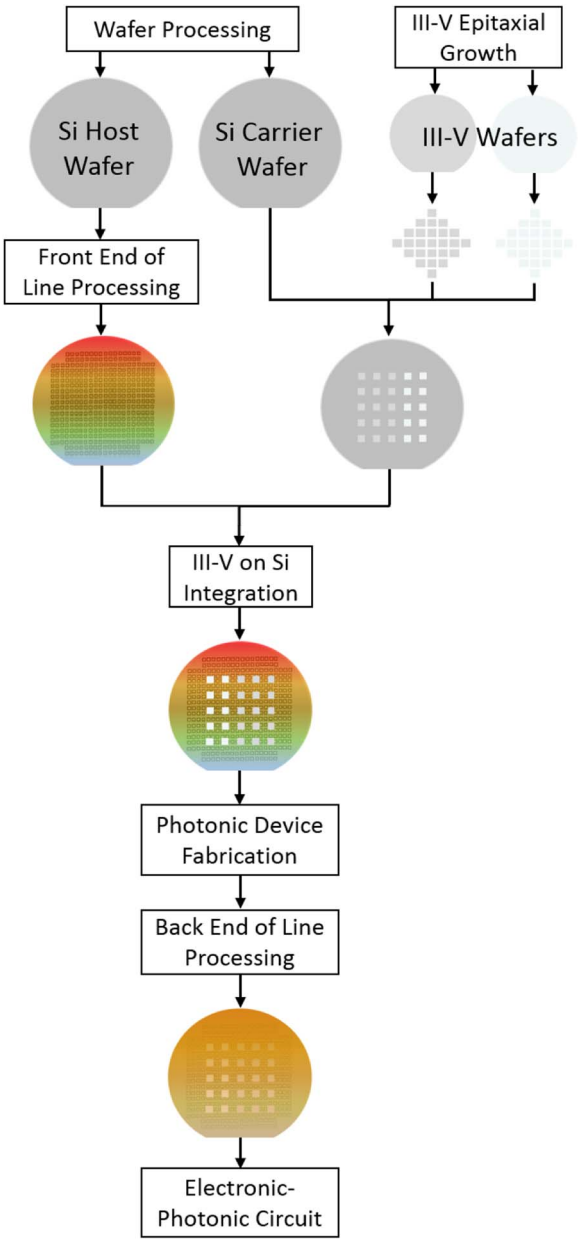

Figure 1. Schematic of the full CMOS-compatible process for developing heterogeneously integrated electronic-photonic circuits.

photonic system with suitable performance rests on the capability for reliable thermal and electrical management of its devices,[15] so the need to establish a bonding process that addresses these is imperative for scaling novel integrated circuitry. A bonding technique that can pattern a metal interface in a CMOS-compatible manner for integrating the photonic devices is ideal.

This paper describes the methods and fabrication techniques that allow for wide-area selective and patterned distribution of III-V materials onto a silicon host, such that a bond may be formed that addresses drawbacks faced by other methods and acts as an interconnect between three-terminal photonic devices and underlying CMOS structures. An epitaxial bonding and epitaxial transfer process is presented for the definition of InGaP-InGaAs-GaAs three-terminal material directly onto silicon, followed by characterization and optimization of the bond to assess the resulting material for photonic device suitability. The processing methods for establishing a eutectic alloy for the bond interface between III-V and silicon host are discussed and analyzed. This single bond works as the mechanical hold, thermal path, and ohmic electrical contact by which the embedded collector terminal of LET and TL devices interface with CMOS, eliminating the isolation of photonic devices above an insulating layer that degrades thermal performance. This approach allows for the stacking of separate materials three-dimensionally such that an intimate mesh of electronics and photonics may be fabricated and characterized. In this manner, an array of III-V materials may be transferred to silicon followed by wide-area fine alignment of devices after transfer, enabling the transition from discretely placed photonic devices to large-scale electronic-photonic integrated circuitry designs. The methods presented show the fabrication and metallization techniques for III-V on Si such that a network of three-terminal photonic devices can be patterned post-transfer and the electrically interconnected materials can form the groundwork for a photonic logic circuit.

Experimental

Epitaxial bonding.—The integration of III-V material onto a silicon host begins by establishing an epitaxial bonding process. In this, III-V epitaxial wafers can be prepared on a separate silicon carrier wafer and converted into an array of fine-aligned III-V materials, ready for integration with a separate CMOS-based electronic device layer. The epitaxial bonding process is shown in Figure 2. Smaller 50 mm (2”) silicon wafers are utilized here due to tooling constraints, but the process is shown to be fundamentally scalable.

A temporary bonding polymer is first used to establish a bond between III-V bulk material and the carrier wafer (Figure 2a). The temporary bonding polymer (*AI Technology*) consists of a blend of copolymers that together act similarly to a polyimide, allowing for the polymer to create a high integrity bond between wafers that is soluble and dry-etchable in an ashless manner such that it allows for temporary adhesion.[27] Thermal tests have been performed to characterize the bonding polymer, assuring that the polymer will not outgas in an N_2-purged chamber up to 450°C and as a consequence will be removable following subsequent bonding and anneal steps. The polymer is commercially-available and is in current use for handling in back side wafer processing (3D-TSV) and for other backend wafer-level processing (WLP), as well as it spins on in a void-free planar manner and is durable across a wide thermal range once it is cured. This is in line with past analyses on how to verify compatibility of temporary bonding polymers for CMOS.[28] Here, this polymer’s use is extended to the handling of III-V material atop a carrier wafer. In the first step of the process, the bonding polymer is spun onto the carrier wafer at a thickness of roughly 2–4 μm and a set of diced III-V epitaxial wafers are assembled epi-side down directly on the polymer in a manner similar to high-speed (low accuracy) “pick-and-place” tooling. Crystalline axes of the cleaved wafer pieces can be oriented and maintained by this tooling as well, ensuring that no misalignment occurs between pieces that may affect later etching or coupling of photonic devices.

Following the initial contact, a purged vacuum anneal is performed at 250°C for 2 hours, applying a constant force of 5 N to the III-V bulk substrate pieces to ensure good planarization of the temporary bond during its vacuum lamination. The remaining polymer exposed between each of the bulk III-V wafer pieces is then removed in a high-power ICP-RIE O_2 plasma (100 sccm O_2, 10 mT, 200 W RIE, 600 W ICP), as shown in Figure 2b. The final assembly is shown in Figure 3, where the III-V epitaxial pieces are seen in distribution after curing (Figure 3a) and again after the excess polymer is removed by plasma etching (Figure 3b). Critical is the fact that the III-V epitaxial layers are face-down into the bonding polymer, as shown in the scanning electron microscope (SEM) micrograph in Figure 3c, leaving the collector terminal most upward facing underneath the bulk substrate.

The assembly of the III-V wafers on the silicon carrier wafer is then prepared for removal of the GaAs-based bulk substrate on which the epitaxial layers were grown. A combination of diamond-based lapping and chemo-mechanical polishing (CMP) removes the bulk substrate of the III-V wafers (Figure 2c). The bonding polymer

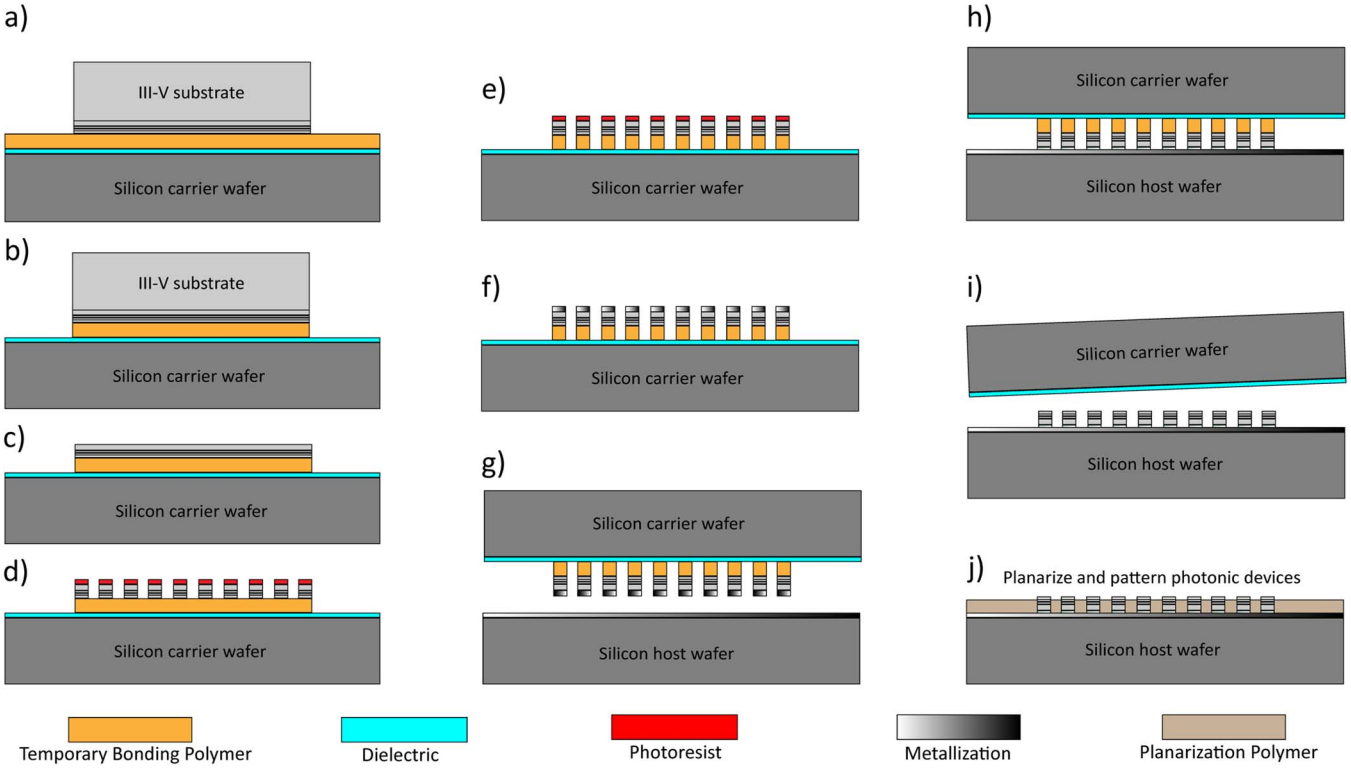

Figure 2. Process flow of epitaxial bonding and epitaxial transfer processes. The bonding proceeds by: a) placing the III-V epitaxial wafers onto the bonding polymer, b) removing excess bonding polymer, **c)** performing substrate thinning on the III-V wafers, d) photolithographically defining and etching III-V islands in an array, e) removing excess bonding polymer between islands, and f) establishing an ohmic collector contact on the III-V islands. The transfer process then proceeds by: g) bringing the III-V islands in contact with a metallized host wafer, h) eutectically alloying the interface, i) removing the carrier wafer and bonding polymer, and finally j) planarizing the epitaxial material.

maintains mechanical stability of the III-V material atop the silicon during mechanical lapping and allows for scalable removal of the excess substrate. An additional wet-etch consisting of dilute ammonium hydroxide and hydrogen peroxide ($NH_4OH:H_20_2:H_20$, 4:1:8) at room temperature can also be used to remove the bulk GaAs material while maintaining its polished surface and maintaining the polymer underneath. The epitaxial structures are protected from the thinning processes throughout by means of being face-down toward the polymer. Additional findings show that the inclusion of a grown nitride dielectric on the carrier wafer beneath the bonding polymer helps alleviate stress in the polymer during substrate thinning and provides higher yield. This is notable as the yield from epitaxial bonding carries toward the final integration without further degradation. By this, substrate thinning stands as the largest factor in the overall process yield, as improvements in wet-etching chemistries and lapping techniques atop dielectric have shown pronounced increases in the area of suitable epitaxial layers, and it is expected that more automated industry-scale thinning processes can completely alleviate this factor. A wide-area distribution of III-V epitaxial material is thus formed on the carrier wafer, removed of its substrate yet held rigidly in place by the bonding polymer.

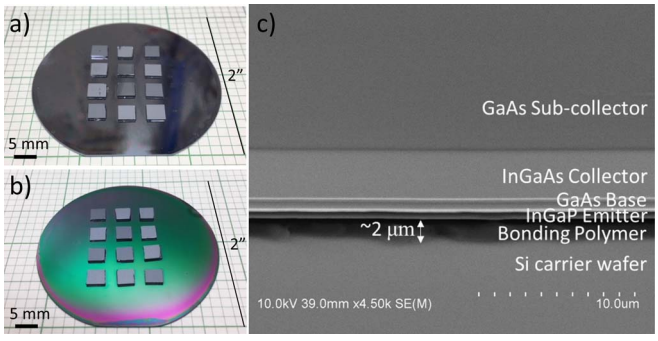

Figure 3. Wafer-scale placement of III-V epitaxial wafers on carrier wafer during epitaxial bonding**.** The silicon carrier wafer is shown with a) III-V wafers placed on top of the bonding polymer after curing, b) the same assembly after removal of excess polymer, and c) a close-up SEM micrograph of the temporary bonding polymer interface, where the composition of the epitaxial layers is shown (via selective A-B stain etch) face-down into the polymer and the n-type collector is upwards.

The temporarily bonded materials proceed through photolithography in order to define a geometric array of material (hereafter known as III-V islands). The III-V islands are patterned in a manner such that they take the thinned III-V wafer pieces and convert them into photolithographically-aligned blocks with high accuracy (Figure 2d). Each III-V island is defined so as to be suitable for photonic device formation, sized on the order of photonic devices (i.e. 10^2 μm's) and distributed as functional blocks capable of containing multiple interconnected photonic devices. A dry etch process using chlorine-based chemistry (7 sccm BCl_3, 20 sccm Cl_2, 5 mT, 100 W RIE, 800 W ICP) is calibrated so as to remove excess III-V material and establish isolated III-V islands, with the etch proceeding from the collector material and stopping at the bonding polymer. A secondary dry etch in a high-power O_2 plasma then removes the newly exposed bonding polymer between each III-V island (Figure 2e). Optical microscope photomicrographs of these etch processes are shown in Figure 4. The striations shown in the floor in Figure 4a are a result of the thermal stress in the bonding polymer during plasma etching, but the resulting III-V island grid in Figure 4b shows a wide-area arrangement of suitable material that maintains good adhesion to the carrier wafer. Noting the epitaxial layers are a modified HBT structure for light emission, the most upward-facing epitaxial layer after III-V island formation is the collector (n-GaAs) across the aligned grid of material.

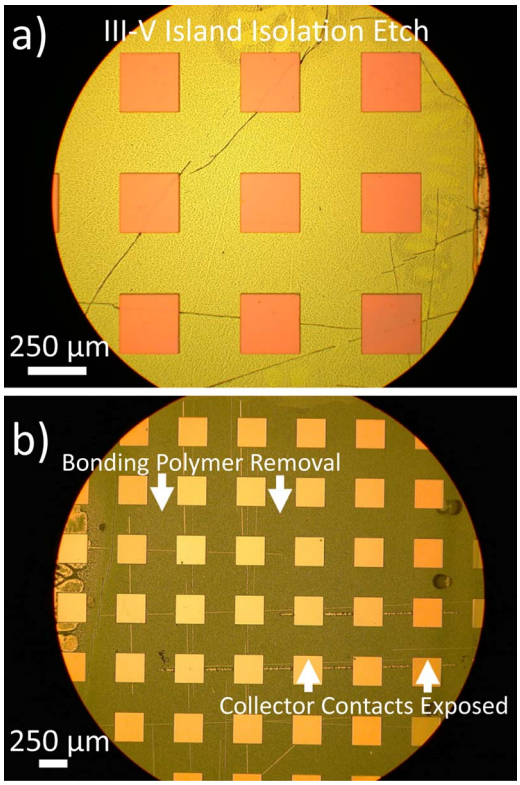

Figure 4. a) Photomicrograph of dry-etch isolation of epitaxial layers into aligned III-V islands atop bonding polymer, and the b) etch removal process of exposed bonding polymer and hard mask, opening collector contact at each III-V island.

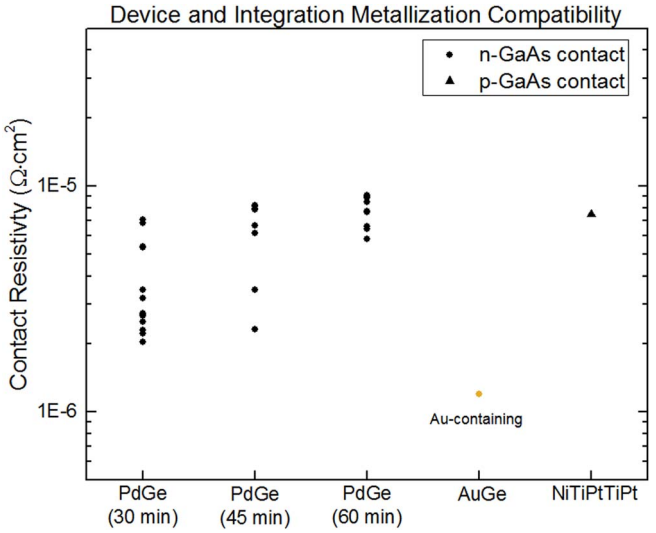

Figure 5. Characterization of the contact resistivity of GaAs-based device metallization. Both Au-free (CMOS-compatible) and traditional Au-containing contacts are examined.

This collector layer of each of the III-V islands is then utilized to establish a novel form of interconnect to enable integration. Common metallization strategies for GaAs-based photonic devices employ gold-bearing alloys, yet gold is not compatible with CMOS fabrication due to its status as a deep trap in silicon, so new contacts must be pursued. A non-gold contact is analyzed and formed by the use of a solid-phase regrowth process between palladium and germanium, where germanium migrates across the palladium during annealing and works to both alloy and degenerately dope the n-GaAs interface.[29,30] An optimal stack of Pd (500 Å)/Ge (1265 Å) is grown by E-beam evaporation onto each of the III-V islands for the n-GaAs collector contact, enabling a PdGe alloy that performs as an ohmic contact with remaining germanium atop each of the III-V islands (Figure 2f). An additional benefit of this technique is that the contact can be annealed below the thermal threshold of the bonding polymer. To ensure scalability in CMOS fabrication, the resulting PdGe contact is tested for contact resistivity and compared to standard AuGe alloys for n-GaAs contacts. The quality of this contact in terms of low resistivity is critical as it will function as the primary interconnect to underlying CMOS electronics. Transmission line measurements with 25 µm × 25 µm pads are performed to determine contact resistivity across a sweep of anneal times for the PdGe contact and compared to a separate contact metallization made using AuGe, as shown in Figure 5. The optimized metallization scheme based on PdGe is shown to reach comparable resistivities of $2.1 \cdot 10^{-6}$ Ω·cm^2 after 30 minutes of annealing at 320°C, rising in resistivity with additional time due to over-annealing, whereas the standard AuGe is measured at $1 \cdot 10^{-6}$ Ω·cm^2 with available tooling. It is expected that both metals would see further improvement in contact resistivity with further optimization and process control, with the notion that PdGe will continue to approach AuGe. In this, it is seen that a comparable n-collector contact can be formed that adheres to CMOS constraints, thus allowing for a photonic device contact that may interface with silicon directly.

Additional low-resistivity metallization methods compatible with p-type GaAs and CMOS are also found in prior literature and tested for contact resistivity for base contacts of the photonic devices,[31] eliminating any use of gold by establishing an E-beam evaporation of Ni (50 Å)/Ti (50 Å)/Pt (50 Å)/Ti (300 Å)/Pt (1000 Å) annealed at 400°C. The epitaxial bonding process concludes with the establishment of collector terminals across the entire distribution of III-V islands now prepared for epitaxial transfer.

Epitaxial transfer.—The procedure continues into an epitaxial transfer process that permanently unites the III-V material to a separate silicon host wafer (50 mm). An array of III-V islands has been established on the carrier wafer with a CMOS-compatible collector terminal, so a metal-eutectic bond is designed to connect the distribution of III-V islands and a silicon host wafer. The host wafer is utilized to emulate a CMOS-based IC having gone through FEOL processing, where gated electronic devices have been laid out and the host wafer is ready for the distribution of III-V islands. A metallization strategy is chosen to uniformly E-beam evaporate onto the host wafer a stack of Ti (500 Å)/Al (1500 Å), producing a contact floor in a manner familiar to CMOS.[32] This could also be patterned such that the Ti/Al metal is only present where III-V islands are intended to be bonded. This metallization allows for further optimization of the III-V on Si system given titanium's role in silicide formation and its use in self-aligning processes.[33] Future work that might look to other metallizations used in CMOS fabrication—such as variations on titanium-based gate contacts or using other refractory metals—is still compatible with the approach outlined here so long as the terminating surface on the host wafer remains an aluminum layer. This allows for this process to accommodate a range of FEOL metallization schemes and interconnects.

A metal-eutectic bond is then pursued between the two surfaces, as shown in Figure 6. As shown, the annealed collector contact on the III-V islands ends with a terminating germanium surface, while the host wafer separately presents an aluminum floor to patterned electronics, providing an ideal platform for wide-spread interconnects of III-V islands. The Al-Ge system exhibits a straightforward binary phase alloy that has only minimal mutual solid solubility,[34] allowing for a reliable regular-alloy to form that has seen success in silicon-based bonding processes.[35] The interface of Al-Ge contains an intrinsic eutectic point at 420 ± 4°C that is within the range of acceptable III-V processing temperatures, far below the melting point of aluminum (660.3°C) and germanium (938.3°C). By raising the

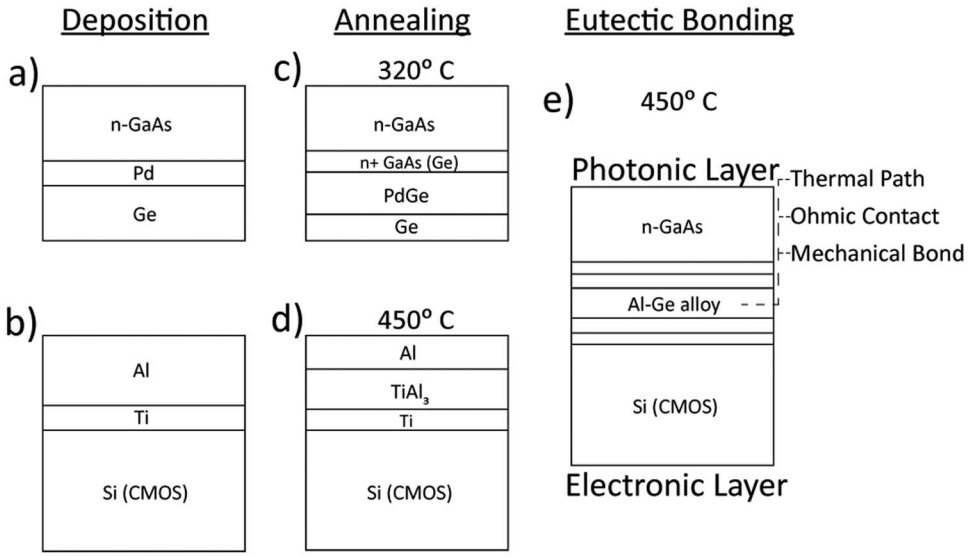

Figure 6. Interconnect formation between III-V and silicon material. a) The collector electrical contact is patterned on the n-GaAs while b) a separate ohmic layer is patterned on the carrier (CMOS) wafer. c) The collector contact is annealed and creates an ohmic contact to the III-V island terminating in germanium and similarly d) the carrier wafer contact is annealed and terminates in aluminum. Finally, e) a bond at the Al-Ge interface is formed by ramping the thermal profile to above the eutectic point.

temperature of the metal interface slowly above this eutectic point, a liquid metal alloy forms at the interface between germanium and aluminum that consumes roughly 28% germanium in weight compared to 72% of aluminum, followed by a slow reduction in temperature to below the eutectic point that produces a permanent alloy bond between the materials (Figure 6e). Past findings have confirmed that the compound formation of the alloy remains strong throughout the concentration range of constituent metals.[36] The excess germanium above the annealed ohmic collector contact of PdGe is then sufficient weight for the bond to proceed, while the host wafer metallization can also be annealed during the eutectic bonding process to ensure sufficient weight of aluminum.

In this, the carrier wafer and the host wafer are first prepared for the eutectic bonding procedure. A wet-etch strip of the germanium oxides on the III-V island arrangement is utilized, using dilute hydrochloric acid (HCl:H_20, 1:9), while a similar process is performed to strip the oxide layer from the aluminum-coated host wafer in very dilute phosphoric acid (H_3PO_4:H_20, 1:35), so as to minimize surface pitting of the aluminum. The assembly of the carrier wafer and host wafer are then loaded into a standard wafer bonding tool, where the carrier wafer is flipped over and contacted to the host wafer (Figure 2g). This allows for the III-V islands to be positioned directly between the carrier wafer and host wafer, establishing a direct interface between ohmic contacts of photonic and electronic materials. The chamber is purged and slowly ramped in temperature to 450°C, followed by a dwell time of 30 minutes to ensure full eutectic bond formation. The entire metal-eutectic bonding process is performed under a constant force to ensure uniform contact, chosen at 750 N after a test sweep across force measurements. After the eutectic bond is formed, a slow ramp down in temperature is maintained to avoid metallic brittleness and undesirable microstructures caused by rapid cooling of Al-Ge alloys.[37] The bonding polymer remaining beneath the III-V islands holds in place throughout the metal-eutectic bonding process, even as the wafer is flipped over and the temperature is raised, allowing for scalable bonding of III-V in unison (Figure 2h).

After bonding, a stack of material is formed that sandwiches III-V epitaxial material between a carrier and a host wafer, held in place by temporary bonding polymer and a permanent metal-eutectic alloy, respectively. The stack of material is then submerged in a solvent stripping bath, which works to dissolve the remaining bonding polymer and allow for the liftoff of the entire silicon carrier wafer (Figure 2i) while not affecting the metal-eutectic bond. The bonding polymer comes off readily in the solvent bath, requiring only minimal heating and agitation to release the entire carrier wafer. Once the carrier wafer is clearly removed, the host wafer is inspected for the permanent bonding of III-V epitaxial material in an array. This is shown in the SEM micrograph in Figure 7, where a clear distribution of integrated III-V epitaxial material is found that maintains its fine alignment and is now electrically interconnected to a host by its collector terminal. Small amounts of the bonding polymer may remain on the integrated III-V on Si after bonding, but this is removed by conducting a final high-power ICP-RIE O_2 plasma etch to eliminate any residual organics from the surface of the host wafer in a CMOS-compatible manner. A pattern of III-V epitaxial material is now permanently integrated onto silicon, with the emitter contact now facing upward and an interconnect layer below that unites collector contact to the silicon host. This arrangement has the advantage of

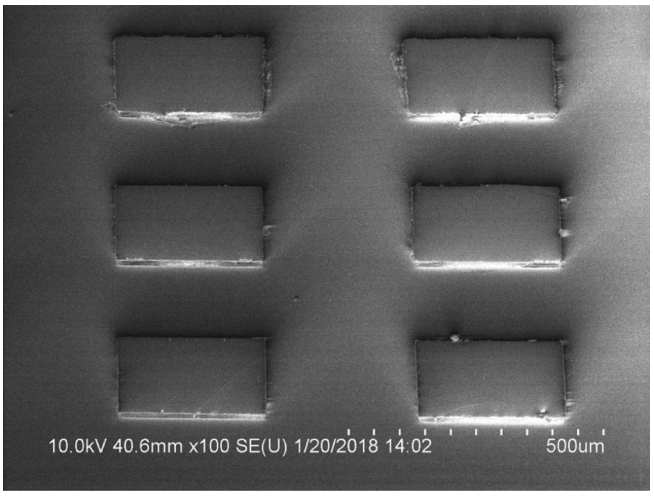

Figure 7. Scanning electron micrograph of integrated epitaxial material on silicon after epitaxial transfer. The background is the aluminum-coated silicon host wafer while the aligned features are the III-V islands with emitter side upward.

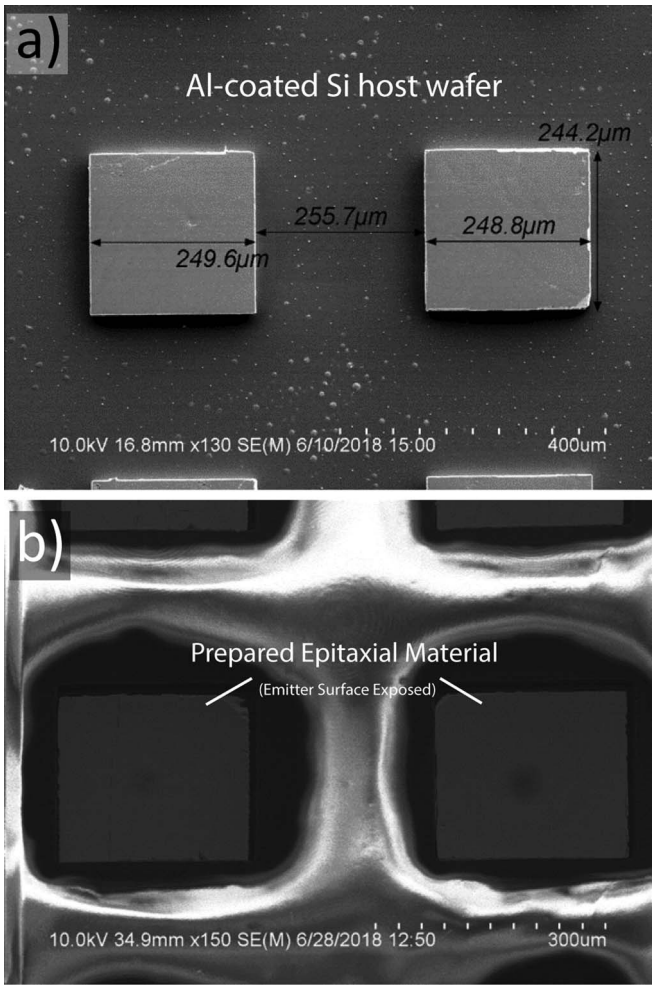

Figure 8. Scanning electron micrographs of the integrated epitaxial material prepared for further device fabrication. a) The III-V islands are shown after the transfer process and cleaning processes with emitter surface upward. Fine alignment of III-V islands is shown to be maintained throughout the bonding and transfer processes. b) Polymeric planarization is shown to further isolate each III-V island and establish a uniform surface for further device processing.

allowing for thermal and electrical flow to pass vertically through the material and into the silicon substrate while any light emission from the quantum wells (QW) in the base travels parallel to the host wafer, distinguishing optical and electrical reference planes uniquely.

Results

Device preparation.—The epitaxial layers are shown after O_2 cleaning in Figure 8. The emitter face is upward in the SEM image (Figure 8a) and what is clear is that the III-V islands stay in good form throughout the bonding process, with no signs of breakage or misaligned material that might disaffect the eventual layout of integrated photonic devices. The dimensions of the final bonded III-V islands also show strong consistency to the intended feature sizes, implying a good anisotropic dry-etch is attainable with the III-V islands suspended above bonding polymer. The background is the aluminum-coated host wafer which can be patterned to either isolate or connect collector terminals of photonic devices. The integrated materials are then planarized in compliance with other CMOS and microelectronic designs. This serves to both block the Al-Ge alloy from TMAH-based developers that might etch aluminum and damage the eutectic bond, but also to establish a uniform interface above the photonic devices where further BEOL processing and layer deposition for electrical interconnects might take place. The III-V islands are planarized by the use of a standard benzocyclobutene (BCB) insulating polymer (Figure 2j), which is spun onto the devices, cured, and later etched back with standard Freon-based dry etch chemistry (15 sccm SF_6, 25 sccm O_2, 35 mT, 110 W RIE).[38] This is shown in Figure 8b, where the epitaxial materials are opened and shown as ready for device process development and fabrication, while an additional opening may be etched out of the planarization polymer to probe the collector contact of a particular III-V island during testing. The compatibility of BCB for microelectronics and CMOS applications is confirmed by noting that the material acts as a low-K dielectric that is curable at low temperatures and thus has been used in very-large scale integration (VLSI) and multi-chip module (MCM) designs previously.[39,40] Additional processing of the integrated system of CMOS-based electronic devices and photonic devices can then proceed by stacking interconnect layers above the planarized surface as per usual methods, leaving open the possibility of connecting the emitter and base electrical contacts to further interconnect channels and also creating a plane for optical interconnects.

Bond characterization.—Following the transfer of material, characterization of the bond is undertaken to ensure that the final heterogeneous integration of materials is suitable for photonic device processing. The benefits of the preceding are that a bond is formed that serves to mechanically secure III-V islands, so as not to crack or delaminate in subsequent electronic packaging, while also creating a unified metal contact that is free of voids so as to thermally manage the epitaxial structures above the silicon substrate.

The integrated material is tested for the mechanical strength of the eutectic alloy interface by means of a shear force measurement. A test setup is constructed that consists of a shear-force transducer arm suspended above a translation stage, where the applied force may be measured and correlated with the corresponding displacement length to derive the maximum stress applied at the material before a rupture forms in the material. Using bulk III-V substrate to ensure a good shear test at the interface, the metallization scheme in Figure 6 is repeated on both the III-V material and a host wafer, followed by the same eutectic alloying method confirmed before. The total eutectically-bonded area to be sheared is then a summation of III-V islands across the sample totaling approximately 20.25 mm^2 in area, providing a fill-factor of ~20% of the total bulk wafer piece so as to mitigate any issues present when shear testing large-area bonds. The bonded material is assembled and secured above the translation stage while a steady translation of the material presses measure the shear force applied at the transducer. The results of the measurement for both a failed and a successful eutectic bond are shown in Figure 9. The failed bond ruptured at roughly 10 $N \cdot cm^{-2}$, cracking and sliding the substrate off the host, and the inset image of the bond layout shows that this is due to non-uniform bonding where voids are noticeable. The successful bond then is found to maintain its secure bond until the GaAs substrate itself finally ruptures at around 40 $N \cdot cm^{-2}$ of stress for the full sample. Upon inspection of the shattered GaAs of the successful bond, the distribution of eutectic alloy bonds themselves remained in place after the maximum shear force, implying that the eutectic alloy can withstand forces on the order of what can be expected for GaAs in fabrication and usage.[41] The inset image of the successful bond reinforces this, where no voids are seen on the surface of the alloys. The total stress calculated to just the area of eutectic bond islands is at 1.97 MPa, which is comparable to past research showing the strength and quality of the Al-Ge alloy in silicon bonding.[42] This conclusion rests well with the indication that the eutectic alloy has the capability of maintaining mechanical integration at capacities that can be expected of an interconnect in CMOS fabrication. It is also expected that the transferred material is robust to other forms of packaging stresses, such as wire bonding, owing to the fact that past work on flip-chip bonded chips via solder balls withstood wire-bonding,[43,44] and it is expected that the uniform metal interconnect in this work would match or exceed solder balls in terms of relieving process stress and heat.

Following mechanical tests, the bond interface is examined by cross-sectional analysis. A planarized integration of epitaxial

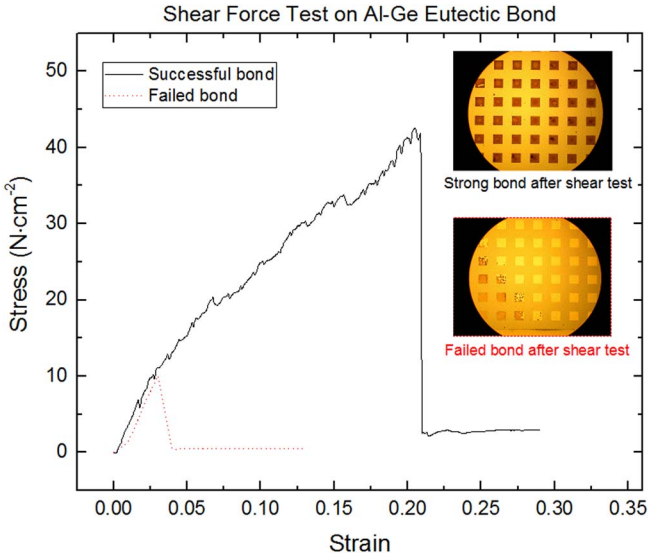

Figure 9. Characterization of the shear force strength of the bond layer integrating the III-V epitaxial material on silicon.

material on Si is assembled by the preceding processes and a focused-ion beam (FIB) mill is performed on the surface to inspect the underlying layers and the bond, in particular. The interface at the end of one III-V island is chosen and a wide-area ion-mill (gallium ion-based) is used to etch deep into the host substrate. The results of this are shown in a series of FIB-SEM micrographs in Figure 10. In these, it is clearly seen that the bonding and transfer processes have reduced the III-V substrate to just its epitaxial layers and, by transfer, reestablished the HBT-based structure with its emitter contact upward for three-terminal photonic devices. The edge of the planarization polymer is also etched through, contributing some minor resputtering. The eutectic bond appears across the entire interface of the III-V island, assuring that good contact is formed between the underlying substrate and preventing localized heating or thermal gradients across the integrated structure (Figure 10a). The bond is void-less, confirming strong mechanical strength as per the optimized shear strength testing, while the close-up micrograph of the eutectic bond interface distinguishes the two metal stacks and shows them both to have maintained good uniformity throughout processing and transfer (Figure 10b). The interface of Pd/Ge and Ti/Al shows good adhesion to both the III-V island as its collector contact and also to the underlying host wafer, assuring that there is no degradation of electrical or thermal performance of any resulting devices.

Additional inspection of the bond is performed to assess the bond interface for thermal and electrical conduction. An infrared (IR) test is used to penetrate past the surface of the integrated material and see the uniformity of the embedded contact between electronic and photonic materials after transfer. A tungsten-filament halogen lamp that has been filtered of visible and near-IR spectrum by use of double-polished GaAs is coupled into a microscope fiber and illuminated normally onto the surface of the integrated III-V material. The results of the infrared inspection of the bond collected in a silicon-based camera are shown in Figure 11, where integrated material is atop aluminum and is surrounded by planarizing BCB. The overall bond is shown to be highly uniform in two separate inspections, void-free with only minor variations in the eutectic formation that would not degrade the overall thermal or electrical path to a CMOS host wafer. This leads to the conclusion that a uniform bond can be formed that allows for proper thermal sinking of photonic devices formed into the integrated epitaxial structure. The high thermal conductivity of the bond interface between aluminum and germanium (Al-Ge, 1.26 $W \cdot cm^{-1}K^{-1}$[145]) placed between the III-V and silicon allows for good thermal characteristics of any resulting photonic devices, whereas integrated bonds

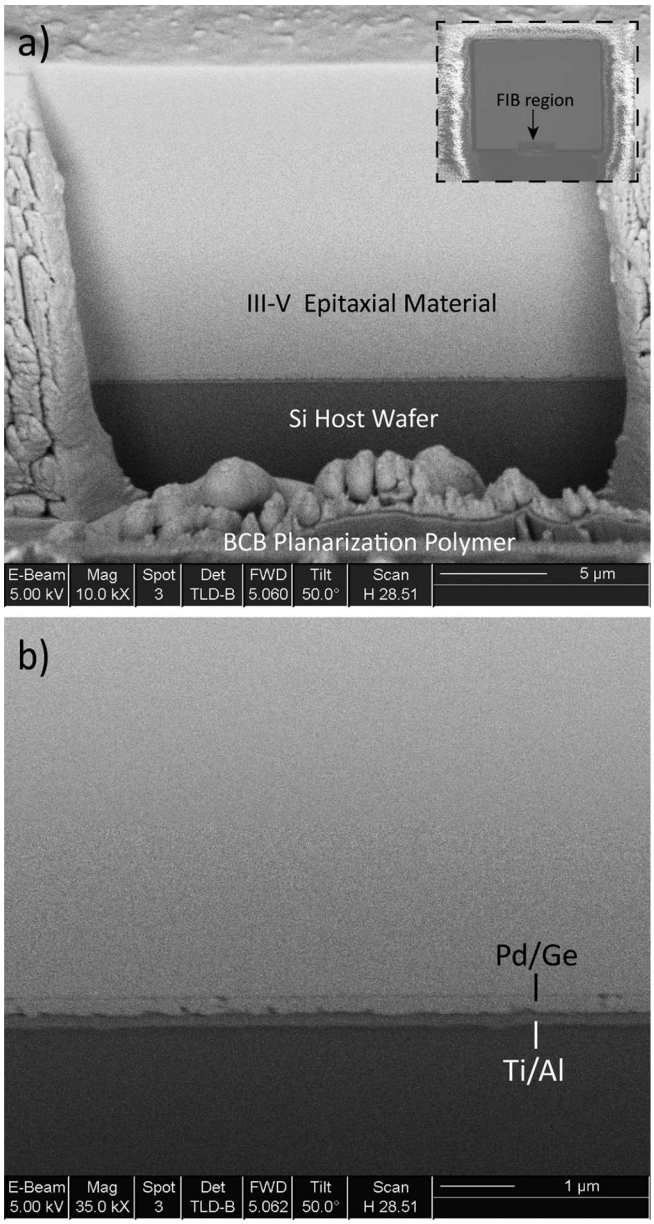

Figure 10. Inspection of interconnect interface between integrated heterogeneous materials. Resulting scanning electron micrographs of focused ion-beam milling (FIB-SEM) show a) the interface between the III-V epitaxial material and the silicon host wafer, and b) the eutectic bond between the materials that is shown to be smooth and void-less.

formed on SOI can be expected to have thermally insulating characteristics (thin film SiO_2, ~0.0005 $W \cdot cm^{-1}K^{-1}$[146]) that can impede photonic device performance at scalable system levels. It is further expected that the choice of integrating III-V on silicon substrate via eutectic bond will have improved thermal characteristics as compared to III-V devices on a native GaAs substrate, due to the low thermal conductivity of bulk GaAs relative to silicon.[47] The thermal mismatch between III-V and Si is therefore alleviated by the embedded metallic layer. Work is underway to compare integrated photonic devices to their native substrate counterpart.

Discussion

This work outlines a complete methodology for creating integrated material that is suitable for electronic-photonic circuitry, but may also be extended to the integration of other types of devices and materials.

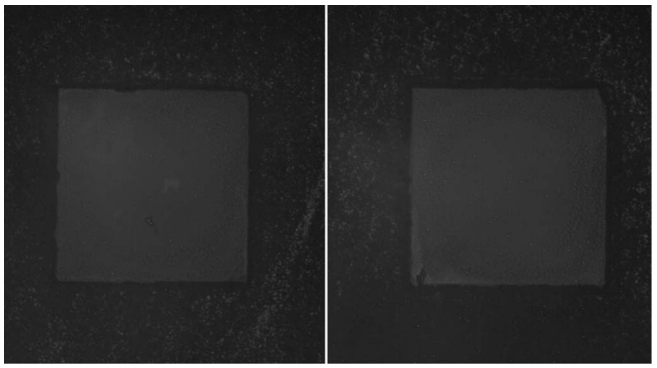

Figure 11. Infrared photomicrographs of the reflected light from the bond interface between III-V epitaxial material and host wafer. The bond is seen to be very uniform across different infrared inspections with no noticeable voids at the metallic interconnect layer.

Bulk III-V wafers are converted into integrated epitaxial layers atop a silicon host wafer in a CMOS-compatible fashion, establishing the blueprint for a network of photonic devices that can be patterned and interconnected in tandem with BEOL processing for patterned electronic gates. Owing to the metal contact that bonds the third-terminal of the photonic epitaxial material, there is the potential for directly improved thermal characteristics, improved high-speed performance, and incorporation of electronic controls for resulting integrated photonic devices. This establishes a fundamentally scalable platform for designing complex electronic-photonic circuitry, where the processes outline may be extended to other III-V materials and other photonic device designs to allow for even wider heterogeneity in an integrated system. Other epitaxial material structures, such as based on InP or GaN, can be utilized by this process with only minor refinement of the substrate removal and metallization processes. Work has begun on investigating this for GaN-based material designs, but further work is needed to verify the possibility of extending beyond three-terminal GaAs-based epitaxial structures. Additional variations for other types of device designs are possible with the same epitaxial bonding and transfer methods. Devices desiring high thermal conductivity with low electrical conductivity are implementable with this same technique given that, though the metal-eutectic bond layer is intrinsically both electrically and thermally conductive, a portion of a semi-insulating (SI) substrate can be left intentionally as part of a designed epitaxial stack to ensure that electrical isolation is maintained for an integrated III-V island. The epitaxial bonding and transfer process shown is also extendable for creating optical interconnects between active III-V photonic material, where epitaxial material made of dielectric or wide-bandgap semiconductor may be similarly patterned into islands and transferred in the same manner, followed by the definition of this material into passive waveguide or coupling structures. Alignment between the active and passive material for good optical transmission is ensured given that the definition of photonic devices occurs after all material has been integrated. This resulting network of three-terminal active photonic material has the advantage of interfacing directly with a CMOS system containing electronic or memory structures and allows for the collector terminal to link between electronic and photonic domains in sharing logic functions as needed. As such, epitaxial bonding and transfer hold promise in addressing the bottleneck in scaling up photonic devices from discrete to system-level by establishing new methods of bonding that can line up with CMOS-based interconnect methods.

Conclusions

Epitaxial bonding and transfer processes are developed and characterized to allow for the full integration of III-V material onto a CMOS-compatible host wafer. A temporary bonding polymer is used for epitaxial bonding to establish a large-scale distribution of fine-aligned III-V islands in a compatible manner with post-FEOL CMOS processing, while a permanent metal-eutectic alloy is formed and analyzed to ensure that an embedded interconnect between the third-terminal of HBT-based epitaxial structures and a CMOS host wafer can be formed while acting as the ohmic contact, thermal path, and mechanical bond for the III-V material. The heterogeneous integration of III-V onto silicon allows for the subsequent patterning of photonic devices atop silicon substrate as a separate chip layer for emerging multi-functional circuit designs.

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