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# Multi-chip heterogeneously integrated array of active three-terminal transistor lasers and passive photonic structures for electronic-photonic integration on silicon

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## ABSTRACT

An array of active photonic devices is fabricated in unison after a heterogeneous integration process first metal-eutectically bonds these distinct materials as a distribution onto a silicon host wafer. The patterning out of heterogeneous materials followed by the formation of all photonic devices allows for wide-area fine-alignment without the need for discrete die alignment or placement. The integration process is designed as a CMOS-compatible, scalable method for bringing together distinct III-V epitaxial structures and optical-waveguiding epitaxial structures, demonstrating the capabilities of forming a multi-chip layer of photonic materials. Integrated GaAs-based vertical light-emitting transistors (LET) are designed and fabricated as the active devices whose third electrical terminal provides an electrical interconnect and thermal dissipation path to the silicon host wafer. The performance of these devices as both electrical transistors and spontaneous-emission optical devices is compared to their monolithically-integrated counterparts to investigate improvements in device characteristics when integrated onto silicon. The fabrication methods are modified and optimized for thin-film transferred materials and are then extended to transistor laser (TL) fabrication. Passive waveguiding structures are designed and simulated for coupling light from the active devices, and their fabrication scheme is presented such that it can be similarly performed with transferred materials. Work toward the demonstration of integrated transistor lasers is shown to represent progress toward an electronic-photonic circuit network. The combination of heterogeneous integration with three-terminal photonic structures enables an elegant solution to both packaging and signal interconnect constraints for the implementation of photonic logic in silicon photonics systems.

**Keywords:** Heterogeneous integration, light-emitting transistor, transistor laser, CMOS-compatibility, photonic logic

## 1. INTRODUCTION

The capabilities of optical telecommunication systems have steadily grown due to the range of photonic devices and electronic controls available in a given network. These systems have pushed forward data throughput and are now well-established for long-haul and enterprise operations<sup>1</sup>. As network technologies have matured, industry interests have turned to the means of integrating photonic devices more intimately together on an electronics platform for more advanced circuit design. Such circuit systems would inherently present new considerations versus all-electronic device systems, but the allure of incorporating photonics at the node level remains given the high efficiency, coherence, and rapid speed available in the optical domain that together can enable more complex operations. In migrating to integrated photonic designs, device networks may move to the chip-to-chip scale and leverage established CMOS silicon technologies to build out new silicon photonic device designs that can show improved performance and control<sup>2</sup>.

The means to scalably interconnect between photonic and electronic devices is at the heart of new endeavors in electronic-photonic integrated circuitry. Owing to the range of materials capable of supporting photonic devices, a heterogeneous platform must be established that balances the manufacturing and material needs of integrating multiple photonic devices together in a scalable manner. A wealth of research has emerged, as a result, into methods of producing the heterogeneous integration of photonics based in III-V semiconductors onto a wafer native to electronics (silicon CMOS)<sup>3</sup>. Methods ranging from direct growth of III-V epitaxial structures on silicon to various wafer-scale bonding techniques have each been employed to prepare III-V materials on a scalable platform<sup>4,5</sup>. Yet the performance of resulting photonic devices formed in integrated III-V materials remains a concern, where sufficient yield, thermal sinking, and electrical conduction is needed to maximize device performance. Thus, the goal of electronic-photonic circuitry on silicon is to provide an electrical interconnect to the substrate and a horizontally aligned plane for optical interconnects, as shown in Figure 1a.

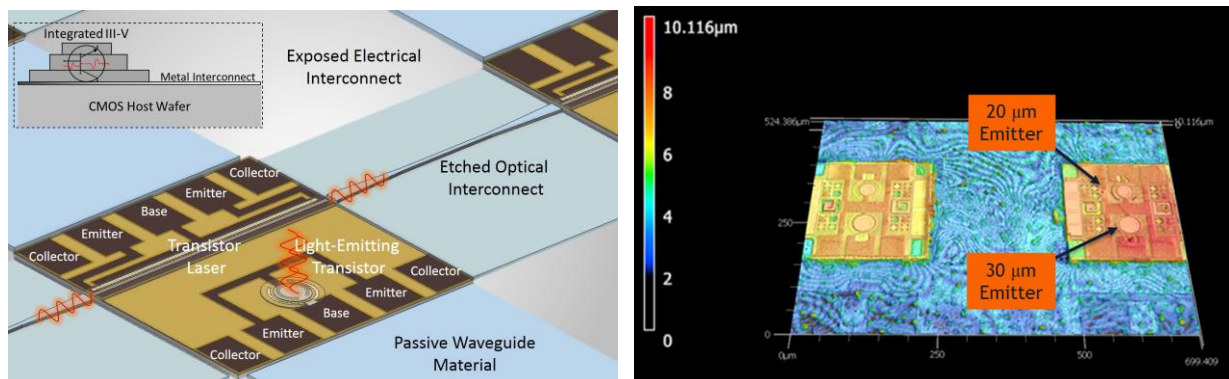


Figure 1a (left). Schematic of a multi-chip layout of active and passive photonic devices etched into epitaxially transferred and aligned materials as a heterogeneously integrated array on silicon (CMOS) with both electrical and optical interconnects shown. The inset shows the bonding process establishes an electrical interconnect from the Collector contact to the CMOS host wafer.

Figure 1b (right). 3D profile of the multi-chip array of integrated LETs.

The formation of photonic devices in modified heterostructures bipolar transistors (HBT) by the insertion of an InGaAs quantum well (QW) inside the p-GaAs Base region enables an elegant approach to novel electronic-photonic circuitry<sup>6</sup>. The resulting light-emitting transistors (LET) produce both an electrical and optical output from the single device, while the further confinement of light inside a cleaved cavity enabled transistor lasers (TL) that see further benefits in optical output and high-speed performance<sup>7</sup>. In line with the goals of silicon photonics, the three-terminal nature of the LET and TL presents unique opportunities in demonstrating a heterogeneously integrated photonic device array, where an electrical interconnect layer on silicon (CMOS) can be directly connected to the Collector terminal of the III-V material to form arrays of active photonic devices (Figure 1b) that can be optically guided toward through passive photonic devices. Electronic-photonic circuits can then be formed that interact between both electrical and optical domains, including the formation of photonic logic structures that would serve to extend the performance of silicon CMOS systems<sup>8</sup>.

This work describes the methods and analysis in establishing a photonic chip layer that consists of a lithographically-aligned array of active (LETs and TLs) and passive (waveguiding) photonic devices. An integration process is outlined and demonstrated that enables a distributed array of III-V epitaxial materials to form a thermal, electrical, and mechanical bond to a silicon (CMOS) host wafer by use of only CMOS-compatible fabrication methods. The integration method is designed so that it may fit in between front-end-of-line (FEOL) and back-end-of-line (BEOL) processing steps in standard CMOS fabrication<sup>9</sup>. A device fabrication process is then detailed, where the integrated III-V material are converted into an array of photonic devices in unison. The optimization and characterization of the fabrication processes is explained in detail, while additional simulation and early results for the integration of passive photonic elements is outlined. Electrical and optical device characterization is performed to analyze the expected device performance under a range of three-terminal inputs to establish the suitability of the device array for photonic logic applications.

## 2. METHODOLOGY

### 2.1 Epitaxial Bonding and Epitaxial Transfer

The approach for establishing a heterogeneously integrated platform of electronic-photonic circuitry devices relies on the method of integration. In contrast to past methods of integrating III-V onto silicon that rely on transfer printing<sup>10</sup> or insulating polymer bonding<sup>11</sup>, a metal-eutectic bond has been previously established by the authors and is pursued here to allow for an array of aligned III-V “islands” to be formed that each maintain an electrically and thermally conductive connection to the underlying silicon substrate<sup>9</sup>. The bonding process is divided into an epitaxial bonding and epitaxial transfer stage, detailed in Figure 2.

The epitaxial bonding process begins by cleaving a III-V epitaxial wafer into chiplets that can be assembled onto a silicon carrier wafer for processing. The LET and TL epitaxial layers are GaAs-based and the wafer thickness is initially 650 μm. A durable temporary bonding polymer is spun-on to a silicon carrier wafer (50 mm) and the III-V chiplets are manually

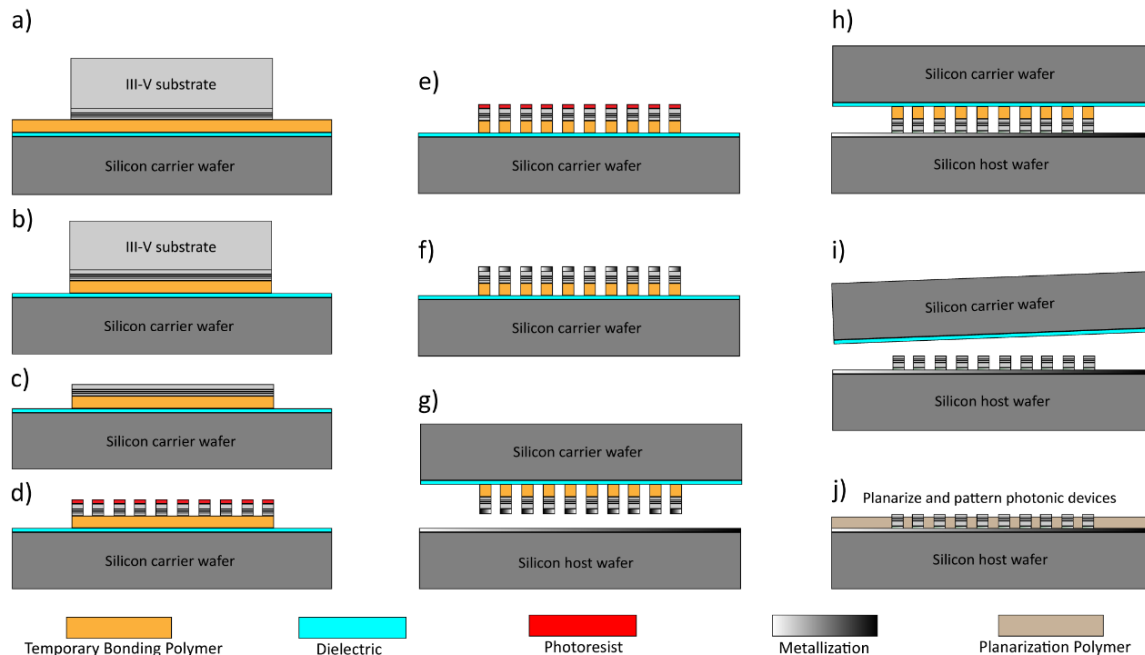


Figure 2. Schematic of integration processes of epitaxial bonding and epitaxial transfer for III-V photonic materials [9].

placed onto the polymer epi-side down (Figure 2a), followed by a curing process that serves to securely fasten the polymer to each III-V chiplet. The excess, exposed polymer is then dry-etched by an oxygen plasma recipe (Figure 2b) and the bulk of the GaAs substrate is removed by a combination of diamond-pad lapping and chemo-mechanical polishing (CMP), reducing the total thickness of the bonded materials to below 10  $\mu\text{m}$  (Figure 2c) and exposing the Collector terminal of the epitaxial layers. Additional thinning can be achieved by submerging the III-V materials in a  $\text{NH}_4\text{OH}:\text{H}_2\text{O}_2:\text{H}_2\text{O}$  wet-etch, where the selectivity of GaAs to the bonding polymer is favorable.

Following the removal of the bulk substrate of the III-V wafer, lithography is performed on the remaining thin-film III-V epitaxial layers to convert the broad area material into an aligned array of “III-V islands” whose Collector terminals are faced upwards. A chlorine-based dry etch is used to remove the excess III-V material, leaving the III-V islands atop the bonding polymer (Figure 2d), and the exposed polymer is again etched in an oxygen plasma (Figure 2e). A CMOS-compatible Pd(500  $\text{\AA}$ )/Ge(1265  $\text{\AA}$ ) Ohmic contact is then evaporated and annealed onto the exposed n-GaAs Collector of each III-V island (Figure 2f)<sup>12</sup>.

The epitaxial transfer process then commences by preparing a silicon host wafer (50 mm) to emulate a CMOS wafer that has proceeded through FEOL processing. A standard metallization recipe of Ti(500  $\text{\AA}$ )/Al (1500  $\text{\AA}$ ) is evaporated onto the host wafer to produce the electrical interconnect layer that serves as the electrical and thermal bond for the photonic chip layer. The silicon carrier wafer containing the III-V islands terminated in germanium is then brought into contact with the silicon host wafer containing the electrical interconnect layer terminating in aluminum. A wafer bonding tool unites the carrier and host wafer and performs a metal-eutectic bond, where a force of 800 N is applied as the temperature ramps above the eutectic point of Al-Ge and then down again (Figure 2h), bringing the stack of materials to a state where the aluminum and germanium may bond and secure the III-V islands permanently. Following the bonding process, a final solvent bath removes the temporary bonding polymer from the stack of materials (Figure 2i) and the bonded array of III-V materials are dry-etched in an oxygen plasma to remove any residue from the polymer (Figure 2j). Following the epitaxial bonding and epitaxial transfer processes, the III-V islands are Emitter side up with the Collector Terminal embedded underneath the III-V island and interconnected to the host wafer.

The bonding process has been established and is here extended to the use for three-terminal photonic devices. The result of the process is a scalable means of converting bulk III-V substrates into their thin-film epitaxial structures; as such, the process is extendable to other substrates and photonic device designs, including wide-bandgap and dielectric based epitaxial structures that can serve as low-loss passive photonic devices.

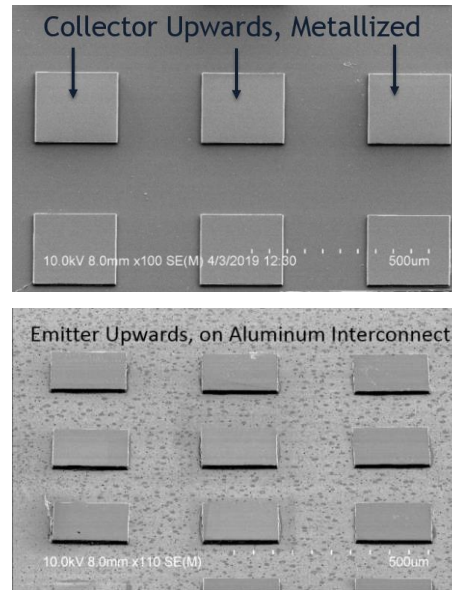
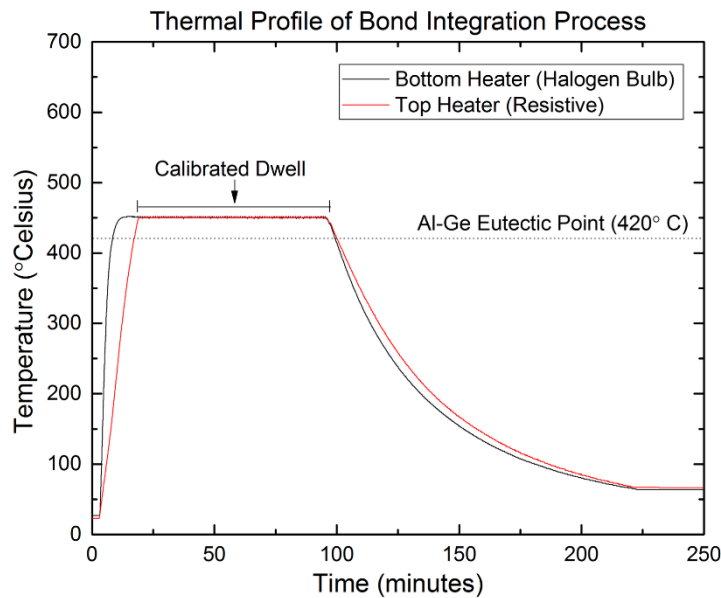


Figure 3a (left). Plot of the thermal profile over time for the metal-eutectic bond. The eutectic point of Al-Ge is shown.  
 Figure 3b (top right). Scanning electron micrograph of the results of the epitaxial bonding process showing the III-V islands.  
 Figure 3c (bottom right). Scanning electron micrograph of the results of the epitaxial transfer onto the host wafer.

The thermal profile seen by the III-V islands during the metal-eutectic bonding process is shown in Figure 3a. A calibrated dwell time between 60-80 minutes is used to ensure that the metal stack on the Collector terminal of the III-V islands sees sufficient thermal energy to reach a eutectic point with the electrical interconnect layer underneath, followed by a slow ramp-down time such that the metal stack slowly retreats below the Al-Ge eutectic point of 420° C as one bonded stack. The results of the epitaxial bonding process is shown in Figure 3b, where the metallized Collector terminals of the III-V islands on top of the bonding polymer is shown. The result of the integration process is shown in Figure 3c, where the epitaxial layers have flipped over and the Emitter terminal is now properly face-up. Mild pitting of the aluminum interconnect layer is visible in the epitaxial transfer photo, owing to a dilute wet-etch performed on the metal surfaces before bonding to remove any surface oxides. Together, the results are promising in showing that arrays of III-V islands can be bonded onto a silicon substrate for the purposes of forming active and photonic devices.

## 2.2 Device Modeling

A typical single-heterojunction HBT is designed as an n-InGaP (Emitter)/p-GaAs (Base) /n-GaAs (Collector) structure, where the band offsets between the InGaP and GaAs produce an electron-dominating current flow. The modified HBT that forms the LET and TL structure incorporates an InGaAs QW inside the p-GaAs Base, providing an additional mechanism for carrier recombination inside the Base<sup>13</sup>. In forward active mode under Base current, injected electrons come from the Emitter into the Base while holes are injected from the Base into the Emitter. A portion of the Base carriers in transit to the Collector is lost to recombination processes, including Auger and Hall-Shockley-Reed recombination, but of particular significance is the radiative recombination component that is greatly enhanced by the inclusion of the QW in the Base. It is noted that:

$$I_E = I_B + I_C$$

where  $I_E$  is the Emitter current,  $I_B$  is the Base current, and  $I_C$  is the Collector current, in total accounting for all elements of the device current profile. By this, the injected Base current must account for all elements of recombination as well. The LET and TL epitaxial structure is plotted in Figure 4, using a non-equilibrium Green's function (NEGF) solver to

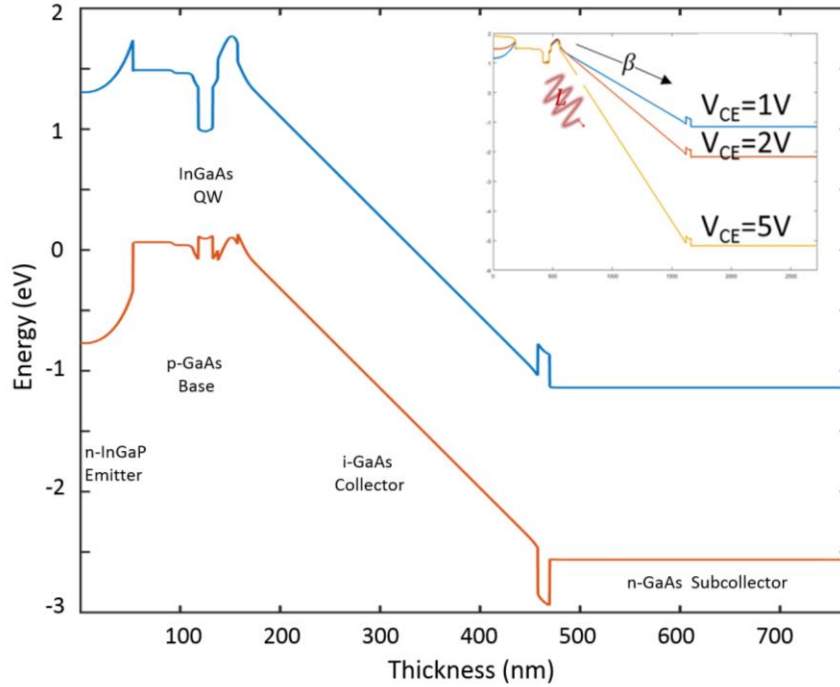


Figure 4. Band structure simulation of the three-terminal III-V epitaxial layers used in fabrication and integration. The inset shows the Conduction band offset under  $V_{CE}$  bias, where the comparison between gain and light output is shown.

produce a self-consistent solution to the Emitter-Base and Base-Collector junctions, under the assumption of low Base current injection<sup>14</sup>. In this profile, it is seen how carriers (electrons) injected from the Emitter at the left would be captured by the QW and amplify electron-hole recombination and its corresponding Base current element, as well as how increasing biasing ( $V_{CE}$ ) across the Collector-Emitter would produce larger band bending. Under biasing conditions where an excess minority carrier density exists inside the neutral Base, the radiative recombination Base current component becomes<sup>13</sup>:

$$I_{B,rad.} = \frac{qA\Delta n}{\tau_{rec.}} \propto L \text{ (Watts)}$$

where  $q$  is the charge of the electron,  $A$  is the Emitter area,  $\tau_{rec.}$  is the Base recombination lifetime, and  $\Delta n$  is the excess minority carrier (electron) density. It is seen here that the intensity of the light output is directly related to this component of radiative recombination, as well as how a larger area Emitter can account for larger optical components of the three-terminal device operation. The Base recombination lifetime,  $\tau_{rec.}$ , for bulk GaAs has previously been calculated at 134 psec, but with the inclusion a QW it drops to below 40 psec and then further still when driven above current threshold to stimulated emission<sup>15</sup>, indicating further enhancement of the  $I_{B,rad.}$  element (and thus light output) in the continuity conditions based on the Base current injection.

The crucial condition for three-terminal photonic devices is then the expectation that carriers will either recombine radiatively or will pass through to the Collector terminal and provide electrical gain. The electrical gain equation for a standard HBT under common-Emitter configuration is:

$$\beta = \frac{I_C}{I_B} = \frac{\tau_{rec.}}{\tau_b}$$



where  $\tau_b$  is the Base transit time for carriers<sup>13</sup>. The transit time is not expected to increase with Base current, but  $\tau_{rec.}$  is expected to reduce as the minority carrier conditions approach threshold, producing the indication that increased light output will reduce electrical gain, or:

$$\beta_{stim.} < \beta_{spon.} < \beta_{HBT}$$

A device design is then pursued to compare Emitter mesa areas directly to inspect the light output relative to the electrical gain achieved for a given Emitter mesa size<sup>16</sup>, with 20  $\mu\text{m}$  and 30  $\mu\text{m}$  diameter mesas chosen for the initial LET measurement. Beta-compression is a well-defined feature of previous TL and LET experiments, as well as it serves as a helpful indicator regarding the onset of lasing in a cavity<sup>15</sup>. A common-Emitter configuration is also chosen to match to the theoretical expectations.

### 2.3 Device Fabrication

The completion of the epitaxial bonding and epitaxial transfer processes prepares III-V islands on a silicon (CMOS) host wafer as bonded by the aluminum electrical interconnect. A series of processing steps have been developed to then convert III-V islands into an array of active photonic devices in unison. Given that the III-V islands are bonded in a photolithographically-defined array, micron-scale fine alignment is ensured by the nature of the bonding process. The III-V island dimensions are 250  $\mu\text{m}$  x 250  $\mu\text{m}$  with a pitch of 500  $\mu\text{m}$  in each direction for the LET islands, and a dimension of 500  $\mu\text{m}$  x 380  $\mu\text{m}$  with a pitch of 750  $\mu\text{m}$  and 1.5 mm, respectively, for the TL islands. The TL islands are distributed in such a way where the cavity length is along the 380  $\mu\text{m}$  length and are arranged to enable the subsequent bonding and close proximity of passive photonic elements to the edge-emitting facet of the active device multi-chip array. Additional considerations are that the host wafer can be safely diced for full analysis and power reading of the edge-emitters.

Following the oxygen plasma cleaning process that concludes the epitaxial transfer process (Figure 5a), the arrangement of III-V islands on each host wafer is then planarized with the low- $\kappa$  dielectric benzocyclobutene (BCB). The BCB polymer

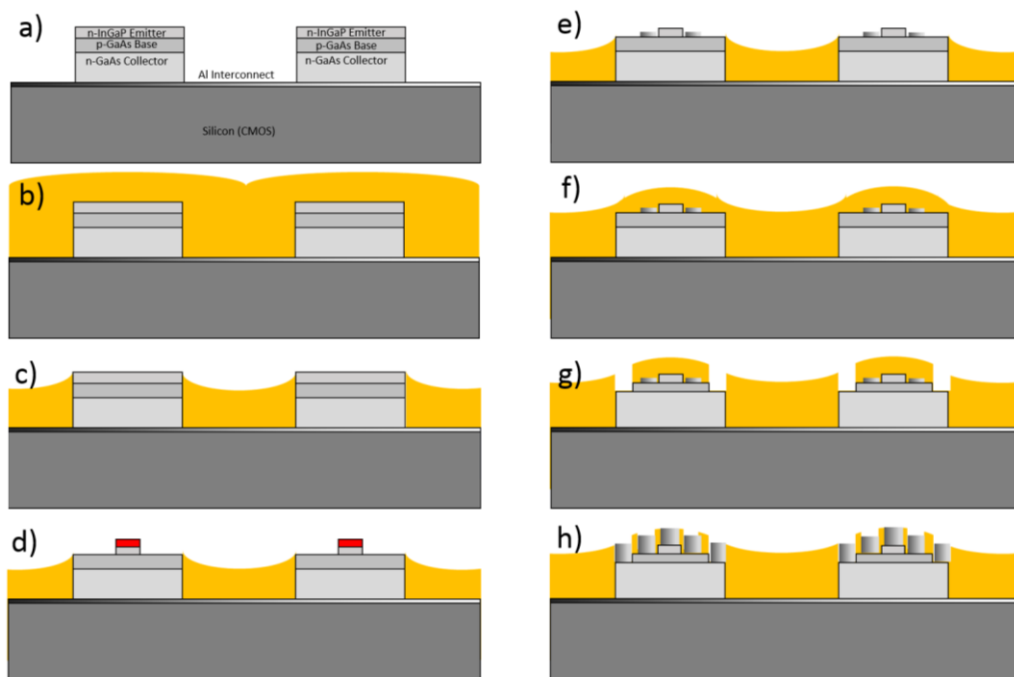


Figure 5. Schematic of integrated three-terminal photonic device fabrication processes. The epitaxially bonded materials are a) prepared and cleaned, b) planarized with BCB, c) dry-etched to remove excess BCB and to open Emitter terminal surface, d) dry-etched to open Base floor, e) metallized with Base contact, f) planarized and isolated with BCB, g) dry-etched to remove excess BCB and then dry-etched to open Collector trench, h) dry-etched to open remaining contacts and metallized with Emitter and Collector metal.

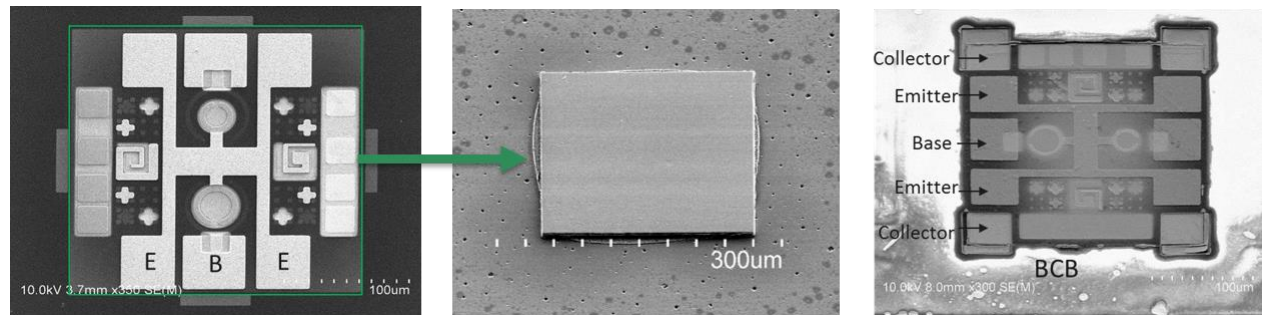


Figure 6. Scanning electron micrographs showing (left) the completed monolithic LET, (center) an integrated III-V island whose dimensions match the monolithic LET, and (right) the integrated LET with both 20  $\mu\text{m}$  and 30  $\mu\text{m}$  mesas.

is spun-on at a thickness that fully encases the silicon (CMOS) host wafer and the III-V islands as well (Figure 5b). This provides the benefit of creating a planar surface for subsequent processing but also it shields the interconnect layer on the silicon (CMOS) host wafer from developers and wet-etch solutions that may attack aluminum. A Freon-based RIE dry-etch is used to perform an etchback and remove the excess BCB, opening up the Emitter terminal of the III-V active material (Figure 5c).

The opened-up Emitter surface is then photolithographically prepared for the Base floor opening. For the LET fabrication structures, the Emitter mesas chosen are one 20  $\mu\text{m}$  diameter and one 30  $\mu\text{m}$  diameter per square III-V island, allowing for sufficient room around each device for probing pads and other testing structures. A chlorine-based dry-etch process is initially used to remove the GaAs Emitter cap and the underlying InGaP Emitter, followed by a dilute HCl wet-etch to cleanly remove the residual InGaP Emitter and stop right at the p-GaAs Base floor (Figure 5d). With the p-GaAs Base floor now exposed, a CMOS-compatible Ohmic contact of Ni(50 Å)/Ti(50 Å)/Pt(50 Å)/Ti(300 Å)/Pt(1000 Å) is evaporated and annealed to enclose the Emitter mesa diameter for optimal current injection (Figure 5e)<sup>17</sup>.

To isolate the Base and Emitter terminals, a second layer of BCB is spun-on and cured to ensure that a strong electrical insulation exists between the overlapping contacts (Figure 5f). A selective removal of the BCB is then performed to open up the Base floor to the edges of the III-V island for the formation of the Collector trench etch (Figure 5g). The Collector is revealed by a similar chlorine-based dry-etch process and a final dilute HCl wet-etch, selectively removing the Base material and stopping at the upper edge of the Collector epitaxial layers. It is noted that in high-speed LET designs, the sub-Collector is unintentionally-doped (UID) for better performance, so the question of where to terminate the Collector etch so as not to etch past n-GaAs must be calibrated and actively considered.

The final stage of the integrated device fabrication involves further Freon-based RIE dry-etching to open up the Emitter mesa and the Base terminal metal contacts. Following this, the CMOS-compatible n-GaAs metal structure previously used to metal-eutectically bond the III-V islands is again employed as the top-side Emitter and Collector contact, as well as it is evaporated onto the Base Ohmic contact to provide for a sturdier probing pad that can sufficiently rise out from the opening in the BCB (Figure 5h). The same processing steps are shown to apply to the formation of a TL array.

The processing results for the LET active device design are shown in Figure 6. The initial LET design fabricated on a monolithic substrate are shown on the left side, where the two comparing Emitter mesas are in the center. This design is then transferred onto an integrated III-V island, where the design matches to the dimensions of a particular III-V island as shown in the center, and the resulting integrated LET is what is shown on the right. The Emitter mesas are again in the center and the Collector trenches are shown on the four corners of the III-V island that is planarized in insulating BCB.

### 3. RESULTS

#### 3.1 Active LET's

A comparison is performed between monolithic active devices and their integrated counterparts with identical CMOS-compatible metallization. The monolithic devices are formed with the same dimensions as the integrated devices. The results of the comparison are shown in Figure 7. In the comparison, it is shown that the 20  $\mu\text{m}$  devices produced stronger



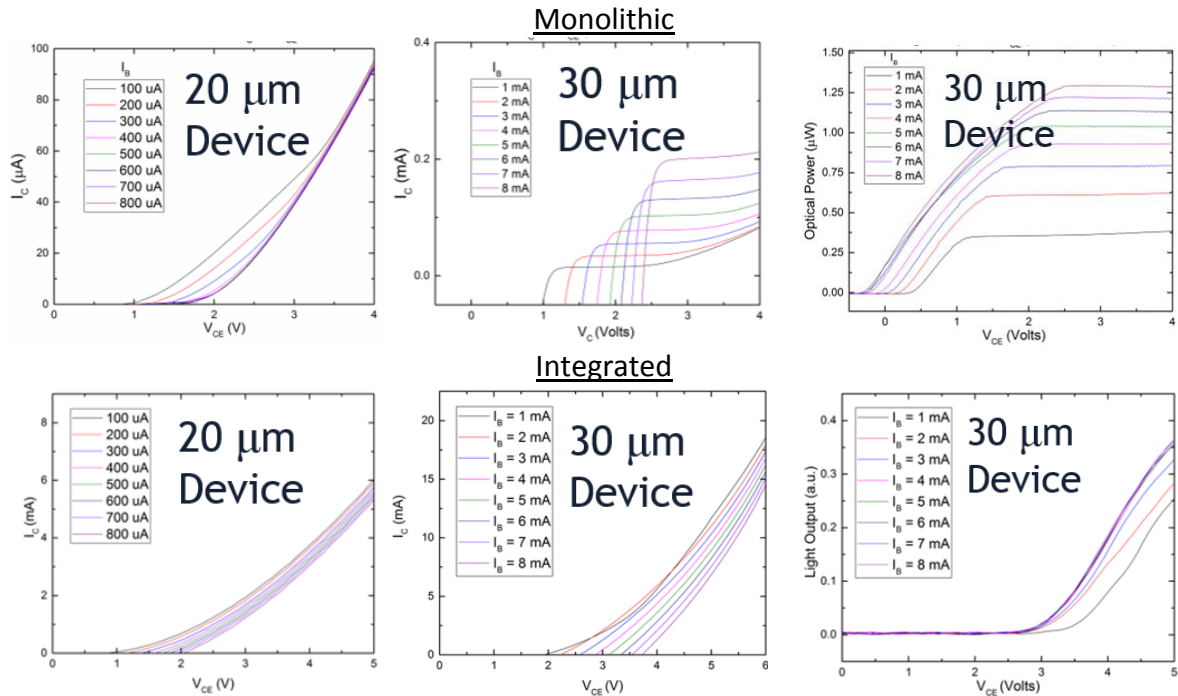


Figure 7. Comparison of the measured family of curves for the monolithic and integrated LET active photonic devices. The electrical gain families are on the left and the optical output families are on the right.

electrical gain than 30  $\mu\text{m}$  devices at earlier Base currents within the family of curves. The optical comparison found that much more light was apparent and measurable on the 30  $\mu\text{m}$  devices than on the 20  $\mu\text{m}$  devices, in good agreement with the notion that the 20  $\mu\text{m}$  devices would have smaller  $I_{B,rad.}$  and thus a larger component of carriers that reaches the Collector terminal. This was clear on both the monolithic and the integrated devices, where substantially less light from the 20  $\mu\text{m}$  devices relative to the 30  $\mu\text{m}$  ones. The range of optical output values ( $\lambda=980$  nm) from the integrated LETs varied over the devices, implying further iteration and optimization of the dry-etch profile would help. The combined results comparing the electrical gain to the optical output on a single monolithic device is shown in Figure 8. Beta-compression is apparent in the device profile, where the larger Base currents quickly diminish electrical gain while optical

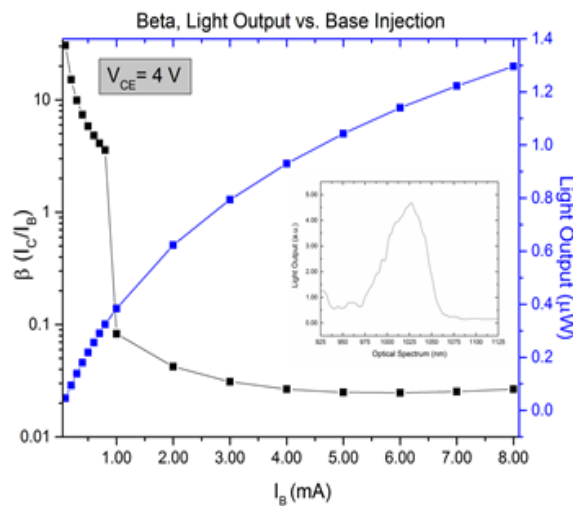


Figure 8. Comparison of measured electrical gain ( $\beta$ ) and light output ( $\mu\text{W}$ ) across injected Base current values. Inset image shows the measured optical spectrum of the spontaneous emission from the LET.

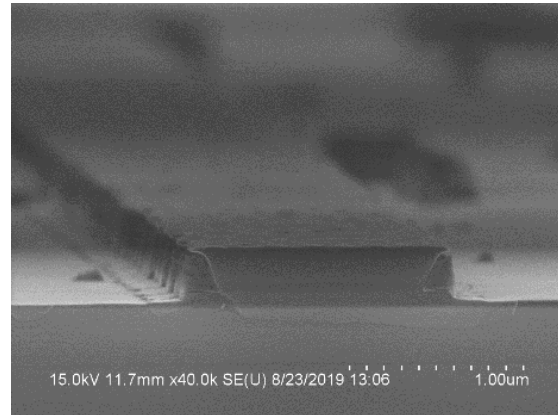
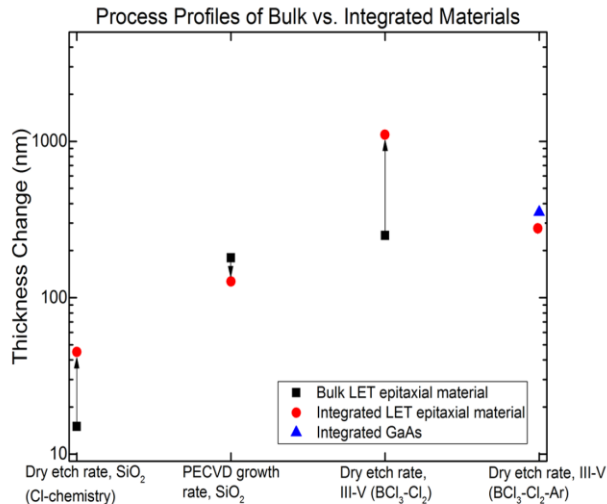


Figure 9a (left). Process parameter comparison of dry-etching III-V epitaxial structures on the native bulk substrate (~650 μm) and as an integrated thin film on a metal-eutectic layer on silicon.

Figure 9a (right). Scanning electron micrograph of an Emitter mesa stripe after timed wet-etch. The anisotropy of the wet-etch is apparent in the image.

output more gradually increases. This signifies that, by choice of Base current, a single three-terminal device can be utilized in electrical gain or optical output mode in a given electronic-photonic circuit. These principles can be extended to TL designs and related to running a device above and below threshold current, where it is known that  $\beta$  will vary.

### 3.2 Fabrication Optimization

The results from processing and fabricating the photonic devices showed that variation in the dry-etch processes became apparent in the thin-film integrated III-V islands relative to the bulk monolithic devices. An analysis was undertaken to investigate this and examine methods to eliminate these variations. The results, shown in Figure 9a, were found to show that the dry-etch rates in thin-film devices accelerate relative to their monolithic counterpart. As is seen in the plot, both the etch rate of the hard masks in a chlorine chemistry dry-etch and the etch rates of the III-V epitaxial structures saw much faster etching times that posed questions on how to calibrate for this change. These changes are likely due to an additional thermal component present in the ICP-RIE dry-etch that is not present in the monolithic device case.

Given that the thermal conductivity of the III-V materials is lower than the silicon host wafer (substrate), it is unlikely that the removal of the III-V substrate created excess heating and thus sped the etch rates up. Instead, the explanation for this etch rate speed-up stems from the fact that the aluminum interconnect layer is exposed to the RF radiation during the ICP-RIE dry-etch processes and will accumulate heat at the interface of the III-V islands during a dry-etch process, causing rapid etch acceleration due to the thermal profile at the exposed GaAs surfaces.

To remedy this and prepare a modified fabrication process for the thin-film devices, a series of wet-etch processes are employed to enable a less-thermally sensitive etch process and also to provide for a smoother Base and Collector terminal floor for metallization. The wet-etch chosen for the Base floor opening is a combination of a NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (4:1:8) dilute etch solution that is used to remove the Emitter InGaAs/GaAs cap layers, followed by a HCl:H<sub>2</sub>O (1:1) wet etch that readily removes the InGaP Emitter and chemically stops right at the p-GaAs Base interface. These wet-etch solutions produce smoother floors and were confirmed to enable stronger initial diode performance tested across the Emitter-Base and Base-Collector structures. The wet-etch for the Collector trench opening follows the same two etch steps, where the NH<sub>4</sub>OH:H<sub>2</sub>O<sub>2</sub>:H<sub>2</sub>O (4:1:8) is used to remove the GaAs-based Base and AlGaAs layers, followed again by an HCl:H<sub>2</sub>O (1:1) wet-etch to remove the etch-stop layer just before the n-GaAs Collector terminal. Owing to the HCl etch used, sufficient BCB planarization over the electrical interconnect is necessary so as not to remove the aluminum layer and risk damage to the III-V islands after active device processing.

The results from the initial wet-etch tests are shown in Figure 9b, where a 2  $\mu\text{m}$  stripe is formed out of the Emitter layers with strong anisotropy and good hard mask retention throughout the etch. The surface looked cleaner than prior dry-etched surfaces and the conversion from dry-etch to wet-etch is pursued for the integrated devices.

### 3.3 TL Modal Simulation

The III-V epitaxial structure is extended in usage from the LET vertical emission design to allow for a lateral edge-emitting TL design while still maintaining the CMOS-compatible wet-etch and fabrication techniques as optimized. To confirm that the epitaxial structure of the III-V islands can support an edge-emitting modal profile with minimal loss at the three-terminal metal contacts, a series of finite-element method (FEM) solver simulations are employed. The figure of merit investigated is the percentage of modal power overlap within 100 nm ( $\sim \lambda/10$ ) of the top Emitter contact, so as to minimize the absorption of the optical power at the surface.

Shown in Figure 10a, the results of the FEM simulation are shown across a range of designs. The designs compare between a 6  $\mu\text{m}$  or 15  $\mu\text{m}$  wide Base stripe and either a single or a pair of narrow Emitter mesa stripes (1.5, 2  $\mu\text{m}$ ) so as to confine the optical modal power ( $\lambda=980\text{ nm}$ ) downward and away from the upper metal contact. The optimal performance is shown to be a two-stripe (each 2  $\mu\text{m}$  wide) design, as it has a minimized 3.4% modal power within the top 100 nm of the device (Figure 10b). This design is carried forward into mask development, along with a comparison structure of a single 4  $\mu\text{m}$  wide stripe.

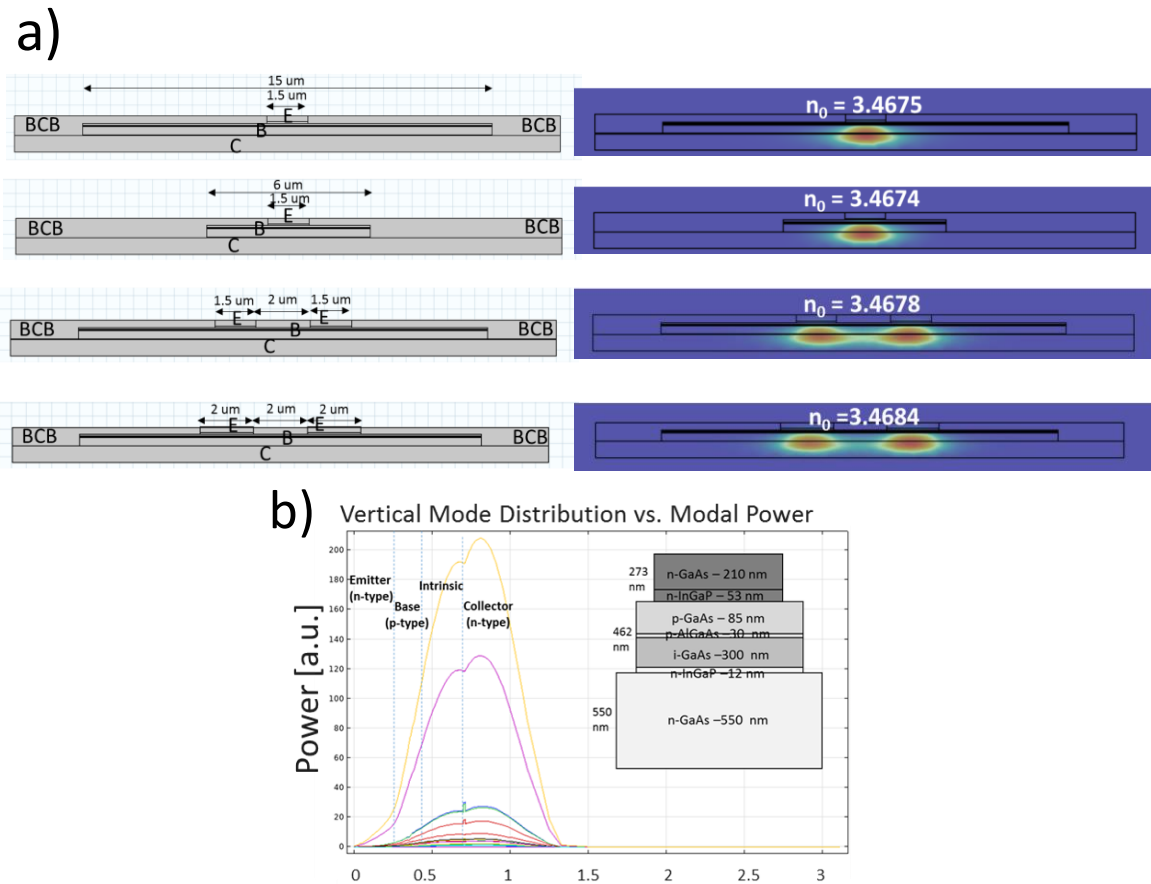
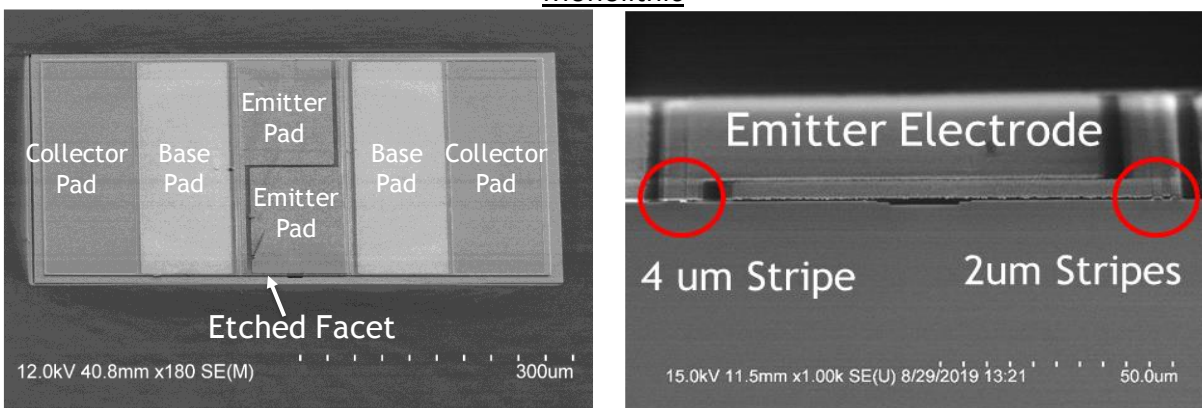


Figure 10a (top). FEM solver profiles of the electromagnetic modal profile in the III-V epitaxial structure. The profiles range across a set of Emitter mesa stripe widths and the effective modal index is listed above the modal profile.

Figure 10a (bottom). Plot of modal power distribution along vertical axis of Emitter mesa stripe. The inset shows the III-V epitaxial structure thicknesses for comparison.

### Monolithic



### Integrated

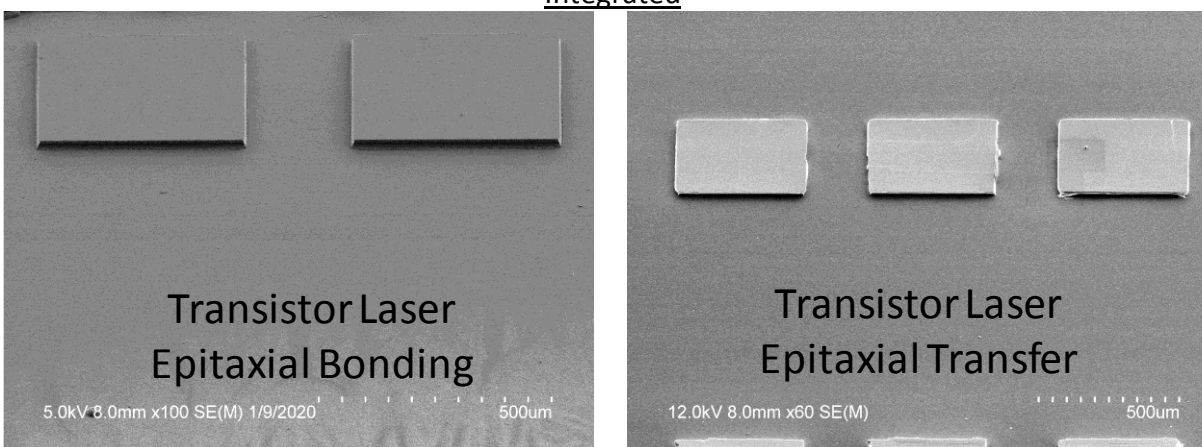


Figure 11. Scanning electron micrographs of the monolithically fabricated TL structures and the multi-chip integrated array of III-V islands for TL structures.

### 3.4 Active TL Fabrication

The fabrication techniques outlined for the integrated spontaneously-emitting LETs are utilized for the edge-emitting TL structure design, as outlined in Figure 5. The initial design is tested on a monolithic GaAs substrate, similar to the LET device comparison. The TL structures are lithographically patterned out with an isolation trench to the Collector terminal between the two-stripe and single stripe design layout, and both the Emitter mesa and Collector trench are defined with the aforementioned wet-etch schemes.

The wet-etch profiles produce smooth floors for proper metal evaporation coverage. Shown in Figure 11, the monolithic device layouts are fully fabricated to emulate the multi-chip layout. Cleaved facets are created in the monolithic devices to inspect the Emitter stripe anisotropy, and the test confirms the suitability of the wet-etch technique as a CMOS-compatible technique for sufficient photonic device stripes. A set of TL III-V islands are then patterned using the epitaxial bonding and epitaxial transfer process and the technique is iterated to confirm the integration process works for the larger III-V islands. The results of the multi-chip integrated of the TL structures is shown in Figure 11, where the alignment of the devices is still maintained after the metal-eutectic bonding process.

### 3.5 Passive Photonic Device Modeling

The process for integrating active materials carries forward to passive photonic materials and utilizes the same integration strategy. Combining epitaxial bonding and epitaxial transfer again, a range of transmissive optical materials can be

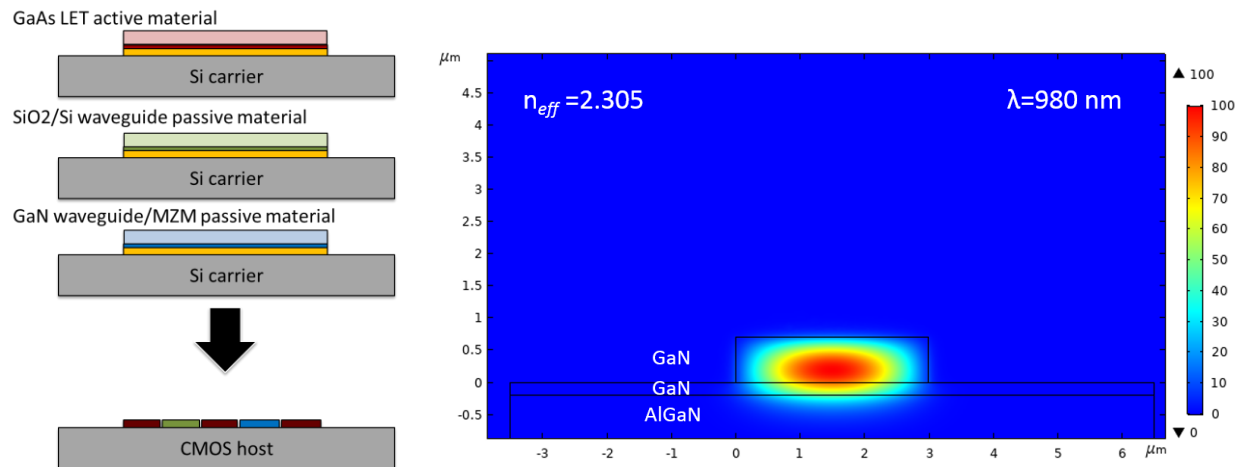


Figure 12a (left). Schematic of the bond-alignment process to bring together dissimilar active and passive photonic materials for a single heterogeneous platform.

Figure 12b (right). FEM electromagnetic modal pattern of fundamental single mode in a passive, waveguiding GaN/AlGaN/Si(111) waveguide.

incorporated onto the same heterogeneously integrated platform. Shown in Figure 12a, the strategy relies on a bond-alignment technique. Once the metal-eutectic bond has been secured between the III-V islands and the silicon (CMOS) host wafer, additional carrier wafers containing III-V or dielectric materials can be prepared and converted into a distributed array of islands as well. The use of photolithography to etch and pattern the materials again ensures a distribution of fine-aligned materials, suitable for the fabrication of optical coupling structures that taper and match directly to the outset of the edge-emitting active photonic devices.

Early work in the simulation and fabrication of wide-bandgap waveguides formed of GaN-based epitaxial structures has been performed. The GaN waveguides have the benefit of being lossless at near-infrared wavelengths and of exhibiting other nonlinearities in the crystal that potentially can be explored for other forms of passive photonic structures. Figure 12b shows a FEM solver model showing how similar fabrication processes and geometries can be tailored to match modal distributions from active to passive photonic elements. In doing this, numerous active elements can work in tandem and coordinate complex electronic-photonic circuitry by means of propagating their signals through the passive structures composed of GaN or other dielectric waveguides.

## 4. CONCLUSION

This work presents the steps for designing, fabricating, and implementing a multi-chip array of integrated transistor lasers based off the fabrication and modeling techniques from the formation of arrays of integrated light-emitting transistors. The combination of heterogeneous integration and three-terminal photonic devices is presented as a means for establishing photonic logic designs, where the metal-eutectic bond between the Collector terminal and the BEOL aluminum interconnect allows for a thermal path and an electrical connection to exist, in contrast to other bonding techniques. The methods of heterogeneous integration for active devices can then be expanded to passive photonic devices with new analyses in wide-bandgap and dielectric-based passive structures that can be similarly bonded and fine-aligned using bond-alignment techniques. These devices in a distributed array can enable electronic-photonic integrated circuits where active photonic elements based on three-terminal device designs can interact with both an underlying silicon electronics network by way of an electronic interconnect and an in-plane optical network by way of coupling to passive photonic structures that act as optical interconnects in a photonic chip layer. The performance of the three-terminal devices is analyzed under both monolithic and integrated device constraints, while the methods and techniques for using integrated photonic devices in a photonic logic network are discussed and the modal profile of such devices are simulated. These results together are



presented as building blocks for a CMOS-compatible large-area patterning of distinct III-V materials and waveguiding materials that can be brought together to form a truly heterogeneous platform of electronics and photonics circuit elements.

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