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Heterogeneously integrated VCSELs on silicon

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ABSTRACT

A wafer-scale CMOS-compatible process for heterogeneous integration of III-V epitaxial material onto silicon for photonic device fabrication is presented. Transfer of AlGaAs-GaAs Vertical-Cavity Surface-Emitting Laser (VCSEL) epitaxial material onto silicon using a carrier wafer process and metallic bonding is used to form III-V islands which are subsequently processed into VCSELs. The transfer process begins with the bonding of III-V wafer pieces epitaxy-down on a carrier wafer using a temporary bonding material. Following substrate removal, precisely-located islands of material are formed using photolithography and dry etching. These islands are bonded onto a silicon host wafer using a thin-film non-gold metal bonding process and the transfer wafer is removed. Following the bonding of the epitaxial islands onto the silicon wafer, standard processing methods are used to form VCSELs with non-gold contacts. The removal of the GaAs substrate prior to bonding provides an improved thermal pathway which leads to a reduction in wavelength shift with output power under continuous-wave (CW) excitation. Unlike prior work in which fully-fabricated VCSELs are flip-chip bonded to silicon, all photonic device processing takes place after the epitaxial transfer process. The electrical and optical performance of heterogeneously integrated 850nm GaAs VCSELs on silicon is compared to their as-grown counterparts. The demonstrated method creates the potential for the integration of III-V photonic devices with silicon CMOS, including CMOS imaging arrays. Such devices could have use in applications ranging from 3D imaging to LiDAR.

Keywords: VCSELs, heterogeneous integration, integration, wafer bonding, silicon photonics

1. INTRODUCTION

A future of seamless electronic-photonic integration with active photonic layers on a CMOS IC could be enabled by the epitaxial transfer of III-V materials optimized for optical devices onto a traditional silicon wafer upon which electrical devices have already been fully or partially defined. An approach to realizing this future is through the bonding of III-V materials onto silicon using a carrier wafer process in which the III-V substrate is removed. Following permanent bonding to a silicon host wafer, this heterogeneously integrated material will have a lower thermal impedance path for the optical devices by replacing lower thermal conductivity GaAs with higher thermal conductivity silicon. Additionally, heterogeneous integration allows for direct on-wafer connections between the optical and electric devices.[1] While prior work with VCSELs has chosen to approach integration using flip-chip bonding of fully-fabricated individual devices onto silicon,[2] the approach described here, where the integration of III-V material with silicon is done prior to device fabrication, allows for both precise photolithographic alignment of integrated photonic devices to existing features on the host wafer and for the fabrication of photonic devices in uniform arrays across the silicon host wafer.[3]

The methodology of integrating III-V material with silicon using epitaxial transfer has been previously established,[1,3,4,5] however this technique has not been applied to the fabrication of vertical cavity surface emitting lasers (VCSELs). In this paper we investigate 850 nm, 10 μm oxide aperture VCSELs that are successfully fabricated on integrated AlGaAs VCSEL material after an epitaxial transfer process. Using CMOS-compatible integration methods, this research shows that the described integration approach based on standard processing methods and tools can be used to produce heterogeneously integrated lasing devices. With improved thermal pathways provided by the integration on silicon, these devices are shown to have less thermal shift in their emission wavelengths when compared to their as-grown counterparts, indicating improved thermal resistance for a wide range of operating conditions.

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2. METHODOLOGY

2.1 Heterogeneous integration of epitaxial material with silicon

The epitaxial VCSEL material is integrated with a silicon wafer via the CMOS-compatible process depicted below in Figure 1 using the process flow described in Carlson, et al.[1] After temporary bonding to a silicon carrier wafer, the VCSEL epitaxy wafer substrate is thinned via chemo-mechanical lapping and polishing to a thickness of 18 µm. With an epitaxial structure thickness of 9.41 µm, the remaining GaAs substrate is determined to be approximately 8.6 µm. Typically, it is desirable to remove as much of the less thermally conductive GaAs substrate as possible to reduce the thermal impedance between the device junction and silicon, ideally leaving less than a few microns of GaAs. Here, a slightly thicker substrate layer is kept to minimize any disruption of the bottom DBR reflectivity caused by reflections from the bonding metal. The III-V material is photolithographically patterned into an array of islands; depending on the mask used one can selectively choose where the III-V material will be placed in general locations on the silicon, with future lithography post-integration allowing for precise alignment of the optical devices to features on the host wafer. Pd (500 Å)/ Ge (1265 Å) is used as the ohmic contact on the back of the III-V islands to maintain CMOS compatibility by avoiding the use of gold. The silicon host wafer is metallized with Ti (500 Å)/ Al (1500 Å), where Ti is used to improve adhesion to the silicon wafer and Al is used for the eutectic attach (Al-Ge) of the III-V islands to the silicon wafer. This layer is also used as an interconnect to the III-V n-side ohmic contact. After integration, BCB 3022-57 is used as the planarization polymer to create a uniform interconnect plane when fabricating the devices into the integrated material.

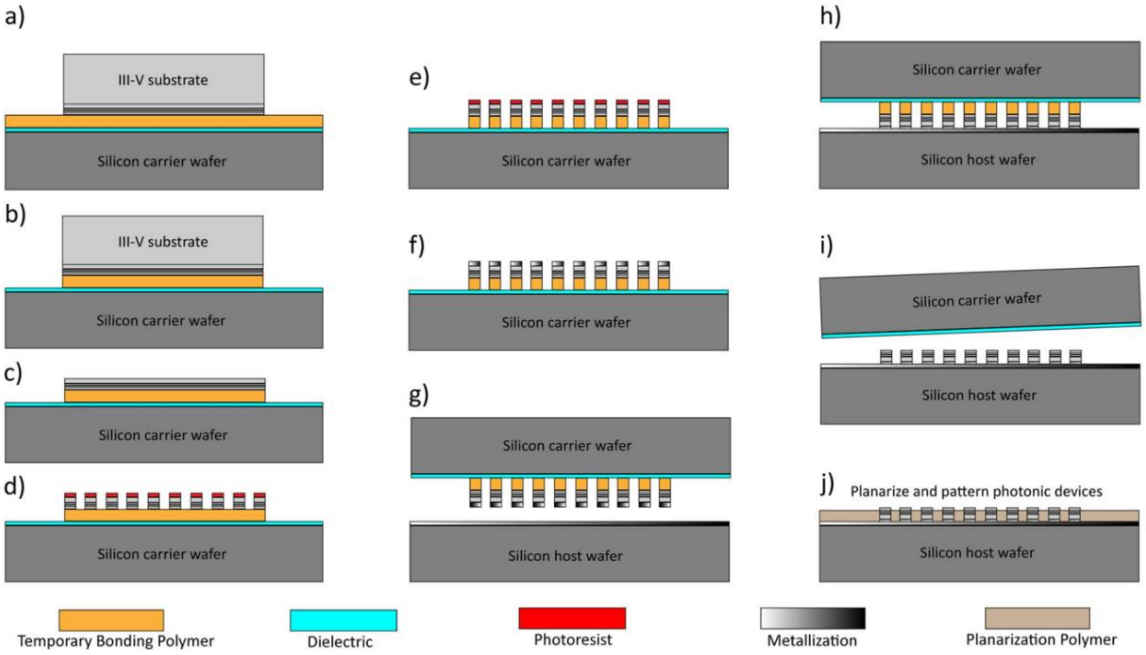

Figure 1. Epitaxial bonding and transfer process diagram. a) III-V epitaxial wafer placed onto bonding polymer, b) excess bonding polymer removed, c) III-V substrate is thinned, d) III-V island array is formed through photolithographic design and etching, e) excess bonding polymer removed between islands, f) ohmic contact deposited on islands, g) III-V islands placed in contact with metallized silicon host wafer, h) eutectic alloy of interface formed, i) carrier wafer and bonding polymer removed, j) epitaxial islands planarized.[1]

2.2 Device fabrication

After the integration of VCSEL material with silicon, 20 µm VCSEL mesas are fabricated into the III-V islands. If required, precise alignment of the VCSEL apertures to existing features such as electronic devices on the silicon host wafer would be performed here. Simple arrays of VCSELs are desired in this case, and the resulting islands are planarized once again using BCB. The 20 µm VCSEL mesas are then oxidized via wet oxidation[6,7] to form 10 µm oxide apertures. Contact to the p-type GaAs top layer is made using a Ti (500 Å)/ Pt (1000 Å)/ Au (1000 Å) stack. Gold is added here to allow testing via wafer probing, but this could be replaced by just Ti/Pt or Ti/W to maintain CMOS

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compatibility. The previously discussed Pd (500 Å)/ Ge (1265 Å) contacts are used for the bottom n-type contact with an Al interconnect. A labeled scanning electron microscope (SEM) micrograph of the integrated VCSEL can be seen below in Figure 2.

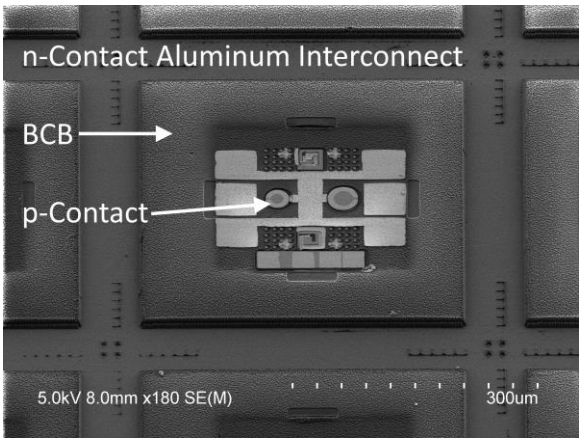

Figure 2. Labeled SEM micrograph of four integrated VCSELs. The dark, textured areas are planar BCB. The broken circle around the emitter is the p-contact, with a 10 µm aperture device on the left and a larger, 20µm device on the right which is not discussed. The lines separating devices are the n-contact interconnects.

2.3 Data collection

The integrated VCSEL is characterized from room temperature (23˚C) to 50˚C using a thermoelectric cooler run in reverse bias to heat the device on a copper stage which is monitored via a temperature controller (LDT-5525). A micro-probe is used to provide current injection to the devices. For optical power measurements, a lensed optical fiber is centered above the lasing device and connected to a calibrated Newport 818-UV photodetector with an OD-3 attenuator. The optical spectra are collected via the same lensed optical fiber directly connected into an optical spectrum analyzer (HP7105A).

3. RESULTS

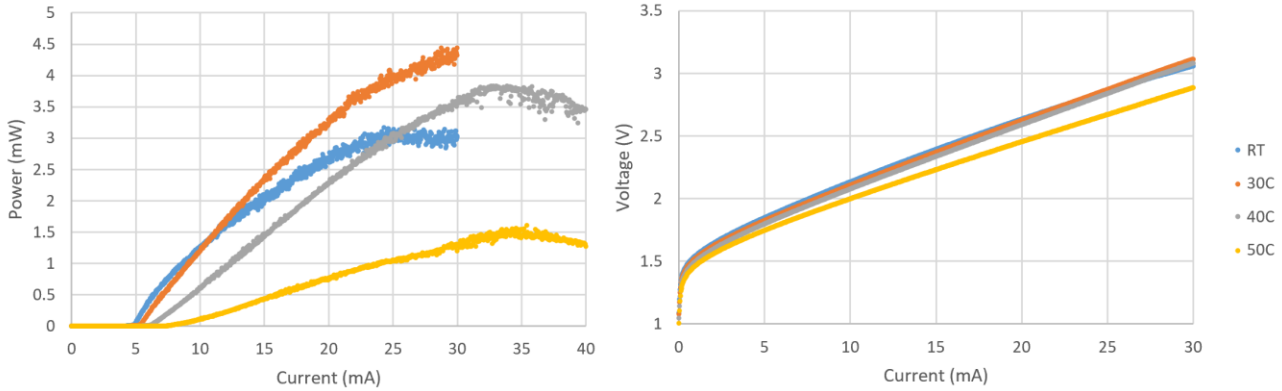

Figure 3. Integrated VCSEL L-I-V for room temperature (RT) to 50˚C. Left: power versus current, right: voltage versus current.

As shown above in Figure 3, the integrated VCSEL has a threshold current of $I_{th} \approx 5$ mA and a maximum power of approximately $P_{max} \approx 3$ mW at room temperature. At 30˚C these characteristics change to $I_{th} \approx 5.5$ mA and $P_{max} \approx 4.5$ mW, at 40˚C $I_{th} \approx 6.3$ mA and $P_{max} \approx 3.8$ mW, and at 50˚C the performance starts to more significantly degrade to $I_{th} \approx 8$ mA and $P_{max} \approx 1.5$ mW. The integrated VCSEL had a lower than typical series resistance of between 30-50 Ω,

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demonstrating a greater than 2x reduction in series resistance compared to the typical values of over 100 Ω of similar as-grown devices.[6]

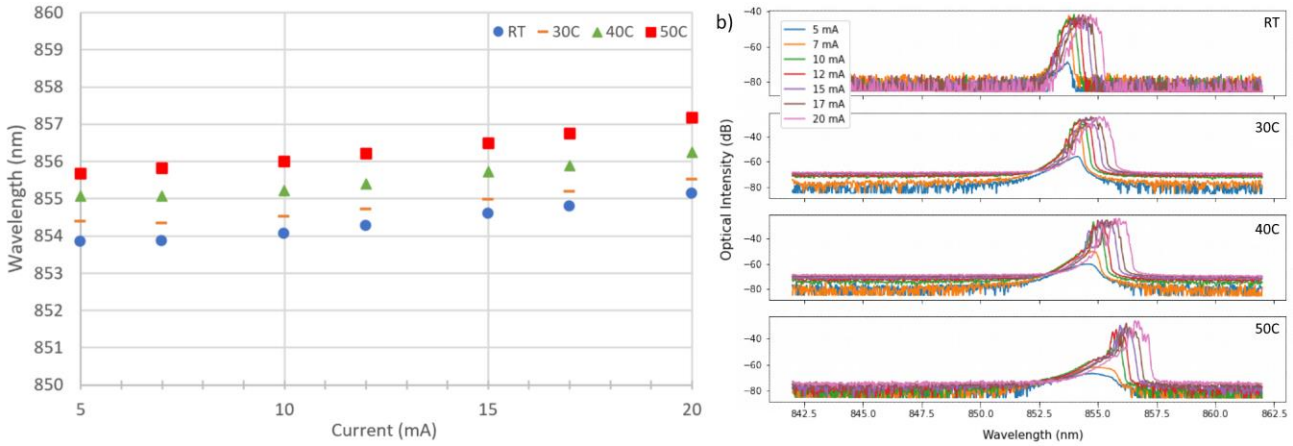

Figure 4 Integrated VCSEL spectral shift for room temperature (RT) to 50˚C. a) Wavelength shift of fundamental mode. b) Spectral data.

As shown above in Figure 4, these integrated VCSELs at threshold have a lasing wavelength of approximately 853.8 nm. At room temperature from 5 to 20 mA the fundamental mode redshift is $\Delta\lambda = 1.3$ nm, at 30˚C it is $\Delta\lambda = 1.1$ nm, at 40˚C it is $\Delta\lambda = 1.2$ nm, and at 50˚C it is $\Delta\lambda = 1.5$ nm. These average to a wavelength redshift of 1.2 nm from 5 to 20 mA for an average redshift of 0.08 nm/mA. These results are summarized below in Figure 5 and are compared to the results of a non-integrated VCSEL with a similarly sized oxide aperture of 10 µm.

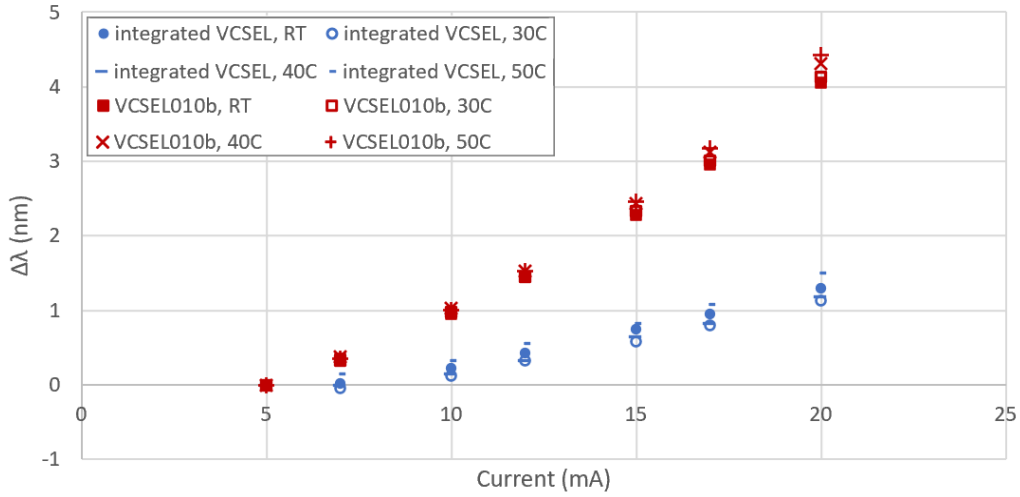

Figure 5. Normalized fundamental mode wavelength redshift of an integrated VCSEL versus a non-integrated VCSEL (VCSEL010b) of similar oxide aperture size from room temperature to 50˚C.

As shown above in Figure 5 the integrated VCSELs has a significantly reduced redshift compared to a non-integrated VCSEL with similarly sized 10 µm oxide apertures. Additionally, this reduced redshift is consistent across operable temperatures. As recorded below in Table 1, the integrated VCSELs have an average redshift of 0.08 nm/mA which demonstrates a greater-than 3x reduction in thermal shift compared to the typical greater-than 0.27 nm/mA for similarly sized non-integrated devices[8] and a greater-than 5x reduction in thermal shift compared to the typical greater-than 0.45 nm/mA for similarly sized flip-chip integrated devices.[9,10] As 0.06-0.08 nm/˚C is the typical redshift associated with pure temperature changes,[11] this is a significant difference. This can also be used to estimate junction temperature rise. The

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decreased redshift of heterogeneously integrated VCSELs is likely due to an improved thermal path provided by the silicon allowing enhanced heat dissipation of the otherwise uncooled VCSEL. Many flip-chip VCSELs have found increased redshifting of their integrated devices compared to non-integrated counterparts due to the bonding compromising the thermal conductivity,[12] an effect evidently not found in this heterogeneously integrated device. The enhanced wavelength stability is greatly beneficial for a variety of systems such as wavelength dependent optics, coarse wavelength division multiplexing (CWDM) for high-speed data transmission,[13] and sensing systems requiring CMOS cameras.[14]

Table 1. Room temperature redshift of 10 μm oxide aperture VCSELs across multiple integration types, displaying ratio of each method's redshift to that of the heterogenous integration method.

Methodology	Redshift	Ratio to Heterogeneous Integration
Heterogeneous Integration	0.08 nm/mA	1:1
Flip-Chip Integration	0.66 nm/mA[9]	8.3:1
Flip-Chip Integration	0.45 nm/mA[10]	5.6:1
No Integration	0.27 nm/mA	3.4:1
No Integration	0.58 nm/mA[8]	7.3:1

4. CONCLUSIONS

We successfully demonstrated heterogeneous integration of GaAs VCSELs onto silicon. Unlike prior work, fabrication of the VCSELs takes place on the silicon host wafer after the epitaxial transfer process. The resulting integrated devices show significantly reduced red-shifting of the emission wavelength with increasing current and reduced power dissipation due to a lower series resistance when compared with as-grown devices of similar oxide aperture size, indicating heterogeneously integrated VCSEL devices have an improved thermal environment when compared with their non-integrated counterparts. This improved performance is additionally consistent across increased temperatures and when compared with flip-chip bonded VCSELs. The observed advancement to wavelength stability found with heterogeneously integrated VCSELs indicates a potential application for integration beyond the typical desire for seamless electronic-photonic systems, as improved wavelength stability is a significant development unto itself for a variety of applications including wavelength dependent optics, coarse wavelength division multiplexing (CWDM),[13] and sensing systems requiring CMOS cameras.[14] Devices formed through the same process with smaller apertures and reduced substrate thickness are expected to further improve performance with a smaller aperture contributing to lower threshold current and reduced red-shifting while decreased substrate thickness improves thermal pathways.

5. ACKNOWLEDGEMENTS

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