Heterogeneous Integration of Light-Emitting Transistors on Silicon for Hybrid Electronic-Photonic Logic Circuitry

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Abstract: An array of heterogeneously integrated light-emitting transistors is fabricated after an epitaxial transfer process bonds and interconnects active III-V photonic material onto a CMOS-compatible host wafer for the purposes of establishing a photonic logic network.

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1. Introduction

The desire to extend optical communications to the chip-scale has created opportunities to integrate devices that can directly interact between electronic and photonic domains, augmenting CMOS-based circuits with speed and energy savings. Current approaches are limited to using two-terminal photonic devices to couple light into silicon waveguide structures [1], but new designs in three-terminal photonics allow for devices to interact in both the electrical and optical domain [2]. These light-emitting transistors (LETs) allow for fundamentally broader access to electronic systems as one LET is able to transmit both electrical and optical signals, making it ideal for integration.

The means to heterogeneously integrate three-terminal photonic materials onto silicon has been demonstrated by epitaxial bonding and transfer processes [3], and here integrated LETs are fabricated directly into transferred III-V epitaxial material. The design and analysis of heterogeneously integrated LETs is presented, shown as a step toward forming active components in a photonic logic system. By integrating directly to a CMOS host wafer with electrical and thermal contact, hybrid electronic-photonic circuitry can be formed where LETs perform new functionalities [4], with potentially improved bandwidth over monolithic designs.

2. Experimental Setup and Results

An array of III-V epitaxial material optimized for LET devices is first heterogeneously integrated to silicon by an epitaxial bonding and transfer process. These processes conclude by establishing a permanent metal-eutectic alloy between a silicon host wafer (CMOS) and the collector terminal (n-GaAs) of LET epitaxial material, creating an interconnect layer to the photonic material that allows for good electrical and thermal conductivity to resulting devices [3]. The benefit of proceeding with device fabrication after material integration is that this eliminates the need for discrete device alignment and allows for photolithographic definition of LETs into the material in unison. The resulting integrated material after transfer and planarization is shown in Figure 1, where a confocal three-dimensional optical profile is shown to confirm that the resulting III-V islands have good flatness and maintain their spatial arrangement before LET fabrication. The emitter terminal of each III-V island is upward following transfer while the collector terminal is embedded underneath, so an opening to the interconnect layer is required for testing.

The distribution of III-V islands are patterned to form LET devices from the integrated material in unison. The material structure consists of a graded n-GaAs emitter cap, n-InGaP emitter, p-GaAs base, i-InGaAs quantum well (λ_0=980 nm), p-AlGaAs barrier, and an n-GaAs collector. To maintain CMOS-compatibility, a metallization strategy is chosen such that gold-free contacts are established for each terminal of the LETs, utilizing the same n-GaAs for the emitter as used in integration (Pd(500 Å)/Ge(1265 Å)) and employing a p-GaAs contact (Ni(50 Å)/Ti (50 Å)/Pt (50 Å)/Ti (300 Å)/Pt (1000 Å)) for the base that together act as Ohmic contacts for integrated LET material [3].

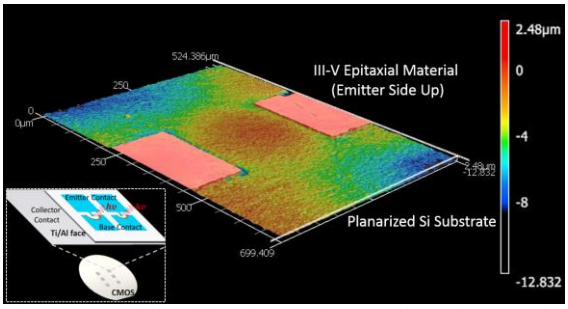

Figure 1. Optical profile of integrated photonic material on silicon host wafer. Inset shows diagram of photonic devices in integrated material.

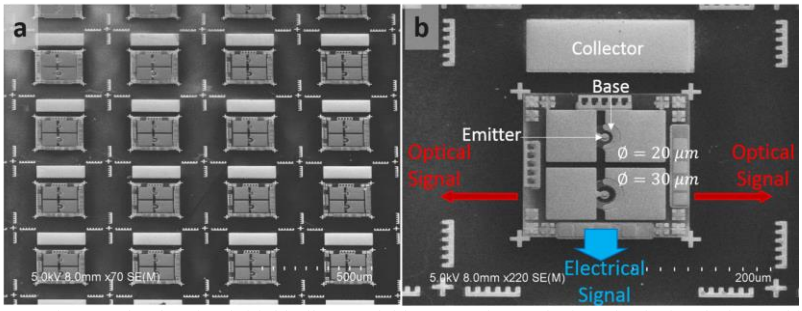

Figure 2. Scanning electron micrographs showing initial bulk a) scalable array of LET devices, b) device design and its signal interconnects.

A series of dry-etch processes (BCl_3, Cl_2) are utilized to establish a set of two emitter mesas into each of the aligned III-V islands, stopping at the base. Metal contacts as described above are then E-beam evaporated and annealed onto the material, defining two LETs with base metal diameters of 20 and 30 μm. A second planarization step isolates the contacts, while a dry etch (SF_6) open up the planarization polymer to the interconnect layer for collector probing. A set of bulk LET devices are fabricated alongside the integrated III-V material so as to verify the fabrication process and ensure optimal parameters. The final array of LET devices is shown in Figure 2, where a close-up in Figure 2b shows the resulting electrical and optical planes inherent to the single device.

The band structures for each integrated LET are then simulated to establish baseline values for the drive voltages required to operate each LET. A non-equilibrium Green's function (NEGF) solver is utilized to produce a self-consistent solution to the emitter-base and base-collector junctions [5] of the LET epitaxial structures, using applied biases expected of an electronic-photonic circuit. In Figure 3, the emitter-base junction is simulated at 0.5, 0.6, and 0.8 V of forward bias for values typical of an LET operating in current injection mode, while the base-collector junction is simulated at reverse biases of -1, -2, and -5 V so as to show the suitability of the integrated devices for light emission or for light detection ($\lambda_0 = 980$ nm = 1.26 eV) via photon-assisted tunneling [4], enabling the intended hybrid electronic-photonic circuits. Preliminary data showing the corresponding diode curves on the bulk LETs are shown in the inset, while testing is ongoing to test transistor family curves and spectra of the integrated LETs.

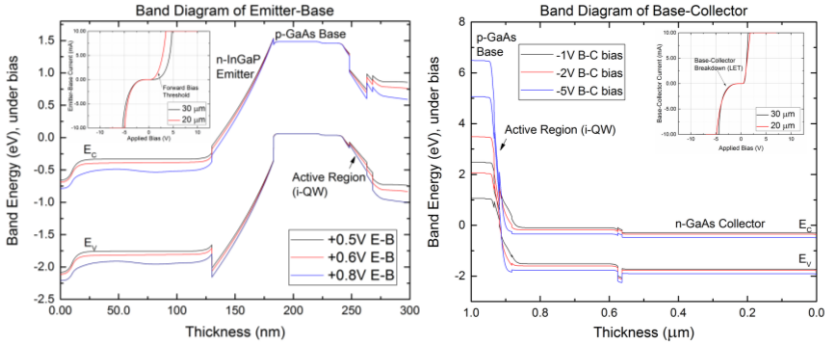

Figure 3. Calculation of the structures of the integrated LET under bias conditions. Inset images show preliminary results of diode curves.

3. Conclusion

An array of three-terminal LETs is designed and fabricated into heterogeneously integrated epitaxial material for the purposes of establishing hybrid electronic-photonic circuitry. Monolithically-integrated LETs are characterized to compare the performance of integrated devices in verifying the integration process, as well as the device structure of the integrated LET is analyzed for performance optimization. This work is sponsored in part by E2CDA-NRI, a funded center of NRI, a Semiconductor Research Corporation (SRC) program sponsored by NERC and NIST, and in part by the National Science Foundation (NSF) under Grant No. ECCS 16-40196.

4. References

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