Analytical Bit-Error Model of NAND Flash Memories for Dosimetry Application

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***Abstract*— In this article, we provide an analytical model for the total ionizing dose (TID) effects on the bit error statistics of commercial flash memory chips. We have validated the model with experimental data collected by irradiating several commercial NAND flash memory chips from different technology nodes. We find that our analytical model can project bit errors at higher TID values [∼20 krad (Si)] from measured data at lower TID values [≪1 krad (Si)]. Based on our model and the measured data, we have formulated basic design rules for using a commercial flash memory chip as a dosimeter. We discuss the impact of NAND chip-to-chip variability, noise margin, and the intrinsic errors on the dosimeter design using detailed experimentation.**

***Index Terms*— 3-D NAND, ionizing radiation, multi-level-cell, read retry.**

I. Introduction

SILICON dosimeters based on metal-oxide-semiconductor field effect transistor (MOSFET) structures are promising candidates for dosimetry applications [1]–[7]. More specifically, floating-gate MOSFET structure has recently gained significant attention for dosimetry application as it offers wireless and passive modes of operation [8]–[13]. Tarr *et al.* [10] demonstrated a floating-gate MOSFET dosimeter using a complementary metal oxide semiconductor (CMOS) compatible fabrication process. They measured the change in threshold voltage of the fabricated floating-gate MOSFET as a function of the absorbed dose. Their measurement showed sensitivity of 0.7 mV/rad. A similar floating-gate MOSFET device structure was later used with an ON-chip signal processing circuit to measure radiation dose in terms of output frequency by Brucoli *et al.* [12], [13]. Scheick *et al.* [8] demonstrated dosimetry concept based on erasure of floating gate memory arrays using commercially available ultraviolet erasable programable read only memory (UVPROM) chips. The same concept was later refined by McNulty *et al.* [14], [15] to improve the resolution and dynamic range of the dosimeter. Recently, Chatterjee *et al.* [11] demonstrated monolithically integrated wearable CMOS radiation dosimeter, which consists of a floating-gate resistive sensor with a sensitivity of 14 Ω/rad. Thus, there remains a continued interest in using floating gate MOSFET devices for possible dosimetry applications.

Since commercial off-the-shelf (COTS) NAND flash memories are made of floating gate MOSFET arrays, they provide a viable and interesting option for dosimeter design. In addition, NAND flash memories provide a few unique advantages for dosimeter design compared with many existing dosimetry solutions. For example, flash memory is ubiquitous in many sensor nodes and Internet of Things (IoT) applications, and hence flash-based dosimetry solutions can be ideal for low-cost, large-scale deployment of dosimeters through existing IoT devices without any hardware modification. Similarly, a part of flash memory can be used as an ON-chip dosimeter in electronic platforms for total ionizing dose (TID) compensation or hardware protection purposes resulting in improved system performance.

Savage *et al.* [16] first proposed the use of NAND flash memories for dosimetry applications. They utilized target theory to predict the occurrence of the first failure in a single-level-cell (SLC) NAND flash memory chip of 42-nm technology node. Through experimental evaluation they concluded that the TID sensitivity of the SLC NAND chip is 38 krad (Si). Since NAND flash memory is a rapidly evolving technology, several advances took place over the last decade, including the multi-level-cell (MLC) storage making it very sensitive to low TID values. For example, Kumari *et al.* [17] recently demonstrated that MLC NAND flash memory of 20-nm technology is sensitive to TID ∼100 rad (Si). Similarly, Bagatin *et al.* [18] demonstrated possible use of commercial 3-D NAND flash technology for high-energy particle detection. Thus, state-of-the-art NAND flash memory offers several interesting features that can be utilized for dosimetry applications.

Even though radiation effects on commercial NAND flash memories have been extensively studied in the last decade, there is no analytical bit error model that physically captures the TID effects on the floating-gate memory arrays. Such a model is essential in order to calculate the absorbed dose from the TID-induced bit error response. In addition, commercial NAND flash memories present several practical challenges for achieving high sensitivity and accuracy of the

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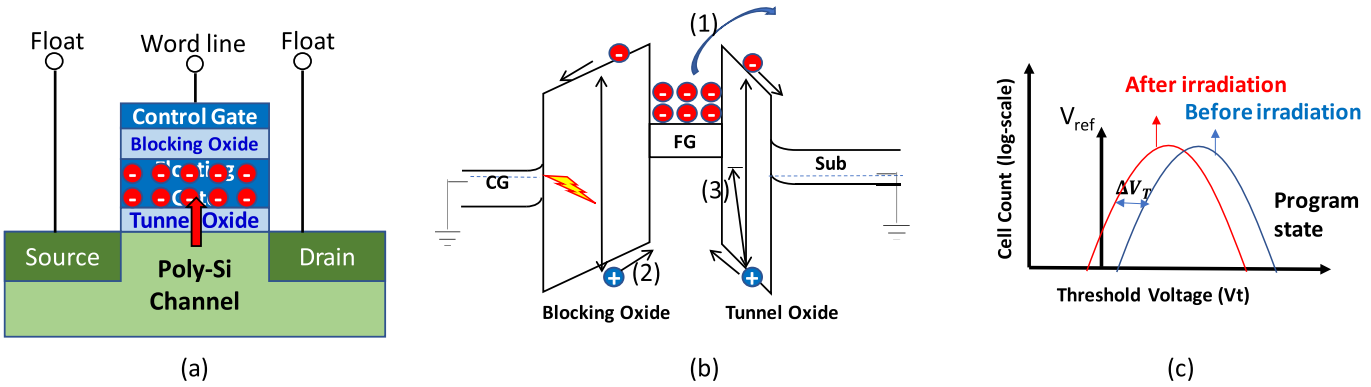

Fig. 1. (a) Schematic of a floating gate flash memory cell. (b) Energy band diagram of a programed cell with all pins grounded, showing different pathways of charge loss: 1) thermionic emission from the FG; 2) electron–hole recombination; and (3) hole trapping in the oxide. (c) Threshold voltage (V_t) distribution of the programed memory cells before and after radiation exposure.

dosimeter. For example, the read-out process of commercial flash chips comes with higher noise-margins, which prevents achieving high TID sensitivity. Second, the manufacturing process variation is significant in the commercial flash memory chips causing large variation in the radiation response (both intra-chip and inter-chip). Third, high density flash chips are susceptible to intrinsic bit errors due to charge leakage and read-noise. Thus, it is important to evaluate the impact of these challenges on the sensitivity and accuracy of the NAND-based dosimeter.

In this article, we provide a theoretical framework to understand the sensitivity and accuracy of flash memory-based dosimeters. We have provided an analytical model to understand the TID response on the bit-error statistics of the commercial NAND flash memory and formulated the basic design rules for using the commercial chips as dosimeters. We performed irradiation experiments on several commercial NAND flash memory chips from different technology nodes to evaluate the proposed model and its limitations. In addition, after performing experimental evaluation on the impact of NAND variability, intrinsic bit error issues, and noise-margin on dosimeter design, we propose corresponding countermeasures.

II. Model System

The device structure of a floating-gate flash memory cell is shown in Fig. 1(a). A flash memory cell is essentially a MOSFET with an extra conducting layer called a floating gate (FG) embedded inside the gate insulator. The bottom insulator in Fig. 1(a) is called tunnel oxide, typically made of SiO_2. The top insulator is called blocking oxide and is made of oxide–nitride–oxide (ONO) layers. The floating gate is commonly made of polysilicon, which retains the charge (electrons) for a long time even in the absence of any voltage on the control gate. Thus, information is stored in the form of electronic charges on the floating gate. If charge is present in the floating-gate, the cell is in the programed state, represented by bit "0," while the absence of electrons means that the cell is in the erased state, represented by bit "1."

Fig. 1(b) shows the energy band diagram of a flash memory cell in the programed state with all pins grounded. Exposure to ionizing radiation creates electron-hole pairs in the insulating oxide layers [19]. Due to the oxide electric field, the electrons will escape the oxide layers and the holes will either get trapped in the oxide or drift toward the floating-gate and recombine with stored electrons. Thus, there is no escape path for the radiation-induced holes meaning there will be an effective charge loss for every generated hole in the oxide layers of the flash memory cell. In other words, flash cell will lose charge cumulatively with the absorbed TID. Please note that the direction of hole movement might be different for erased memory cells in the absence of electrons on the floating gate. In this work, however, we focus only on programed cells for the dosimetry application. Fig. 1(c) shows the simplified cell threshold voltage (V_t) distribution with only one logical V_t-state. Even though all the cells are programed to the same logical state, there is significant cell-to-cell V_t variation as illustrated with Gaussian-like distribution in Fig. 1(c). Usually a fixed read reference voltage, V_{ref}, is used to digitize the analog cell V_t into its corresponding logic state. For example, cells with $V_t > V_{\text{ref}}$ are read as logic-0 and cells with $V_t < V_{\text{ref}}$ are read as logic-1. The lowering of cell V_t will cause 0-to-1 bit flips on the stored data.

The amount of charge loss from a flash cell can be measured in terms of ΔV_t, using the following:

$$\Delta V_t = \frac{\Delta Q_{\text{FG}}}{C_{\text{ONO}}}. \tag{1}$$

Here ΔQ_{FG} is the radiation-induced charge loss from the memory cell and C_{ONO} is the capacitance of the blocking insulator which is typically made of ONO layers. Neglecting the sidewall capacitances, the ONO capacitance can be modeled assuming parallel plate capacitor equation, $C_{\text{ONO}} = ((\epsilon_{\text{ONO}} A)/t_{\text{ONO}})$, where A is the gate area, t_{ONO} is the thickness of the ONO layer, and ϵ_{ONO} is the effective dielectric constant. Since the amount of charge loss is proportional to the absorbed dose and the volume of the insulating layers, we can write

$$\Delta Q_{\text{FG}} \propto \text{TID} \times A \times (t_{\text{OX}} + t_{\text{ONO}}) \tag{2}$$

where t_{OX} is the thickness of the tunnel oxide layer.

Using (1) and (2), we can write the TID-dependent V_t-lowering relationship as follows:

$$\Delta V_t \propto \frac{\text{TID} \times (t_{\text{OX}} + t_{\text{ONO}}) t_{\text{ONO}}}{\epsilon_{\text{ONO}}}. \quad (3)$$

Equation (3) can be simplified further if we assume a fixed ratio between t_{OX} and t_{ONO} which is typically called the coupling ratio in the design of commercial flash memories. Assuming a fixed ratio between t_{OX} and t_{ONO}, (3) indicates that $\Delta V_t \propto \text{TID} \times t_{\text{OX}}^2$. This is a well-known relationship for negative threshold voltage shift originally derived for CMOS logic technologies [20]. Equation (3) has several important implications on the sensitivity of the flash memory-based dosimeter as follows.

1) The sensitivity of the flash memory-based dosimeter is independent of the gate area. The gate area usually shrinks from the older technology node to the newer technology node; however, (3) suggests that such shrinking of the gate area will not have any significant impact on the sensitivity of the flash-based dosimeter design.
2) The sensitivity of the flash memory-based dosimeter is strongly dependent on oxide layer thickness. Unlike CMOS logic transistors, oxide thickness did not scale for the flash memory technology due to data retention considerations. Hence, contrary to CMOS logic, flash memory did not improve in TID sensitivity across different technology nodes. Previous research indicates that flash memory technology remains sensitive to moderate TID values [∼50 krad (Si)] even with ultra-small sub-20 nm technology nodes [21].
3) Equation (3) suggests linear response for ΔV_t for increasing TID. The linear response is another desirable property for designing a good dosimeter.

Even though (3) captures the essential physics for flash memory-based dosimeters, it does not capture several practical design considerations related to high-density flash memory arrays. We explain the practical design considerations of flash memory-based dosimeters with more details in Sections III and IV.

III. Device and Experimental Details

A. Device Details

We used several COTS 2-D and 3-D MLC NAND, flash memory chips from Micron Technology for all our tests. Details of the chip's organization are given in Table I.

B. Gamma-Ray Irradiation

The radiation exposure of the flash chips was conducted at the Sandia National Laboratories Gamma Irradiation Facility. A Co-60 source at a dose rate of 18.6 rad (Si)/s was used for the exposure. If not otherwise stated, all doses in the following are expressed as the absorbed dose in silicon. Gamma exposure was performed on the packaged thin small outline package (TSOP) devices with all pins grounded. The direction of gamma rays during exposure was perpendicular to the top surface of the chip and the entire chip in unlidded condition was exposed to gamma irradiation.

TABLE I
Details of the Device Used

Chip ID	Tech. node	Chip size	Page size	Pages per block
MT29F32G08CBADAWP	20 nm	32Gb	8kB	256
MT29F64G08CBAAAWP	28 nm	64Gb	8kB	256
MT29F32G08CBACAWP	34 nm	32Gb	8kB	256
MT29F16G08CBACAWP	25 nm	16Gb	8kB	256
MT29F256G08CBCBB WP	32 layers (3D)	256Gb	16kB	1024

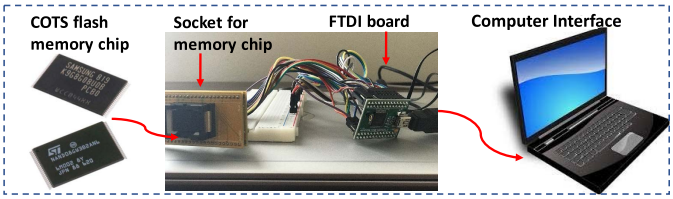

Fig. 2. Our measurement set-up to interface commercial flash memory chip with computer.

To interface the NAND chip with computer we have used a custom-designed hardware board as shown in Fig. 2. There is a socket to place the NAND flash chip and an FT2232H mini-module to interface the chip with a computer through universal serial bus (USB) connection. The hardware setup allows us to calculate raw bit error. All error correction codes (ECCs) were bypassed during the data collection. The hardware set up was not irradiated and was used to write/read the memory chips that were irradiated separately. Before exposing chips to radiation, we wrote an all-zero data pattern on at least ten memory blocks in each chip. We read all the blocks immediately after writing data, to get the initial bit error values. Few bit errors are usually observed just after write operation in MLC memory, which has very low voltage margin between different memory states. We then exposed the NAND memory chips to the Co-60 source and readback the data from the corresponding memory blocks within an hour after irradiation.

IV. Design Considerations for Flash-Dosimeter

In the following, we discuss the design considerations for building a COTS flash memory-based dosimeter with high sensitivity and accuracy.

A. Fail Bit Count With TID

Fail bit count (FBC) is a readily measurable quantity from the COTS flash memories using digital interfaces. Hence estimating TID from measured FBC is a key step for using the flash chip as a dosimeter. However, the functional dependence of FBC with TID is not straightforward as it depends on several factors, such as the initial cell V_t distribution, the amount of TID-induced average V_t shift and the associated cell-to-cell variability. Fig. 3(a) illustrates the mathematical relation between FBC and cell V_t distribution. It has been shown that the cell V_t in NAND array follows a Gaussian distribution with mean μ_{V_t} and standard deviation σ_{V_t} [22]. The exact values for the μ_{V_t}, and σ_{V_t} are technology-dependent,

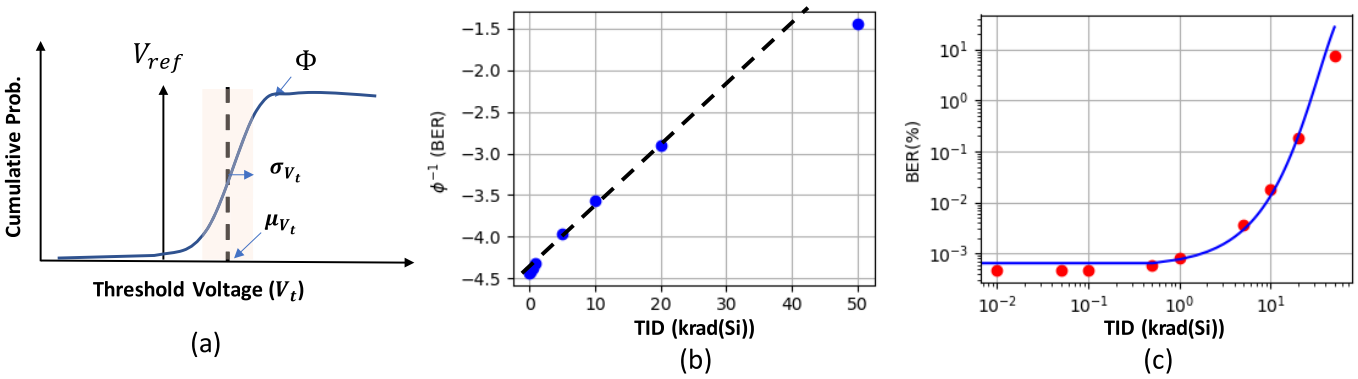

Fig. 3. (a) Illustration of the cumulative distribution function (Φ) of the standard Gaussian distribution for cell V_t with distribution mean μ_{V_t} and variance $\sigma^2_{V_t}$. (b) Measured Φ^{-1}(BER) as a function of TID for 32-layer 3-D NAND. Symbols are measured data and the dashed line is the linear fit. (c) BER dependence on TID calculated by (7) and the measured data in log-log scale for 32-layer 3-D NAND. The solid line represents the model, and the symbols are from the experimental data.

proprietary parameters. Since FBC includes the memory cells whose V_t is below the read reference voltage (V_{ref}), it can be modeled using the cumulative distribution function (Φ) of the standard Gaussian distribution [22] as follows:

$$\text{FBC} = N_{\text{bits}} \times \Phi\left(\frac{V_{\text{ref}} - \mu_{V_t}}{\sigma_{V_t}}\right). \tag{4}$$

Here N_{bits} represents the total number of bits in a memory page that are programed to a given program state. The FBC increase with V_t-downshift can be modeled as follows:

$$\text{FBC}(\Delta V_t) = N_{\text{bits}} \times \Phi\left(\frac{V_{\text{ref}} - \mu_{V_t} + \Delta V_t}{\sigma_{V_t}}\right). \tag{5}$$

The above equation assumes that σ_{V_t} remains unchanged after irradiation, which is an approximation. In practice, σ_{V_t} will increase with higher ΔV_t, however, for small ΔV_t the increase in σ_{V_t} can be ignored. Since $\Delta V_t \propto$ TID according to (3), we can express the above equation in terms of TID as follows:

$$\text{FBC}(\text{TID}) = N_{\text{bits}} \times \Phi\left(\frac{V_{\text{ref}} - \mu_{V_t} + \alpha(\text{TID})}{\sigma_{V_t}}\right). \tag{6}$$

Here, α is a technology-dependent fixed parameter that characterizes the TID-induced linear V_t shift. Equation (6) can be further simplified as follows:

$$\text{BER} = \frac{\text{FBC}}{N_{\text{bits}}} = \Phi\left(\frac{V_{\text{ref}} - \mu_{V_t} + \alpha(\text{TID})}{\sigma_{V_t}}\right). \tag{7}$$

Here BER is called bit error ratio or percentage of error bits in the memory page. The model parameters in (7) can be estimated from the measured BER as a function of TID using the following:

$$\frac{V_{\text{ref}} - \mu_{V_t}}{\sigma_{V_t}} + \frac{\alpha}{\sigma_{V_t}}(\text{TID}) = \Phi^{-1}(\text{BER}). \tag{8}$$

Equation (8) is a linear equation with TID having the slope of (α/σ_{V_t}) and the intercept value of $((V_{\text{ref}} - \mu_{V_t})/\sigma_{V_t})$. We plot the measured Φ^{-1}(BER) values as a function of TID to estimate the model parameters as shown in Fig. 3(b). Using the estimated model parameters, we calculate BER as a function of TID which is plotted in Fig. 3(c). The solid line in the plot represents the model [see (7)] and the symbols represents the measured data. We used $((V_{\text{ref}} - \mu_{V_t})/\sigma_{V_t}) = -4.4$ and $\alpha/\sigma_{V_t} = 0.076$/krad in (7) to fit the experimental data. Please note that σ_{V_t} and $(V_{\text{ref}} - \mu_{V_t})$ are technology-dependent fixed parameters and the NAND manufacturers usually optimize these parameters to ensure reliability. However, these parameters are not publicly disclosed and hence they need to be extracted from experimental data. Note that the pre-characterization step involves exposing the chip to moderate TID [∼1–5 krad (Si)], which is low enough to cause any peripheral device damage in the chip [23]. All the model parameters need to be pre-characterized for a given chip before using it for dosimetry application.

The proposed model has certain limitations. For example, its accuracy degrades for high TID values [∼50 krad (Si)] as shown in Fig. 3(c). Note that the model derivation [see (7)] considers only V_t distribution shift by changing the mean of the distribution as a function of TID. In practice, the cell V_t distribution gradually widens with TID. Since the model does not account for V_t distribution widening effect which is important at higher TID, the model fails to accurately calculate BER at higher TID. If the σ_{V_t} in (7) is considered as a function of TID, the model can be extended for calculating BER at higher TID values. In addition, the model does not include device noise effects which impact its accuracy. Nevertheless, we find a close agreement between measured data and the BER model for TID in the range of 1–20 krad (Si). Finally, (7) does not include the effects of retention errors, which is another important factor contributing to BER. We discuss the effects of retention errors in Section IV-C.

B. Chip-to-Chip Variation

NAND flash memory chips exhibit a significant chip-to-chip manufacturing variation [24]. Chip-to-chip variation was reflected in terms of different BER growth during irradiation for three 3-D NAND memory chips with the same part number in Fig. 4(a). Chip-to-chip BER variation is evident in the plot, but our modeling approach takes into account this chip-to-chip BER variation by introducing chip-dependent model parameters and hence it accurately calculates the BER for all

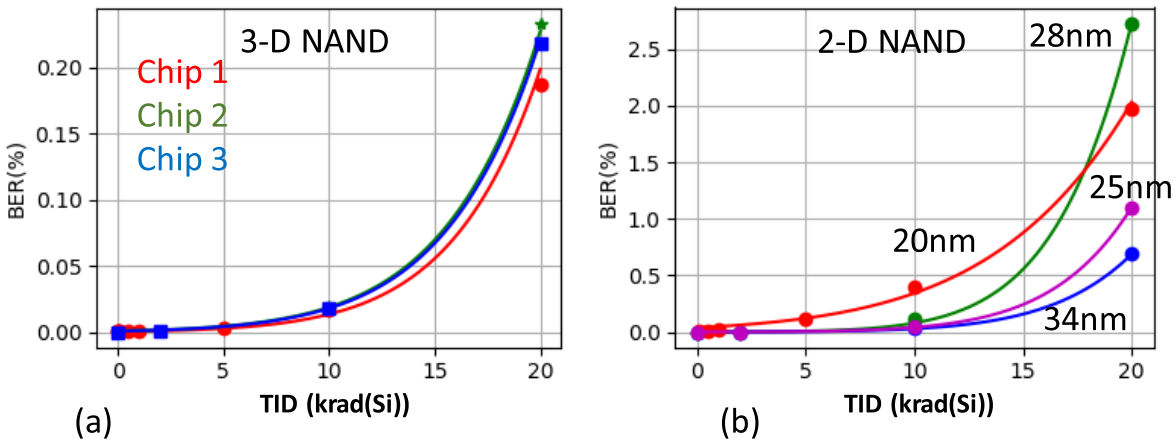

Fig. 4. (a) Cumulative BER with TID for three identical 32-layer 3-D NAND chips. Solid lines represent model [see (7)] and the symbols correspond to measured data. (b) Cumulative BER with TID for four 2-D NAND chips from different technology nodes (34, 28, 25, and 20 nm) calculated by the model (7) (solid line) and verified by measured data (symbols).

TABLE II
SUMMARY OF EXTRACTED MODEL PARAMETERS

Chip	Tech. node	$\frac{V_{ref}-\mu_{V_t}}{\sigma_{V_t}}$	$\frac{\alpha}{\sigma_{V_t}}$
3D 1	32 layers	-4.40	0.076
3D 2	32 layers	-4.26	0.072
3D 3	32 layers	-4.28	0.072
2D 1	20 nm	-3.32	0.071
2D 2	34 nm	-4.41	0.098
2D 3	28 nm	-4.39	0.120
2D 4	25 nm	-4.36	0.104

three chips. Table II summarizes the model parameters used for different memory chips.

Next, we plot the cumulative BER with TID for four different 2-D NAND chips from different technology nodes as shown in Fig. 4(b). The chips from different technology nodes will be different in terms of cell geometry and underlying materials used during fabrication, but our results show that the same model can be used to calculate the BER dependence on TID with an appropriate choice of model parameters. We would like to emphasize that the model parameters such as mean and standard deviation of the cell V_t distribution are extracted from measured data because they are not publicly disclosed for a given chip or technology node. However, chip manufacturers may disclose these values for the commercial use of flash-based dosimeter design. In addition, flash manufacturer may provide a few additional NAND commands for the V_t distribution measurement to extract these parameters at the user end. The model parameter extraction will be very straightforward with the help of chip manufacturers.

C. Intrinsic Errors–Should Be Subtracted for Accurate Radiation Dose Value

High-density MLC NAND flash memory shows intrinsic bit errors which monotonically increase over time. Several charge-loss mechanisms are fundamental to the floating-gate

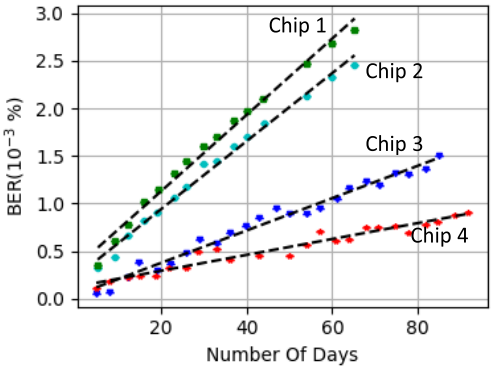

Fig. 5. Intrinsic BER with time in NAND flash memory. Data are collected from four identical 2-D NAND chips of 20 nm node.

structure, which eventually lead to cumulative bit errors at room temperature. For example, the tunnel oxide of the state-of-the-art NAND technology is thin (~6–8 nm), and hence stored electronic charge from the floating gate gradually leaks out through trap-assisted tunneling mechanism. Other prominent charge loss mechanisms include de-trapping of tunnel oxide and thermionic emission. Due to these intrinsic charge loss pathways, the programed V_t of flash memory cells gradually decreases with time causing bit errors. This type of error is known as an intrinsic error.

Intrinsic bit errors are usually corrected by standard error correction codes (ECCs) in the NAND controller. However, for dosimetry applications, the intrinsic bit errors of NAND flash memory need to be properly accounted for to achieve high accuracy of the dosimeter. In this work, we characterized the intrinsic fails of 2-D NAND memory chips for a duration of ~90 days. Fig. 5 summarizes the intrinsic fails from four different chips with identical specification. We wrote all-zero data pattern on at least 100 different memory blocks in each chip and monitor the BER in each chip as a function of time. Following are the key observations from the data.

The cumulative intrinsic errors after 90 days are significant and cannot be neglected when memory chips are used for dosimetry applications for a long duration. The maximum

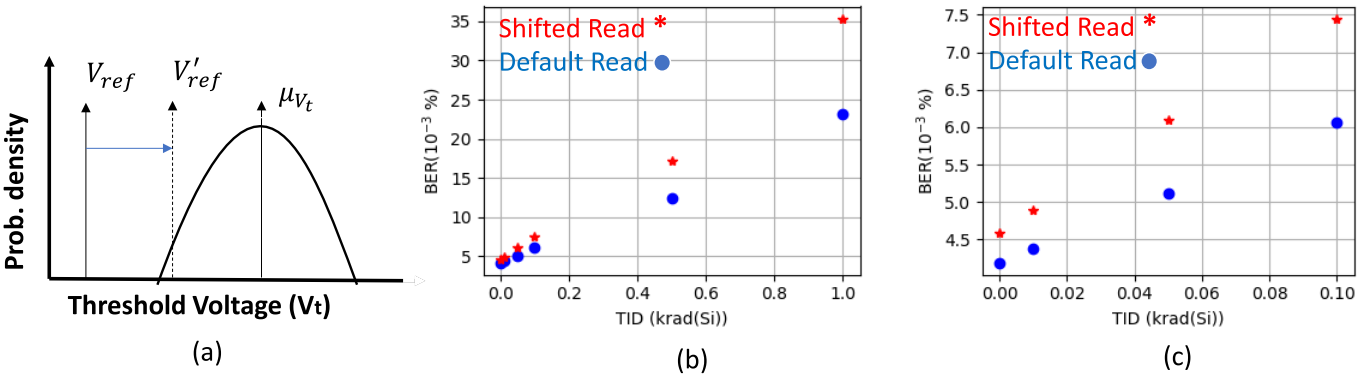

Fig. 6. (a) Representation of read–retry technique. (b) Default read and read retry after radiation is shown for different doses up to 1 krad for 2-D NAND chips of 20 nm node (Si). (c) Default read and read retry after radiation is shown for different dose up to 100 rad (Si) for 2-D NAND chips of 20 nm node.

intrinsic BER after 90 days is ∼0.003% which is equivalent to the BER caused by TID ∼50 rad (Si). Thus, for low-dose measurement, intrinsic errors need to be subtracted from the total errors, which is discussed in the following paragraphs.

The intrinsic errors vary significantly on different memory chips mainly due to chip-to-chip process variations.

Intrinsic bit errors increase linearly with time for all the chips tested in the work.

The above observations suggest that the average intrinsic errors (BER^{int}) in a chip can be approximately modeled using a linear equation with time as follows:

$$\text{BER}^{\text{int}}(t) = \text{BER}_0 + S^{\text{int}} \times t. \tag{9}$$

Here BER_0 is the bit error ratio at time zero or just after data write and S^{int} is the slope related to the increase in intrinsic BER with time. BER_0 is a readily measurable quantity by performing a read operation on a memory chip but the S^{int} needs to be pre-characterized for each memory chip. During dosimetry application, the intrinsic BER needs to be subtracted from the total BER ($\text{BER}^{\text{total}}$) using the intrinsic BER model as follows:

$$\text{BER}^{\text{total}}(t, \text{TID}) - \text{BER}^{\text{int}}(t) = \Phi\left(\frac{V_{\text{ref}} - \mu_{V_t} + \alpha(\text{TID})}{\sigma_{V_t}}\right). \tag{10}$$

Here $\text{BER}^{\text{total}}$ is the measured BER from the dosimeter chip and includes the effects of TID as well as intrinsic charge loss with time. In general, the time evolution of bit error in the flash cells originates from several factors including charge loss by tunneling, de-trapping of the oxide layers, and the hole movement in the oxide layer. The effects of time evolution on the bit error need to be properly accounted for accurate dose estimation [7].

D. Reducing V_t-Margin for Increased TID Sensitivity

To ensure reliable reading of memory states, flash manufacturers keep sufficient V_t margin between the read reference voltage, V_{ref} and the mean value of cell V_t. Fig. 6(a) explains this concept using a simplified cell V_t distribution plot. Mathematically, V_t margin is defined by the value of $|V_{\text{ref}} - \mu_{V_t}|$. When the TID-induced cell V_t shift is large enough

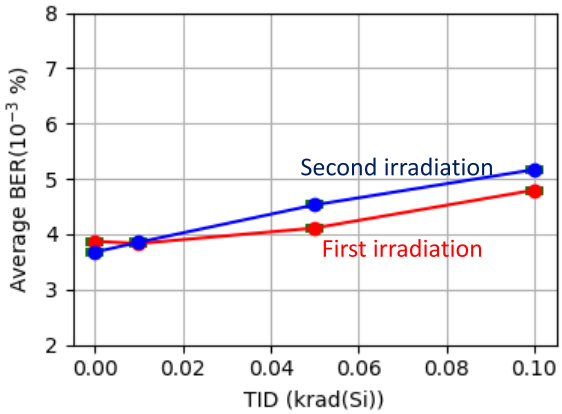

Fig. 7. Average BER for different dose after first exposure and repeated experiment for 2-D NAND chips of 20 nm node.

to reduce this V_t margin, erroneous readings take place. Thus, the higher this V_t margin, the greater is the TID tolerance of the chip and lesser is the TID sensitivity. In other words, to increase the TID sensitivity of a given chip one needs to minimize the manufacturer specified default V_t margin. One effective approach to implement this on COTS memory chips is the read-retry method which allows shifting the read reference voltage during a read operation [25]. Fig. 6(a) explains the read-retry technique where we show a different position of reference voltage with V'_{ref}. We described the implementation procedure of the read-retry command in our previous publication [25]. Here we use the same read-retry technique to increase the TID sensitivity of the chip. Fig. 6(b) shows the measured BER data from a 2-D NAND chip of 20 nm technology node using the read-retry technique. We find that BER increases at a higher rate with TID for the shifted read reference voltage compared with the default V_{ref}. Fig. 6(c) expands the measured data for 100 rad (Si) range, which shows that even 10 rad (Si) results in a significant and detectable BER increase in the memory array. However, 10 rad (Si) may not be considered as the minimum TID detection limit. Instead, it is the minimum TID used in the experiment. In general, the minimum TID detection limit depends on the exact chip details and noise associated during the measurements.

E. Repeatability Test

For any sensor, repeatability is an important criterion. We performed the repeatability test by doing irradiation experiment two times on the same memory chip. After the first irradiation experiment, we erased the chip and wrote the same data pattern again. Fig. 7 shows the results of the repeatability test. We found very close BER values in both irradiation experiments which confirm that TID-dependent BER is repeatable for low TID values.

V. Conclusion

In this article, we have provided an analytical model to correlate the BER response of commercial NAND flash memory chips as a function of TID values. We find that our analytical model is useful for BER projection at higher TID values [$\sim$20 krad (Si)] from the measured data at lower TID values [$<$1 krad (Si)]. Based on the analytical framework and experimental data, we formulated essential design considerations for flash memory-based dosimeters. We have experimentally evaluated the impact of chip-to-chip variability, intrinsic error issues and noise-margin during memory read-out operation on the accuracy and sensitivity of the dosimeter. In addition, we discussed possible countermeasures to improve accuracy and sensitivity of the dosimeter.

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