

New Total-Ionizing-Dose Resistant Data Storing Technique for NAND Flash Memory

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Abstract—This paper describes a new non-charge-based data storing technique in NAND flash memory called watermark that encodes read-only data in the form of physical properties of flash memory cells. Unlike traditional charge-based data storing method in flash memory, the proposed technique is resistant to total ionizing dose (TID) effects. To evaluate its resistance to irradiation effects, we analyze data stored in several commercial single-level-cell (SLC) flash memory chips from different vendors and technology nodes. These chips are irradiated using a Co-60 gamma-ray source array for up to 100 krad(Si) at Sandia National Laboratories. Experimental evaluation performed on a flash chip from Samsung shows that the intrinsic bit error rate (BER) of watermark increases from $\sim 0.8\%$ for TID = 0 krad(Si) to $\sim 1\%$ for TID = 100 krad(Si). Conversely, the BER of charge-based data stored on the same chip increases from 0% at TID = 0 krad(Si) to 1.5% at TID = 100 krad(Si). The results imply that the proposed technique may potentially offer significant improvements in data integrity relative to traditional charge-based data storage for very high radiation (TID > 100 krad(Si)) environments. These gains in data integrity relative to the charge-based data storage are useful in radiation-prone environments, but they come at the cost of increased write times and higher BERs before irradiation.

Index Terms—NAND flash, ionizing radiation, memory reliability, single-level cell (SLC), total-ionizing-dose, watermark.

I. INTRODUCTION

NAND flash memories are a very attractive storage solution across many application domains as they offer the highest bit density, small form-factor, low energy consumption, and low cost. Unfortunately, NAND flash memories are quite vulnerable to the ionizing radiation effects [1]–[6], thus limiting their use in radiation-prone environments.

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To address this vulnerability, radiation-hardened non-volatile memories (NVMs) can be used. However, limited volumes and long development cycles result in the high cost of radiation-hard NVMs that lag behind the commercial off-the-shelf (COTS) NVMs in their functionality, speed, and capacity. As a result, state-of-the-art radiation-hardened NVMs are impractical for emerging data-intensive machine learning applications that require large storage density (> terabytes per die). Hence, there exists a need to enhance the radiation tolerance of the COTS NAND flash memories which will enable their use in data-intensive applications in harsh environments.

NAND flash memories store information in the form of charge on the floating gate, making them sensitive to ionizing radiation. A considerable amount of work has been done to understand the radiation-induced charge loss effects on flash memory [1]–[4]. In addition, several studies investigated radiation-induced bit error rate (BER) on COTS memory chips with single-level-cell (SLC) [7]–[9], multi-level-cell (MLC) [10]–[13], and triple-level-cell (TLC) [14] configurations. Bagatin *et al.* [15] irradiated flash memory chips in different configurations, while varying the total ionizing dose (TID) from 10 to 100 krad(Si). Their results showed that MLC and TLC flash memory chips have a significantly higher sensitivity to TID than SLC NAND chips. Irom *et al.* [16] reported the BER of more than 10% for SLC chips when irradiated with 50 krad(Si), even though SLC memory chips are considered to be highly reliable in a radiation-prone environment.

In this paper, we evaluate resilience of watermark [17], a recently proposed technique for storing read-only data in NAND flash memory arrays, to TID. Watermark stores data in the form of analog properties of memory cells rather than in the form of electronic charges. Analog properties of flash memory cells are changed selectively through repeated program-erase (PE) cycles. Flash cells that repeatedly go through charge/discharge cycles accumulate defects in their oxide layers, whereas cells that remain in the erased state during PE cycling do not [18]. These defect states change analog flash cell properties permanently; hence, the proposed technique resembles imprinting watermarks that behave as one-time-programmable (OTP) memories [17], [19]. Whereas information stored in the form of charge is affected by radiation effects, the information stored in the form of analog properties is fundamentally more resistant to ionizing

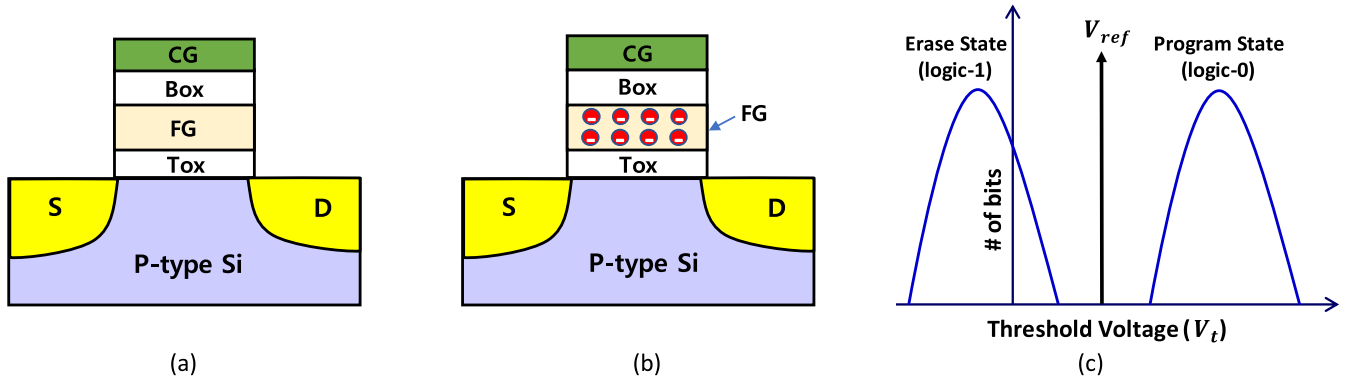


Fig. 1. (a) A cross section of a flash memory cell in the erased state. (b) A cross section of a flash cell in the programmed state. (c) Typical cell V_t distribution for the erased and programmed states.

radiation. Thus, using NAND flash memories to store read-only OTP data offers a new technique for radiation resistant, high density, cold storage suitable for space and nuclear industry applications.

We evaluate the proposed watermark technique and its resistance to ionizing radiation effects by conducting experiments on several COTS NAND flash memory chips from different manufacturers and technology nodes. The chips with imprinted watermarks are exposed to gamma-ray irradiation using Co-60 source arrays at Gamma Irradiation Facility at Sandia National Laboratories, NM. The data integrity of watermarked information and equivalent information stored in the form of charge is evaluated by measuring the intrinsic BER before and after irradiation experiments.

The rest of the paper is organized as follows. Section II provides a brief background of NAND flash memory technology. The proposed watermark technique is discussed in Section III. Section IV describes the experimental evaluation. Section V discusses the experimental evaluation results. Finally, Section VI concludes the article.

II. BACKGROUND

A. Structure and Operations of NAND Flash Memory Array

Fig. 1(a) shows the device structure of a flash memory cell made using planar fabrication technology. It is essentially a floating-gate (FG) metal-oxide-semiconductor field-effect transistor (MOSFET). The presence of trapped negative charge on the FG (see Fig. 1(b)) effectively increases the transistor's threshold voltage (V_t) relative to the case when there is no charge on the FG. Thus, a flash memory cell is a charge-based analog memory. The program operation charges the FG with electrons, whereas the erase operation removes the charges from the FG. The read operation of a flash memory cell involves applying a read voltage (V_{ref}) on the control gate and sensing the cell's V_t (Fig. 1(c)). An erased cell conducts the current, and that is sensed as a logic 1, whereas a programmed cell does not conduct the current, and that is sensed as a logic 0.

A flash memory chip typically includes multiple identical memory blocks. Each memory block is divided into multiple logical pages. The page size varies from 2 to 16 kilobytes, depending on the manufacturer. All the memory cells of a

given page are connected to a shared word line through the control gate. The NAND architecture means that data are read and programmed at the page level, whereas erase operations are performed at the level of entire memory blocks. Any flash cell that is set to a logic 0 by a page program operation can only be reset to a logic 1 by erasing the entire block.

B. Flash Memory Endurance

Flash memory cells have limited endurance, typically $\sim 100k$ PE cycles for SLC and 3k to 5k cycles for MLC. Each PE cycle involves the application of high voltage on memory cells to transfer electrons back and forth through the tunnel oxide layer as shown in Fig. 2(a) with red arrows. This mechanism is called Fowler-Nordheim tunneling. Since tunneling requires a very high electric field across the oxide, it creates defects in the oxide and at the oxide-Si interface as shown in Fig. 2(b). After a certain number of PE operations, a significant number of defects created in the tunnel oxide layer degrades the cell's ability to hold charges. As a result, the data retention properties of flash memory degrade. We call the cells with a small number of defects "good" cells and the cells with a high density of defects "bad" cells. Even though bad cells remain functional, their physical properties such as intrinsic threshold voltage, charge retention, and program/erase speed differ significantly from good cells. In this work, we selectively make certain cells bad by repeated PE operations and then compare their physical properties to distinguish them from good ones.

III. WATERMARK WRITING AND READING OPERATIONS

This section describes basic operations for the proposed watermark technique: imprinting the watermark or writing information and retrieving the watermark or reading information.

A. Watermark Imprinting

The watermark imprinting involves repeated PE operations to selectively alter the analog properties of flash memory cells. Fig. 2(c) demonstrates the watermark imprinting, assuming the watermark information is an integer 2021 or 0x07E5. The first row shows the physical states of the selected memory cells in

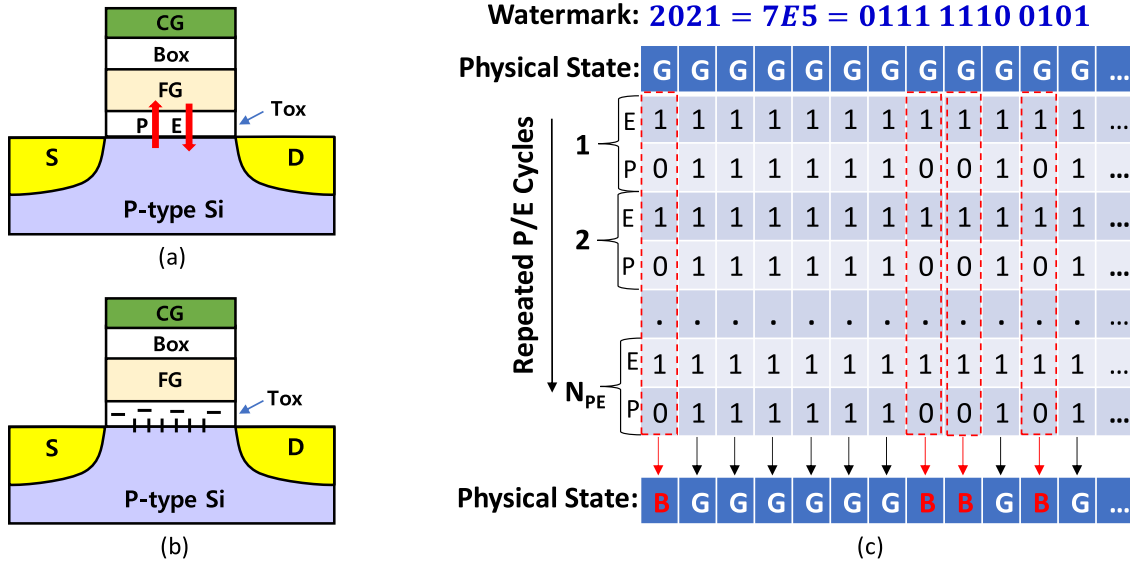


Fig. 2. (a) Illustration of a good flash memory cell with no defects in the oxide. (b) Illustration of a bad flash memory cell with high density of defect states in the oxide. (c) Watermark imprinting technique using repeated program-erase (PE) operations.

a fresh memory page, where all the cells are in good (G) condition. The second row shows the logical states of the memory cells after the erase operation. The third row presents the digital equivalent of the watermark written by a standard page program operation. The fourth row and onwards illustrate the repeated PE operations for N_{PE} times. The process of repeated erasing and programming is continued until there are sufficient differences in physical properties between (i) memory cells that never change their state - “good” or G in Fig. 2(c), and (ii) memory cells that continually go through charge/discharge cycles - “bad” or B in Fig. 2(c). Therefore, the desired information is encoded using physical cell characteristics that cannot be easily altered by ionizing radiation. Note that flash memory cells become bad due to the tunneling of electrons back and forth through the oxide layer, which creates defects in the oxide. That is how we imprint the watermark by selectively altering the physical characteristics of the flash memory cell. The number of PE operations needed for watermark imprinting depends on the type of flash memory, technology node, and manufacturer. A more detailed analysis of the impact the parameter N_{PE} has on the integrity of the imprinted data in various chips is given in our prior work [17].

In a typical use scenario, the Flash Translation Layer (FTL) provides functions for storing read-only data through watermark imprinting and extracting read-only data. In one implementation, a single flash memory block or a subset of flash memory blocks is reserved just for storing read-only data through watermark imprinting. Thus, they are designated by the FTL as such and not used for storing regular charge-based data. An alternative implementation may allow for storing read-only data as well as regular charge-based data on the same flash memory blocks. However, in this case the FTL will have to be made aware that these flash blocks have already been stressed, so the number of PE cycles for charge-based data should be reduced accordingly. Additional stress caused

by program-erase cycling when dealing with charge-based data is not likely to sufficiently change the properties of flash memory cells.

B. Watermark Retrieval

The watermark retrieval relies on distinguishing between G and B memory cells using a standard digital interface of flash memory chips. In our previous work [17], we demonstrated that partial flash memory operations can be applied to extract information about the physical properties of memory cells. In this work, we utilize a partial erase operation to distinguish between G and B cells. Fig. 3(a) illustrates watermark retrieval. The first row shows the physical states of memory cells, where two different colors represent B (red) and G (black) memory cells. We first perform a traditional charge-based memory write operation with all zero data which is depicted in the second row of Fig. 3(a). Next, we perform a partial block erase operation and read the logic state of the page. The partial block erase operation on the all-zero page flips the G cells to logic 1, whereas the B cells remain in logic 0 as shown in the last row of Fig. 3(a). Therefore, with a standard digital interface, we can distinguish between the G and B cells and retrieve the watermark.

Fig. 3(b) illustrates an implementation of the partial erase operation on a COTS NAND memory chip. The solid black line represents the status of the Ready/Busy pin of the NAND flash memory chip during the standard block erase operation. The pin is low when the memory chip is busy performing the erase operation. Typically, the erase operation takes between 1 ms and 10 ms (t_{ers}). However, the erase operation can be terminated prematurely by issuing a RESET command, which is illustrated with a red dashed line in Fig. 3(b). The premature termination of the erase operation causes some cells to be erased (G cells) while some cells remain in the programmed

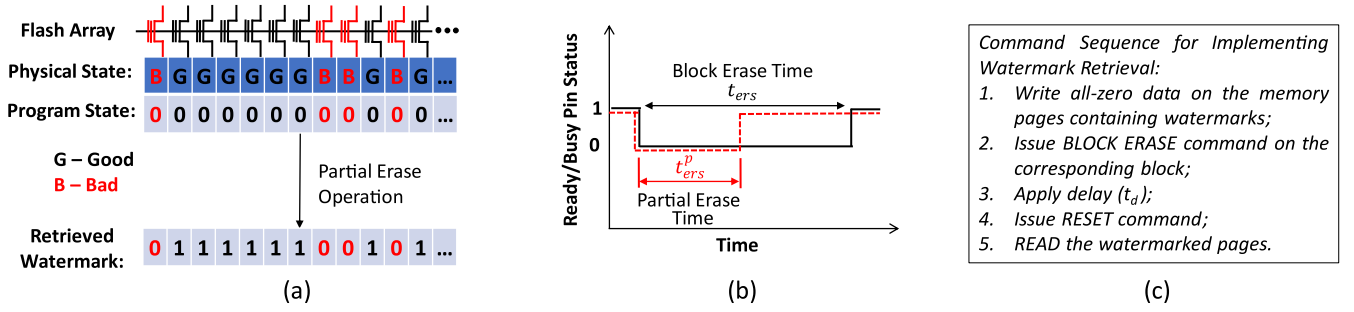


Fig. 3. (a) Watermark retrieval. (b) Illustration of block erase time (t_{ers}) and partial erase time (t_{ers}^p) based on monitoring the Ready/Busy pin status of a flash chip. (c) Command sequence for implementing watermark retrieval.

state (B cells). The exact command sequence for implementing the watermark retrieval is given in Fig. 3(c). The partial erase time (t_{ers}^p) can be controlled by the time delay (t_d) parameter from the host as illustrated in line 3 of the command sequence.

IV. EXPERIMENTAL EVALUATION

To evaluate the robustness of watermarks against ionizing radiation, we use COTS flash memory chips from different manufacturers. They differ in technology nodes and capacity. Irradiation experiments are performed at Sandia National Laboratories Gamma Irradiation Facility using a Co-60 source array at the dose rate of 18.6 rad(Si)/s. Irradiation is performed on the packaged NAND flash memory chips with all pins grounded. The direction of gamma rays during irradiation is perpendicular to the top surface of the chip [20]. The flash operations are performed using a custom-designed flash test board. The test board contains a 48-pin NAND flash socket to hold a thin small outline package (TSOP) flash memory chip and an Atmel ATSAM3U4C ARM Cortex-M3 microcontroller for issuing commands and sending/receiving data from the chip. This hardware setup is used to perform basic flash operations and it is not exposed to gamma radiation.

Several memory chips are exposed to different TID levels up to 100 krad(Si) to evaluate the TID response on the watermarks. Before the memory chips are exposed to radiation, we imprint watermarks following the steps described in Section III-A. Then, we perform watermark retrieval steps as described in Section III-B and calculate the raw pre-irradiation BER. Next, we expose the chips to gamma radiation. After irradiation, we again retrieve the watermark data, calculate the post-irradiation BER, and compare it to the pre-irradiation BER. Note that several chips became non-functional at the TIDs above 100 krad(Si) due to the failures in the peripheral circuits. In such cases, we report the maximum TID at which the chip is fully functional.

V. RESULTS AND DISCUSSION

In this section, we present a detailed analysis of the BER on the retrieved watermarks pre-irradiation as a function of the partial erase time. Next, we analyze the BER on the retrieved watermarks post-irradiation and compare the two.

A. Pre-Irradiation BER Analysis on Watermark

We perform the experimental evaluation of the watermark imprinting/retrieval using a 2D SLC memory chip from Samsung. We choose an image of Einstein of size 4 kilobytes as a watermark. We first imprint the image on a memory page using $N_{PE} = 100k$ PE operations. The N_{PE} is a design variable in the watermark imprinting scheme and its value needs to be carefully chosen in order to minimize the BER in the retrieved watermark. For the chip under the test, we find that $N_{PE} = 100k$ offers the minimum BER. Next, we retrieve the watermark using the partial erase operation following the steps discussed in Section III-B. Fig. 4(a) shows our evaluation results where the BER of the retrieved watermark is plotted as a function of the partial erase time, t_{ers}^p , in μs . Since the image consists of $\sim 50\%$ 0s/1s, the BER is $\sim 50\%$ when we start with an all-zero programmed page. Next, we repeat the experiment by gradually increasing t_{ers}^p . The BER of the retrieved watermark remains close to 50% because no flash cells get erased for small values of t_{ers}^p . However, with a further increase in t_{ers}^p , G flash cells get erased whereas B cells remain programmed. Since G cells represent logic 1s and B cells represent logic 0s of the watermark, the BER of the retrieved watermark reduces. It reaches the minimum and then starts to increase as we keep further increasing t_{ers}^p . Eventually, all flash memory cells are fully erased.

The minimum BER point determines the optimal t_{ers}^p for retrieving the watermark. Fig. 4(b) illustrates the cell V_t distribution before and after the partial erase operation. Before the partial erase operation, the V_t distribution of good and bad cells is indistinguishable. Since NAND memory internally employs a program-verify based incremental step pulse programming (ISPP) scheme, it ensures that both good and bad cells have similar looking V_t distribution at the end of the programming phase. Since good cells get erased faster than bad cells [21], the partial erase operation will cause a separation in the V_t distribution as illustrated with solid blue and dashed red lines in Fig. 4(b). Note that the distribution depicted in Fig. 4(b) illustrates the minimum BER point defined by the crossing point of the V_t distributions. If the read reference voltage (V_{ref}) coincides with the V_t distribution crossing point, it will yield the minimum BER in the retrieved watermarks. Fine-grained control of t_{ers}^p is necessary to arrive at this condition. The optimal t_{ers}^p is a chip-dependent

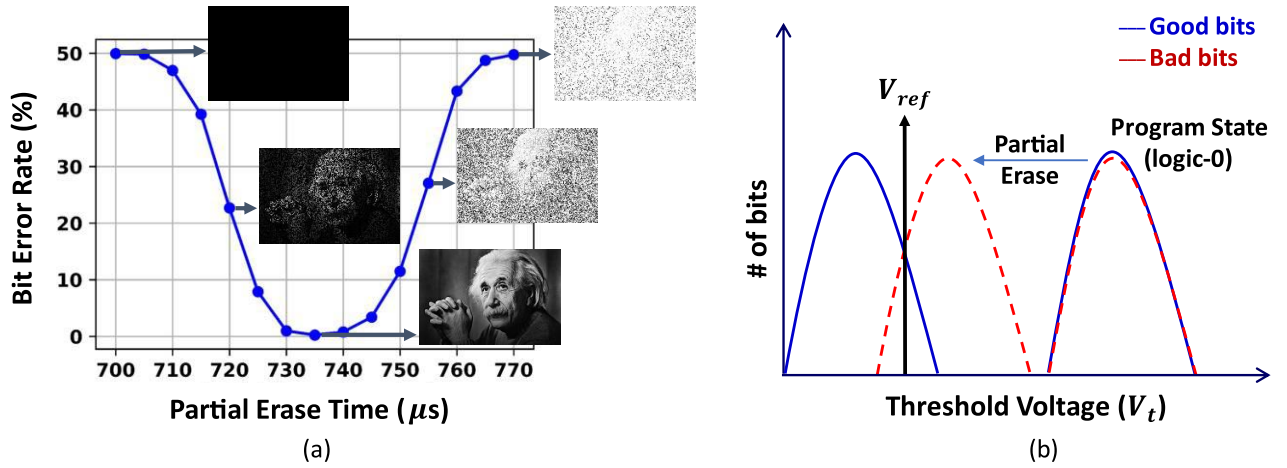


Fig. 4. (a) The BER for the retrieved watermark as a function of partial erase time. (b) Illustration of the minimum BER condition in the retrieved watermark.

TABLE I
PRE-AND POST-IRRADIATION MINIMUM BER RESULTS USING WATERMARK TECHNIQUE

Company	Part Number	Description	N _{PE}	Minimum BER (Pre-irradiation)	TID (krad(Si))	Minimum BER (Post-irradiation)
Samsung	K9F2G08U0M	2D SLC (2Gb) 90 nm node	100k	~0.24%	100	~0.48%
Toshiba	TC58NVG2S3ETA00	2D SLC (4Gb) 43 nm node	50k	~3.80%	50	~5.08%
Toshiba	TC58NVG2S0FTA00	2D SLC (4Gb) 32 nm node	50k	~2.07%	75	~3.35%
Micron	MT29F8G08ABACAWP:C	2D SLC (8Gb) 25 nm node	100k	~1.22%	100	~3.70%
Micron	MT29F256G08CBCBB	3D MLC (SLC Mode) (256Gb)	3k	~6.96%	50	~10.29%
				~2.06%	100	~3.34%

parameter, and it needs to be characterized for each family of chips.

Alternatively, we can estimate the optimal t_{ers}^p during the watermark retrieval process. For example, we can use a small part of the memory page to imprint a known watermark. The same watermark imprinting process is used for both the known and unknown watermark – please note that here the actual data corresponds to the unknown watermark. In this case, the retrieval process involves multiple steps. The t_{ers}^p is varied within a predefined range and the BER in the known watermark is monitored. The optimal t_{ers}^p is determined when the BER for the known watermark reaches the minimum. Once the optimal t_{ers}^p is determined, it is then used to retrieve the actual data (unknown watermark). Please note that depending on the size of the unknown watermark, both the known and unknown watermark can be split among multiple pages of the flash memory blocks. This approach can allow for page-level fine tuning on t_{ers}^p .

Whereas our watermark consists of ~50% 0s/1s, we conducted experiments with different data patterns in the watermark, ranging from 12.5% to 75% of B cells. We find that changes in the data pattern do not significantly impact the optimal t_{ers}^p on chips used in this study. This means the optimal t_{ers}^p during the watermark retrieval process does not appear to

be data dependent. However, in case that this becomes an issue in other chips, using known watermarks with distributions of 0s/1s that match distributions of 0s/1s in the actual data can be considered.

We perform watermark imprinting/retrieval evaluation on several memory chips from different manufacturers. Table I summarizes our characterization results. We find that the minimum BER of the retrieved watermark varies significantly depending on the type of flash memory, technology node, and manufacturer. The raw BER can be minimized if we encode data on multiple pages and apply a majority voting scheme as described in our previous publication [17]. Nonetheless, the results presented in Table I confirm that the proposed technique is applicable for a wide range of NAND flash chips.

B. Post-Irradiation BER Analysis on Watermark

We evaluate the TID effects on the watermark by comparing its BER from the same chip for the pre-irradiation and the post-irradiation conditions. Fig. 5 summarizes our evaluation results. Fig. 5(a) shows the pre-irradiation (blue line) and post-irradiation (red line) BER of the watermark retrieval as a function of the partial erase time. Fig. 5(b) shows the respective BERs as a function of the page number in a

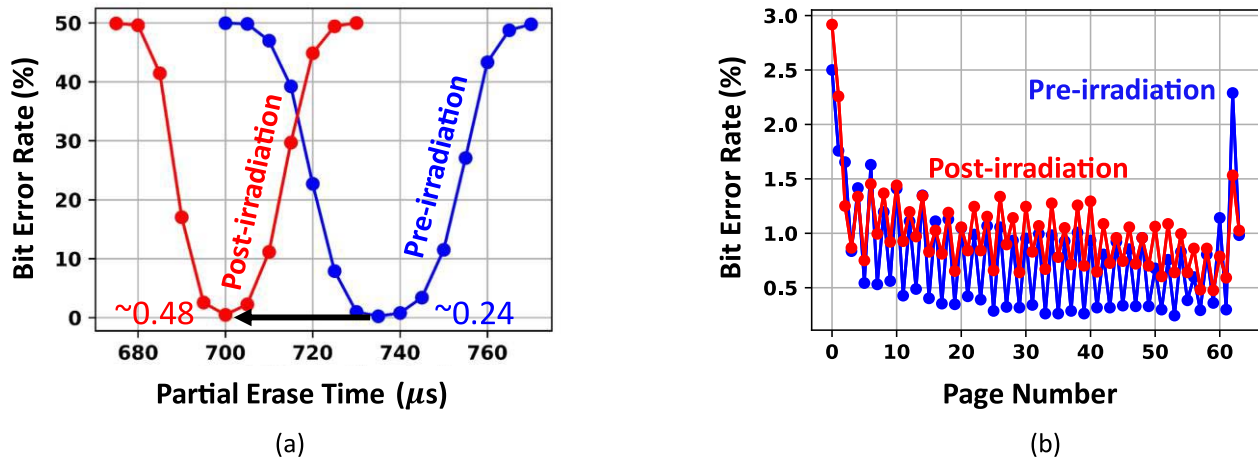


Fig. 5. Pre- and post-irradiation BER for Samsung 2Gb SLC 90 nm node (TID = 100 krad(Si)): (a) The BER as a function of partial erase time (μs). (b) The minimum BER as a function of page number within a block.

block. The memory chip is irradiated with gamma rays up to TID = 100 krad(Si). The results from Fig. 5(a) show that the minimum BER of the watermark retrieval marginally increases after irradiation. Next, the irradiation affects the optimal t_{ers}^p that corresponds to the minimum BER: the post-irradiation optimal t_{ers}^p reduces to 700 μs from the original 735 μs. Note that after irradiation, we estimate the optimal t_{ers}^p of the chip by following the same minimum BER monitoring strategy discussed in the previous section. Several factors can explain these observations. First, ionizing radiation not only causes charge loss but also creates defect states in the oxide and the oxide-Si interfaces. Thus, the physical properties of both the good and bad cells are altered by irradiation. Since the proposed technique relies on relative cell physical properties to imprint information, the TID-induced oxide defects may convert a few good bits into marginally bad ones resulting in a higher BER. Second, ionizing radiation impacts the charge pumps, decoders, and other peripheral circuits present in the NAND memory chip. We believe that the change in the optimal partial erase timing is due to the impact of the TID on the peripheral circuits.

Fig. 5(b) shows the page-by-page comparison of watermark BER before and after irradiation. A memory block in the chip under test contains 64 logical pages. We imprint watermark on all 64 pages. We observe page-to-page BER variation in the retrieved watermark. It is important to note that NAND memories usually exhibit page-to-page process variation which is reflected in the BER variation of the retrieved watermark. The block average BER of the watermark for the pre-irradiation case is 0.8%. The BER increases in most of the memory pages for the post-irradiation condition. The block average BER after irradiation is ~1%.

Even though Fig. 5 shows the irradiation effects on watermarks only on Samsung 2Gb chips, we evaluate multiple chips from different vendors as well. Table I summarizes our evaluation results. Several chips that show high BER in the watermarks even for the pre-irradiation condition see an increase in the BER after irradiation. Thus, optimizing the watermark imprinting and retrieval condition will be essential

for using it on those chips. Note that we report the BER from those chips that remain fully functional after irradiation. We confirm the chip functionality by performing memory operations such as erase, write, and read on the irradiated chips. However, there were a few chips that became non-functional after a certain dose of irradiation, and we could not recover the watermark from them.

C. TID-Induced BER: Watermark vs. Charge-Based Storage

We compare the TID-induced BER in the watermark with that of the traditional charge-based data by writing the same data pattern in an SLC memory chip from Samsung. Note that both watermark and the charge-based regular data are written on the same chip but in different memory blocks. After irradiation, we compare the BER of the watermark with that of SLC data. The collected BERs before irradiation and after irradiation (TID = 100 krad(Si)) on the SLC memory chip from Samsung are shown in Fig. 6(a) and Fig. 6(b), respectively. The green line shows the per-page BER for the watermark data, while the orange line shows the per-page BER data for the charge-based SLC storage. Note that before irradiation, the charge-based SLC data has zero percent BER on all the memory pages of the block. After irradiation, the BER on all 64 pages of the SLC data increases significantly as shown in Fig. 6(b). The block average BER of the charge-based data after irradiation is ~1.5%. Moreover, we observe a significant page-to-page variation in the BER where the last few pages of the flash block have high bit error rates. Unlike the charge-based storage, the watermark BER remains significantly lower after irradiation and exhibits smaller page-to-page variation. The block average BER of the watermark data increases from 0.8% (TID = 0 krad(Si)) to ~1% at TID = 100 krad(Si).

The BER for charge-based data, shown Fig. 6(b), reveals a growing trend as a function of the page number within a flash memory block. A similar trend is observed on other flash memory blocks of the Samsung chip tested in this study. This trend appears to be unique for the Samsung chip as we have not observed it in other chips used in this study, e.g., the page

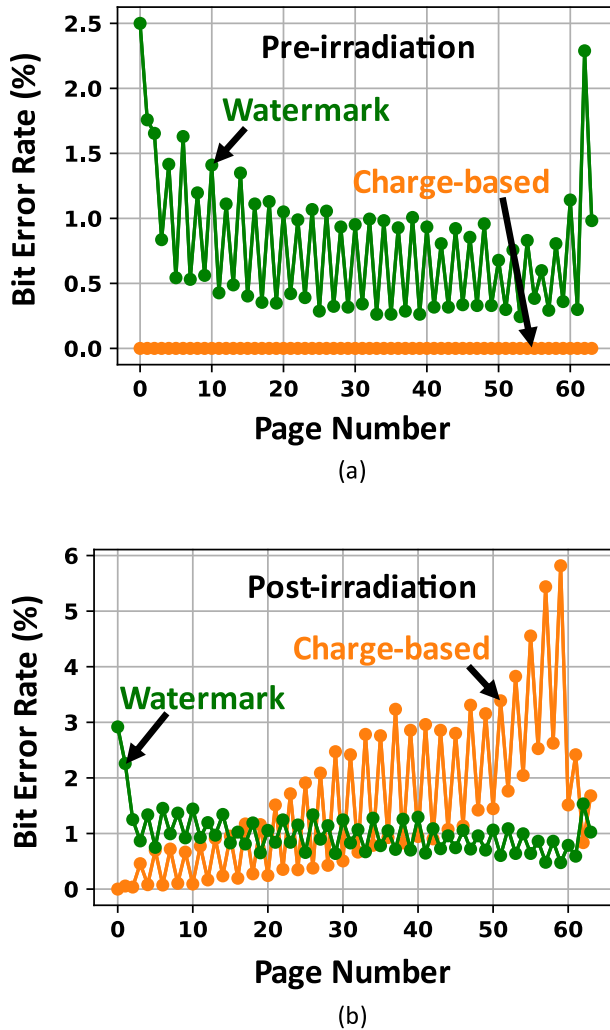


Fig. 6. Comparison of the watermarked BER and the charge-based traditional SLC data encoding BER (a) before irradiation and (b) after irradiation (TID = 100 krad(Si)) from Samsung 2Gb SLC 90 nm node.

BERs in Toshiba chips appear to be uniform. We believe that this trend observed for charge-based data in the Samsung chip is an artifact of the chip geometry or perhaps specific implementation of the programming scheme. However, we cannot make definitive statements about the causes for this trend in the BER because we do not have insights into the chips' organization and inner workings of its on-chip logic.

It is important to note the difference between the rate of increase in BER with TID for the watermark and the charge-based SLC storage. Fig. 7 shows these rates for two chips from Samsung and Toshiba. Since SLC storage provides a large voltage margin between the erase and program states, SLC-BER remains zero until TID ~ 50 krad(Si) for the Samsung chip in Fig. 7(a). The SLC-BER sharply rises for higher TID due to exponential tails of the Gaussian-like program state distribution [22]. Conversely, the watermark BER increases linearly from $\sim 0.8\%$ (TID = 0 krad(Si)) to 1% for TID = 100 krad(Si). Similar results were obtained for the Toshiba SLC chip in Fig. 7(b), where we find that the average BER of the charge-based storage sharply increases after

75 krad(Si), whereas the watermark BER increases linearly with TID. We did not observe any crossover between the average BER of watermark and charge-based storage in the Toshiba chip as we could not collect data beyond 100 krad(Si) due to the functional failure of the chip. However, we find that the worst-case BER of charge-based storage goes higher than that of watermark storage for the Toshiba chip in Fig. 7(d). Since charge-based storage shows significant page-to-page BER variation in comparison to watermark, BER crossover takes place at a lower value TID. Given the observed BER trends, we expect that the BER gap between the watermark and the charge-based SLC storage will be much wider for higher values of TID, provided that the peripheral circuits can be made with a radiation hard process. With the advent of Xtacking technology from YMTC [23], it might be possible to fabricate the peripheral circuits using a radiation hard process. Thus, the future generation of 3D NAND technology promises to extend the radiation tolerance of NAND flash chips.

Charge loss under ionizing radiation is a fundamental vulnerability of NAND storage, and hence it will be the limiting factor for the TID tolerance of future NAND storage even with radiation-hardened peripheral circuitry. Therefore, we believe the watermark technique offers a radiation-tolerant storage alternative for the read-only type of data in future NAND-based storage systems. For example, the watermark technique can be an interesting option for cold-storage applications in space, where data integrity needs to be ensured in presence of a high irradiation dose. Using frequent refreshes of charge-based data can be used as a way to achieve high data integrity in radiation-prone environments. Whereas this approach is commonly used and offers fast write and read times, it requires frequent memory refreshes and thus may increase latency and power consumption. Thus, the watermark technique can be used for dealing with cold and read-only data that needs to be resilient to radiation in systems where frequent data refreshes are not desirable due to power constraints.

VI. CONCLUSION

This paper explores the TID-resilience of a novel data storing technique for NAND flash memories called watermark. We experimentally demonstrate the watermark technique on a number of COTS memory chips. Our evaluations show that the watermark BER increases linearly with an increase in TID, whereas traditional charge-based BER increases exponentially. For example, we show that the BER of the watermark data in a chip from Samsung increases from 0.8% (TID = 0 krad(Si)) to 1% (TID = 100 krad(Si)), whereas the BER for charge-based SLC data on the same chip increases from 0% (TID = 0 and 50 krad(Si)) to $\sim 1.5\%$ for TID = 100 krad(Si). The proposed data storing technique can be easily implemented using the NAND storage controller without requiring any hardware modification. Hence, it can be applied to a wide range of flash memory chips. However, the proposed technique comes with certain limitations in comparison with the traditional charge-based data storage such as long imprinting time and higher BER before irradiation.

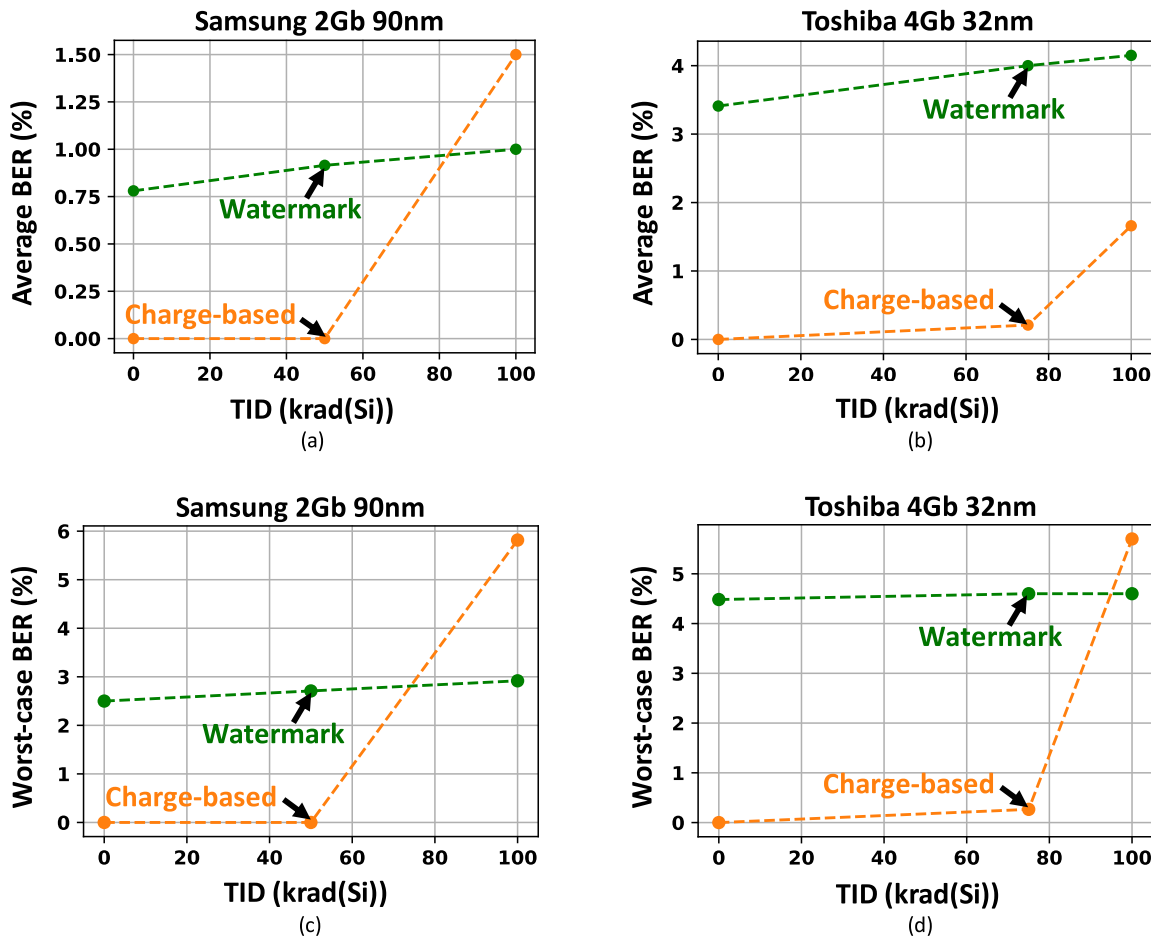


Fig. 7. Comparison of the average BER in charge-based storage and watermark as a function of irradiation dose for two different SLC chips from (a) Samsung and (b) Toshiba. Comparison of the worst-case BER (among different memory pages) in charge-based storage and watermark are shown in (c) and (d).

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