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Total-Ionizing-Dose Effects on Threshold Voltage Distribution of 64-Layer 3D NAND Memories

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***Abstract*—We measure total-ionizing-dose (TID) induced threshold voltage (V_t) loss of a commercial 64-layer triple-level-cell (TLC) 3D NAND memory using user-mode commands. Our experiments show that V_t distributions closely follow Gaussian distributions. At increasing TID, the distributions shift toward lower average values and the distribution widths widen. We calculate exact cell V_t shifts from the pre-irradiation conditions at different TID values. We find that V_t loss (ΔV_t) distributions also follow Gaussian distributions. We also find that ΔV_t values strongly depend on the cell programmed states.**

***Index Terms*—3-D NAND, ionizing radiation, tri-level-cell (TLC), total ionizing dose (TID).**

I. Introduction

NAND flash memory is commercially available and most attractive solution for high-density, non-volatile data storage applications [1]–[3]. However, flash technology is vulnerable to total-ionizing-dose (TID) effects which eventually limits its application for space and nuclear environments [4]–[10]. Previous studies demonstrated that commercial flash memory chips experience accelerated data corruption issues due to threshold voltage (V_t) shifts of programmed memory cells under ionizing radiation. For example, Bagatin et al. [11] recently demonstrated the TID effects on cell V_t distribution of the 3D NAND technology. They concluded that cell V_t distribution downshifts and widens with TID. Unfortunately, they did not report the actual magnitude of V_t downshift due to proprietary nature of V_t measurement procedure used in their chip. In this paper, we experimentally evaluate cell by cell V_t loss magnitude as a function of TID from a commercial 64-layer TLC 3D NAND memory chip using publicly available memory commands. The command for cell V_t measurement is a very recent addition in the user-mode command set which is available for the chip under test. Following are the key findings of our research:

1) In close agreement with previous literature reports, cell by cell V_t distribution becomes wider (larger standard deviation, σ) and the distribution shifts toward lower V_t values (lower mean, μ).
2) V_t loss (ΔV_t) is linear with TID (slope≈8mV/krad(Si)) for the highest programmed state (L_7) of the TLC memory. However, lower programmed states (for example, L_1) show saturating trend for TID values more than 30 krad(Si).
3) Cell by cell ΔV_t values show significant variation for a given programmed state. We show that ΔV_t distribution closely follows the Gaussian distribution. Standard deviation of the ΔV_t distribution increases from 60 mV (TID = 10 krad(Si)) to 120 mV (TID = 50 krad(Si)) for the highest programmed state.

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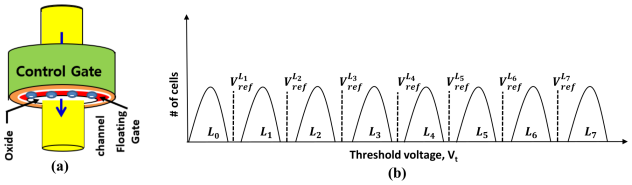

Fig. 1. (a) Schematic of a memory cell in 3D NAND technology. (b) Cell V_t distribution (L_0-L_7) in TLC configuration.

Fig. 1(a) shows the schematic of a flash memory cell in 3D NAND technology. It's essentially a gate-all-around (GAA) transistor [12] with a floating gate (FG) technology. Data is stored in the form of the electronic charge in the FG layer of the transistor gate stack. In TLC NAND flash devices, each memory cell holds three bits of information. The cell threshold voltage (V_t) distribution of TLC memory, thus, has 8 different V_t-states as shown in Fig. 1(b). V_t states are labeled with L_0, L_1,...,L_7 where L_0 state is the lowest (erased) V_t state and L_7 state is the highest (programmed) V_t state. It should be noted that seven different reference voltages ($V_{ref}^{L_1}$,..,$V_{ref}^{L_7}$) are used to identify the cell states during read operation.

II. Experimental Details

The experimental evaluation was performed on a commercially available off-the-shelf (COTS) 3D NAND memory chip from Micron Technology [13]. The part number of the chip was MT29F1T08EEHAF (1 Terra bit, TLC memory chip). The 3D memory chip contains 4032 logical blocks, where each block consists of 2304 logical pages of size 18,592 bytes (16,384 bytes of user data with 2208 bytes of error correction codes-ECC). The chip is fabricated using 3D NAND technology with 64 vertical layers. The memory chip were in thin small outline package (TSOP). The flash memory chips were irradiated using Co-60 sources to evaluate their TID response at a dose rate of 18.6 rad(Si)/s. The irradiation experiment was performed at the Sandia National Laboratories Gamma

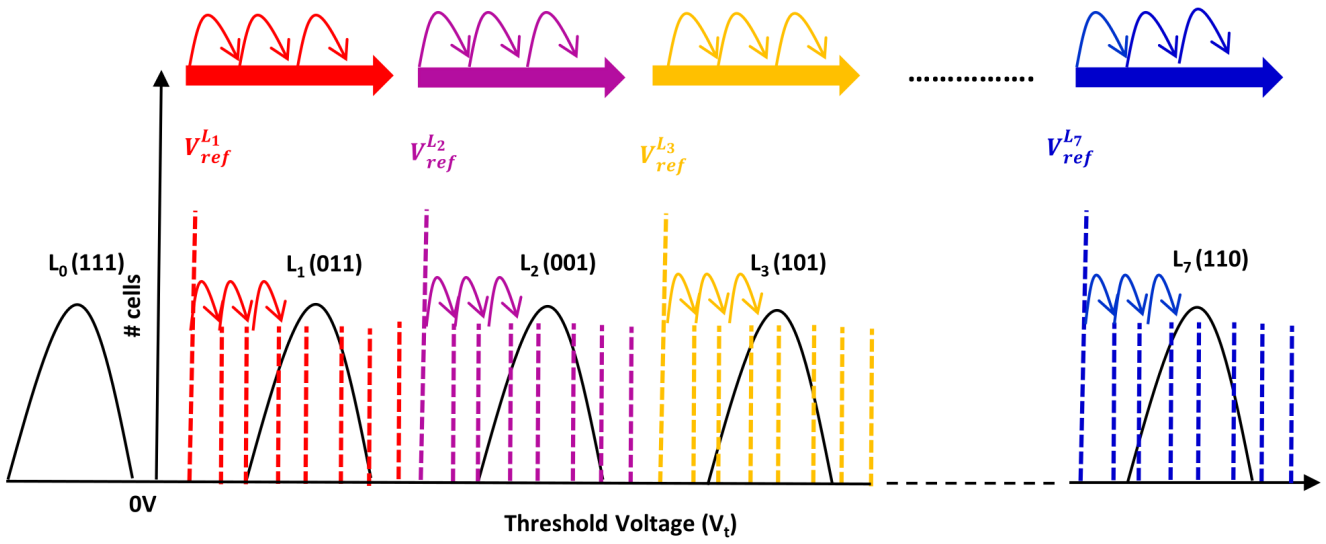

Fig. 2. The read offset operation for each (V_t) state by sweeping the reference voltage (V_{ref}) from default value to right by adding increments of 7.5mV.

Irradiation Facility. All doses are expressed as absorbed dose in Silicon. Gamma irradiation was performed on the TSOP packaged devices with all pins grounded. The direction of gamma rays during irradiation was perpendicular to the top surface of the chip. To interface the raw NAND chip with the computer, we have used a custom-designed hardware board. The hardware setup allows us to access raw memory bits without error correction. There was a time-gap of one hour between irradiation and data readout. The chip under test supports so-called read offset operations [14] that allow the flash controller to adjust read reference voltages: $V_{ref}^{L_1}$,..,$V_{ref}^{L_7}$ (Fig. 1(b)). Fig. 2 conceptually shows the read offset method. In this process, we add an offset voltage incrementally to the reference voltage and thus shift the reference voltage from the default level to $V_{ref}+\Delta V\times i$ where i=0,±1,±2,...±127. For the chip under investigation, ΔV=7.5 mV. For each shifted $V_{ref}^{L_i}$ we read data from the corresponding pages. For example, by shifting $V_{ref}^{L_7}$ from its default value to the right by ∼952 mV in steps of 7.5 mV, we can extract the distribution of the L_7 state. The same process is repeated for the other cell states. This way, we can extract the V_t distributions of all memory cell states. The command sequence to implement read offset operation for ONFI (Open NAND Flash Interface)-compliant memory is as follows:

1) Send Command SET FEATURES (EFh);
2) Send Address for Read Offset Levels (A0h-ACh);
3) Send Parameter for Offset Voltages (00h-FFh);
4) Send Page Address;
5) Send Command PAGE READ.

III. Results and Discussion

A. TID Effects on Cell V_t Distribution

Fig. 3(a)-(d) show a scatter plot of cell by cell V_t values measured at different TID. For simplicity, we show the scatter plot of V_t values for the cells programmed at L_7 state only, however, we collect V_t data for cells in all the states (L_1-L_7), for a specific page. Since V_t values are measured relative to the read reference voltage ($V_{ref}^{L_i}$), we plot the numerical values of (V_t-$V_{ref}^{L_7}$) in the y-axis. There are $\sim 18\times 10^3$ cells in the highest programmed state L_7, which are shown in the x-axis of the plot (Fig. 3(a)) for different TIDs. We observe a significant cell to cell V_t variation (quantified by standard deviation (σ_{V_t})) without any irradiation in the highest programmed state L_7. Cell to cell V_t variation increases with irradiation and mean cell threshold voltage (μ_{V_t}) gradually drops with TID as shown in Fig. 3(a)-(d). We summarize the scatter plots of Fig. 3(a)-(d) in the form of a distribution plot (similar to histogram plot) in Fig. 3(e). Solid lines in Fig. 3(e) represent fitted Gaussian distribution. We observe that V_t distribution for L_7 closely follows the Gaussian distribution. The mean V_t (μ_{V_t}) shifts to lower values and standard deviation of V_t distribution (σ_{V_t}) increases with TID making the distribution wider. Similar observations can be made from the remaining programmed states (L_1-L_6) of the page shown as distributions in Fig. 3(f)-(k).

Next, we show a similar scatter plot of the cell by cell V_t loss or ΔV_t for highest programmed state, L_7 in Fig. 4(a) for different TID values. We realize from the scatter plots of Fig. 4(a) that variation in ΔV_t values also increase with increased dose of radiation. We summarize the scatter plots of Fig. 4(a) in the form of a distribution plot in Fig. 4(b). Again, the solid lines in Fig. 4(b) represent fitted Gaussian distribution. We again observe that ΔV_t variation closely follows the Gaussian distribution. The mean V_t loss ($\mu_{\Delta V_t}$) and standard deviation of ΔV_t distribution ($\sigma_{\Delta V_t}$) increases with TID. The ΔV_t distributions for L_1-L_6 are shown in Fig. 4(c)-(h). Similar conclusions about of the μ and σ of the distributions can be made from Fig. 4(c)-(h).

B. Programmed State Dependent V_t Loss

We compare the programmed state dependent V_t loss with TID in Fig. 5(a). TLC memory has an erased state (L_0)

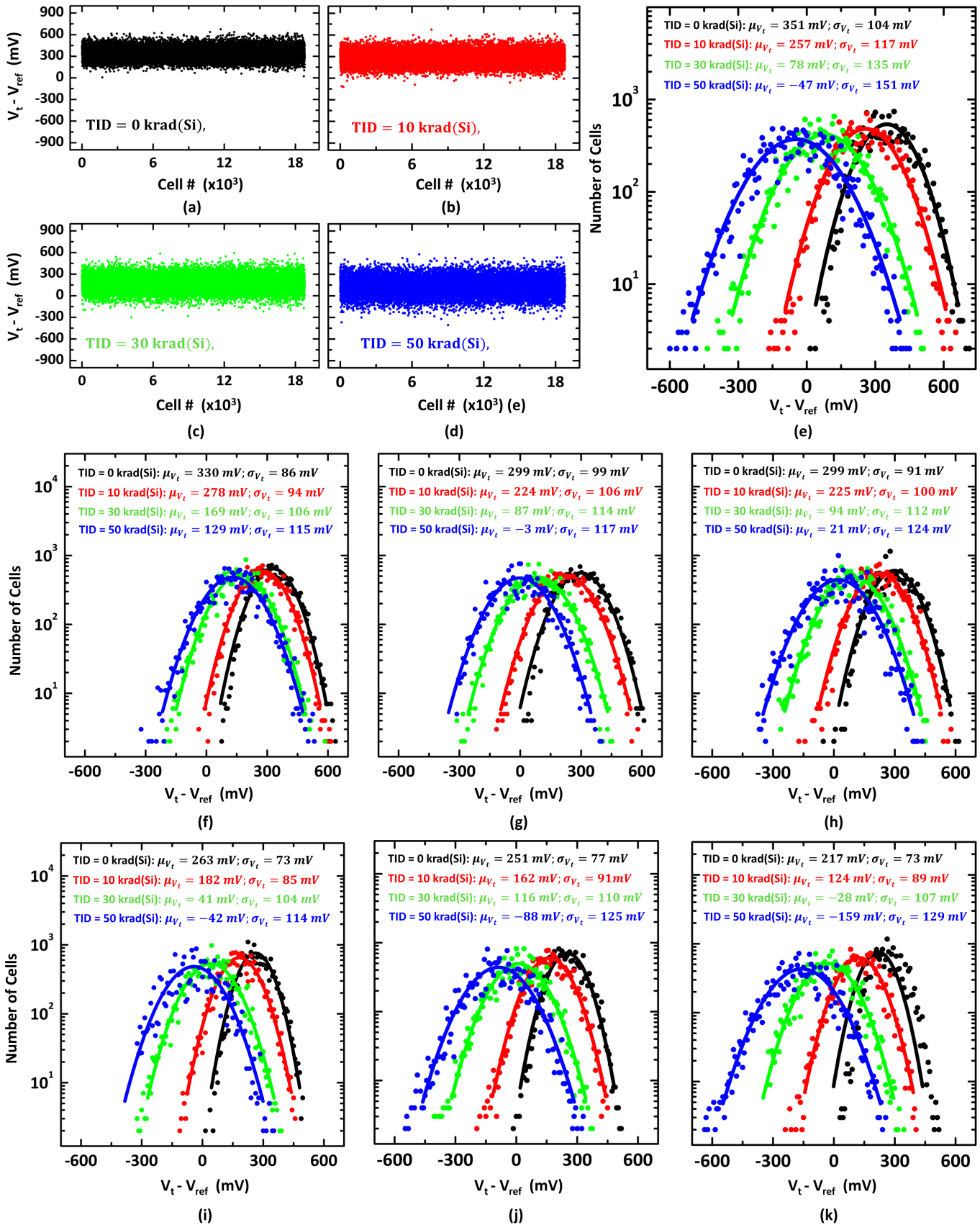

Fig. 3. (a)-(d) Cell by cell V_t values. (e) Distribution plot of V_t for different TID for the highest programmed state (L_7) in a memory page measured for different TID, with mean and standard deviation of the distributions indicated. (f)-(k) Distribution plots of V_t of the remaining states (L_1-L_6) for different TID.

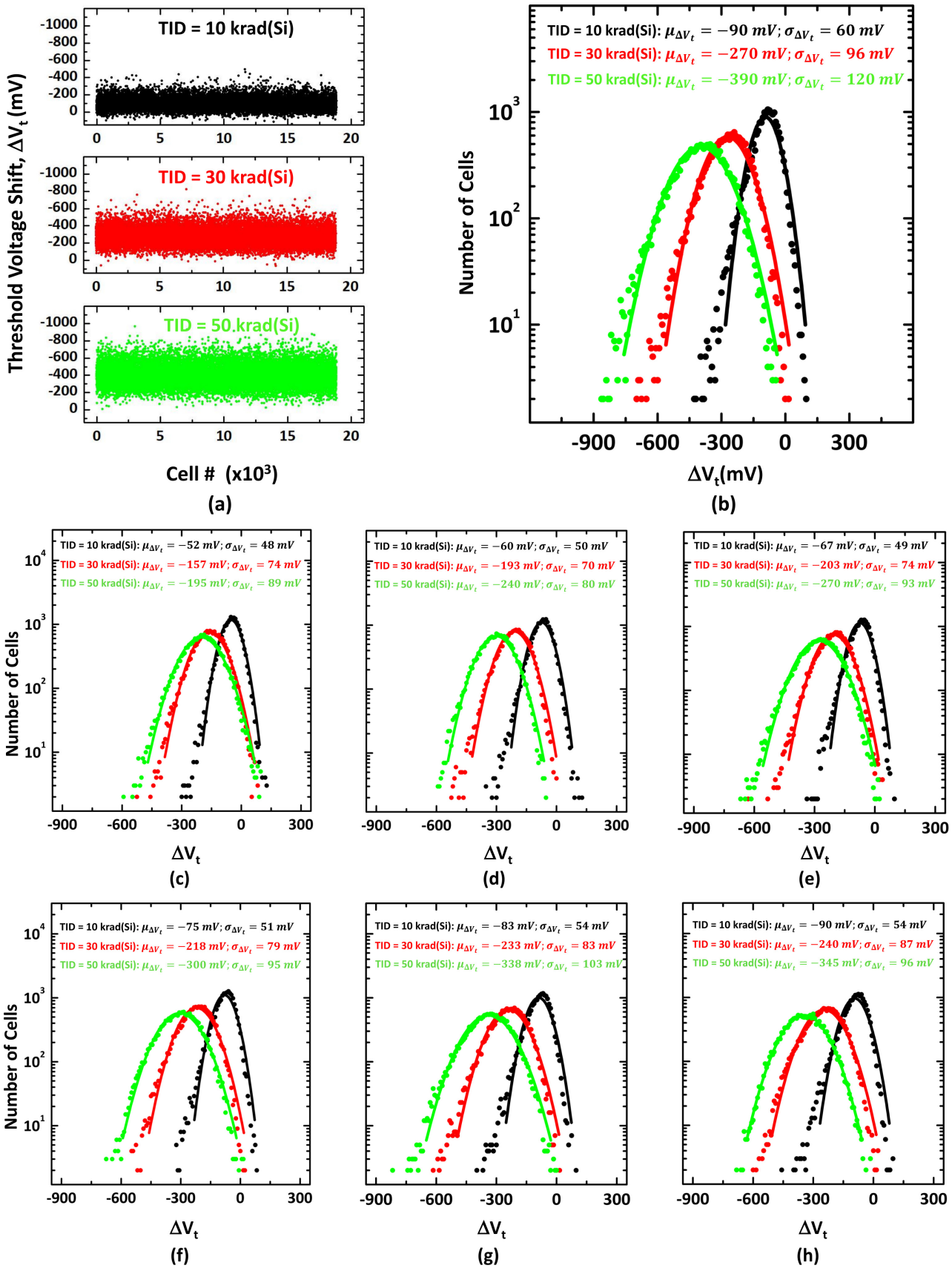

Fig. 4. (a) Cell by cell ΔV_t values. (b) Distribution plot of ΔV_t for different TID for the highest programmed state (L_7) in a memory page measured for different TID, with mean and standard deviation of the distributions indicated. (c)-(h) Distribution plots of ΔV_t of the remaining states (L_1-L_6) for different TID.

and seven different programmed states (L_1,..,L_7). We cannot measure the erased state (L_0) on the chip under test. Mean ΔV_t corresponding to the seven programmed states are shown in Fig. 5(a). It should be pointed out that (ΔV_t) is linear with TID for the highest programmed state (L_7) of the TLC memory. However, lower programmed states (for example, L_1) show saturating trend for TID values more than 30 krad(Si). In principle, we find that memory cells with higher V_t states experience larger V_t loss. This observation was also reported in the previous publications for earlier generations of memory chips [11]. Since electric field in the tunnel and blocking oxides of memory cells increases for higher V_t states, charge yield probability after irradiation is higher in the cells with higher initial V_t. Hence, higher programmed states experience larger V_t shift. Similarly, standard deviation associated with the ΔV_t distribution increases with TID as shown in Fig. 5(b).

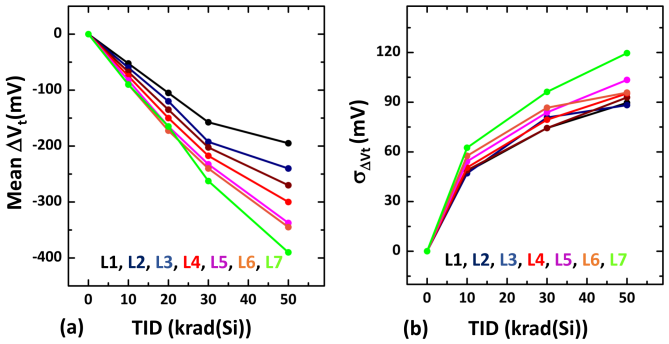

Fig. 5. (a) Mean ΔV_t for different programmed states plotted as a function of TID. (b) Standard deviation of ΔV_t corresponding to different programmed states as a function of TID.

IV. Conclusion

We conclude that both cell V_t and ΔV_t distributions downshift and widen with increasing TID. A significant variability exists in cell by cell V_t loss values even though all the cells are programmed to a particular state. V_t loss is dependent on the previous programmed states. Lower programmed states show a saturating trend for TID $>$ 30 krad(Si) while at the largest programmed state L_7, the V_t loss againts TID is almost linear (slope≈8mV/krad(Si)).

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