An Effective Sneak-Path Solution Based on Transient-Relaxation Device

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ABSTRACT

Efficient strategy for addressing individual devices is required to unveil the full potential of memristors for high-density memory and computing applications. Existing strategies using two-terminal selectors that are preferrable for compact integration have trade-offs in reduced generality or functional window. We propose a strategy that applies to broad memristors and maintains their full-range functional window. The strategy uses a type of unipolar switches featuring a transient relaxation or retention as the selector. The unidirectional current flow in the switch suppresses the sneak-path current, whereas the transient-relaxation window is exploited for bidirectional programming. A unipolar volatile memristor of ultralow switching voltage (*e.g.*, <100 mV), constructed from protein nanowire dielectric harvested from *Geobacter sulfurreducens*, is specifically employed as the exemplary switch to highlight the advantage and scalability in the strategy for array integration.

INTRODUCTION

Memristors or resistive switching devices have programmable conductance, which can emulate the state modulation in biological neural components.[1,2] Their two-terminal structure provides an easy way to arrange them in a crossbar architecture for compact and 3D-stackable integration.[3] Therefore, they are considered promising candidates for constructing high-density memory and efficient neuromorphic computing systems.[4-6] However, the precise selection of individual devices in the array for reading and programming operations requires the efficient suppression of current passing through other devices in unwanted routes or sneak paths.[7,8] The effectiveness and efficiency in addressing this sneak-path issue can determine important metrics such as integration density, complexity, error rate, and power consumption that are relevant to the practical scalability of the technology.[7,8]

The common practice is to associate each memristor with an addressing device that can serve as a switch to gate the current passage. Transistor is widely employed because of its switchable nature and technological maturity.[9-11] However, its three-terminal structure compromises the potential of a compact integration initially benefited from the two-terminal structure in memristors.[8] Alternative two-terminal addressing devices thus are actively sought. Diode can effectively suppress sneak-path current due to its excellent rectifying effect.[12-14] However, the unidirectional current flow has limited its use in addressing bipolar memristors, which constitute a big category preferred for assembling neuromorphic systems.[9-11] To accommodate bidirectional programmability, bipolar nonlinear devices such as tunneling barriers and threshold switching devices,[7,8,15-19] assisted with biasing themes such as V/2 and V/3 methods,[7] have been proposed as selectors to work with bipolar memristors. However, the activation voltages in these selectors are often close to the programming thresholds in memristors,[7,8] which can narrow the reading window or analogue input range and reduces the vector resolution for computation. A current-voltage (*I*-*V*) nonlinearity in the input range can be also introduced by the limited current density in some selectors,[7,8] preventing the direct use of voltage amplitude as the input for vector-matrix multiplication deemed efficient for computation.[7]

Overall, all these addressing devices can be classified as time-independent voltage devices because the selection function is solely based on the *I*-*V* curve. In contrast, the activation of some threshold switching devices involves temporal dynamics in addition (and correlated) to *I*-*V* behaviors.[19] Exploiting the switching dynamics in the time domain may create a new dimension for sneak-path solution. Recently, the delay dynamics in a bipolar volatile memristor was exploited to construct a timing selector.[20] The activation of this selector involved a delay inversely related to the input voltage amplitude. As a result, the selectors in the sneak paths, due to reduced voltage drop from the voltage-divider effect, experienced a longer delay than that in the selected path. This delay gap, during which the selector in the selected path was activated but those in the sneak paths were not, provided a time window for the selective reading and programming of the target device

cell. However, the distribution of the voltage drop across the selectors in the sneak path was heavily dependent on the array configuration. A mismatch between the numbers of wordlines (WLs) and bitlines (BLs) can cause the voltage to be dominantly dropped across one selector in the sneak path, with the value approaching that in the selected path.[20] This will then deplete the time window for the selective reading/programming and thus restrict the strategy from general applicability. In addition, like other selectors, the activation voltage still narrows the reading/input window in the amplitude domain.

Here, we show an effective sneak-path solution without above associated limits. The strategy relies on the unidirectional current flow in a unipolar switch to suppress sneak-path current. The transient relaxation (*i.e.*, conduction retention after the removal of activation voltage) in the switch is exploited to realize the bidirectional programming. Because the switch does not consume voltage drop in the relaxation window, the full-range input can be used by the programmable array for analogue computation. A unipolar volatile memristor of ultralow switching voltage (*e.g.*, <100 mV) is specifically employed as the exemplary device to highlight the advantage and scalability in the strategy for array integration.

RESULTS

General concept of the addressing strategy

We use the sneak path in a 2×2 array, which is the constituent unit for other sneak paths, to illustrate the general working principle in the proposed strategy (Fig. 1a). The key properties of the addressing device (switch) are that it has 1) unipolar switching or rectification and 2) a transient relaxation or retention after the activation voltage is removed (Fig. 1b).

During the selective programming, a positive activation voltage ($V_{activation}$) is first applied to open the switch in the selected route whereas all the switches in the sneak path remain closed due to current blockage by a reversely biased switch (Fig. 1c-i; Fig. S1). Then a SET (V_{set}) or RESET (V_{reset}) programming pulse is applied (Fig. 1c-ii). Since the switch remains open due to the transient retention, V_{set} or V_{reset} can be applied to the associated programmable memristor. For the applied positive V_{set}, one switch in the sneak path is under reverse bias (red cross). For the applied negative V_{reset}, two switches in the sneak-path current are under reverse bias (blue crosses). Together, it enables the bidirectional programming in the selected memristor, whereas the sneak path current is always suppressed to prevent state alteration in the unselected memristors. Substituting V_{set} or V_{reset} with a lower-amplitude voltage (V_{read}) yields a reading operation in the selected memristor without incurring the sneak-path current as well. Importantly, V_{read} can mostly apply across the programmable memristor if the activated switch has low resistance, preserving its full value to be utilized for analogue computation (which is unattainable in previous threshold selectors[7,8]). The selected switch spontaneously closes after the programming/reading operation (Fig. 1c-iii). Since the sneak paths in a larger array are effectively constituted from individual 2×2 paths, this addressing strategy leads to a general solution to the sneak-path issue independent of array

dimension. We may also term the switch as a transient selector as the strategy relies on the transient relaxation/retention in the switch for selective addressing.

A bio-amplitude volatile memristor for the transient selector

A unipolar volatile memristor (VMR) can be a good candidate to serve as the transient selector, because the spontaneous rupture of the filament takes finite time and naturally yields a short retention after the removal of electrical input.[19,21] Based on the working principle described (Fig. 1), some additional properties are desired for improved performance. First, a reduced switching voltage in VMR broadens its applicability in various memristor/memory systems. Specifically, once the VMR is activated, unlike a diode that still consumes a fixed voltage, it will have a sudden decrease in resistance and shift its initial voltage drop ($V_{activation}$) mostly to the series programmable device. The state of the programable device can be unintentionally altered if $V_{activation}$ gets close to the programming regime. A reduced $V_{activation}$ thus improves the programming controllability and broadens the applicability with memristors of varied programming thresholds. Second, a low conductance in the closed state and a high conductance in the open state in the transient selector, corresponding to a large On/Off ratio in the VMR, are preferred to reduce the sneak-path current and improve driving current for the reading/programming operation, respectively.

We employed a VMR that has bio-amplitude switching voltage (*e.g.*, <100 mV) and a high On/Off ratio as the transient selector to demonstrate the proposed addressing strategy.[22] This bio-amplitude volatile memristor (BVMR) was fabricated from a thin film sandwiched between an asymmetric pair of Ag-Pd electrodes (Fig. 2a) to enable unidirectional Ag migration for unipolar switching. The thin film was assembled from ultrasmall protein nanowires (*e.g.*, 3-nm diameter) harvested from microbe *Geobacter sulfurreducens* (Fig. 2b).[23-25] These protein nanowires are designed to facilitate charge transfer and provide a catalytic effect to Ag-filament metallization for reduced switching voltage.[22,26]

Electrical characterizations in the BVMRs were carried out to reveal properties for working as the transient selector. First, *I-V* sweeps in both positive and negative regions were performed to show the unidirectional current flow or rectification effect needed for suppressing the sneak path current (Fig. 2c). In a typical forward sweep, the device switched to a On state at ~ 80 mV (Fig. 2d, red curve). In the reverse sweep in the negative region, however, the device remained in a Off state and the switching to On was suppressed (green curve). The Off resistance was ~ 300 MΩ, much higher than programmable resistance range in various memristors.[9-11] Together, the BVMR showed unipolar switching with a nonlinearity ~10^5 (*i.e.*, On/Off ratio) larger than values in typical tunneling selectors.[7,8] It also featured a transition (~0.5 mV/dec) sharper than other threshold switching devices.[19] The switching voltages showed a consistent distribution between 40-90 mV during a series of 500 *I-V* sweeps (Fig. 2e). Statistics from 100 different devices showed an average switching voltage of 67±11 mV (Fig. S2). The BVMR had sub-100 mV forming voltage close to the switching voltage (Fig. S3). This close-to-forming-free property is also desirable for

integration, because forming the pristine selector with large voltage can complicate or even fail the integration (*e.g.*, damage to other devices).[27] Second, pulse tests were performed to reveal the transient relaxation or retention key to the programming/reading operations (Fig. 2f). After the activation by a 100-mV pulse, the device remained in the On state (~1.5 mS) for ~300 ms after the removal of the 100-mV activation pulse (Fig. 2g, purple region). Statistics from 40 BVMRs showed an average retention ~238 ± 78 ms (Fig. 2h). This retention is attributed to the transient stability in the formed filament before its rupture,[21,22] which can be further affected by the input details.[28] Larger value in the compliance current, voltage amplitude, or pulse width yielded longer retention (Fig. S4), which is consistent with the expectation of a stronger filament from a growth mechanism.[28] The revealed retention time in the ms region and an On conductance in the mS region provide sufficient time and current budget for programming various memristors.

Integrated programmable cell

To demonstrate that we can harness the transient retention in the BVMR for bidirectional programming, we stacked the BVMR on a programmable nonvolatile memristor (non-MR) to form a 1-transient selector-1-memristor ($1S_{tr}1R$) structure (Fig. 3a). The non-MR was based on a Ta-HfO_2 system that is frequently employed for neuromorphic memristive systems.[9-11,29] A middle Pd layer served as the shared electrode, which can also prevent Ag in the BVMR from migrating to the Ta-HfO_2 device. This middle electrode was specifically addressed with a contact to facilitate the probing of state in each device (Fig. 3b).

We tested the programmability in the integrated $1S_{tr}1R$ cell. During a SET programming, a voltage pulse of 200 mV was first applied to activate the BVMR (Fig. 3c; Fig. S5). The activation was indicated by a current increase (~5 μA at t ~ 36 ms), because the total resistance in the cell transitioned from a high value dominated by the Off resistance of the BVMR to a lower value dominated by the Ta-HfO_2 device. The 200-mV amplitude ensured that the initial voltage drop across the BVMR was larger than its switching threshold to activate it but was still much lower than the programming threshold in the Ta-HfO_2 device[29] to not perturb its state after the activation of BVMR (Fig. S6). The activation pulse was followed by a SET programming pulse (100 μs, 1.2 V, at t ~ 150 ms) which largely dropped on the Ta-HfO_2 device. A subsequent 200-mV reading voltage revealed a stable low-resistance state (LRS, ~40 μA at t ~ 120 ms) compared to the initial high-resistance state (HRS, ~5 μA at t ~ 36 ms) in the cell, confirming the successful SET programming of the Ta-HfO_2 device. The RESET programming followed a similar procedure by starting with the activation of the BVMR with a 200-mV pulse (Fig. 3d). The current rise (~30 μA at t ~ 26 ms) indicated the activation of the BVMR, as well as a LRS in the Ta-HfO_2 device. It was followed by a RESET programming pulse (100 μs, -1 V, at t ~ 150 ms). The corresponding negative current ~ -60 μA indicated that the transient retention in the BVMR indeed enabled reverse current for programming. A subsequent 200-mV reading process revealed a HRS with decreased current of ~5 μA (at t ~ 120 ms), confirming the successful RESET programming of the Ta-HfO_2 device. Cell scaled to sub-micrometer size maintained the same programmability (Fig.

S7), showing the promise for high-density integration. The result is consistent with expectation because memristors with a filamentary mechanism were shown to scale down to sub-micrometer size.[22,29]

The programming speed in the integrated cell can be substantially improved by exploiting the amplitude-dependent switching dynamics in the BVMR devices. The average delay time in the BVMR devices reduced from 8.9±2.5 ms with a 100-mV input to 0.19±0.17 ms with a 500-mV input (Fig. S8a). This 500-mV input did not perturb the conductance in the Ta-HfO_2 memristor (Fig.S8b) and is below the programming thresholds in many other nonvolatile memristors.[7] Therefore, a 500-mV amplitude can fulfill the purpose of faster activation. Meanwhile, based on the filamentary mechanism, a reverse input may accelerate the breakage of the filament to shorten the retention time. The average retention time in the BVMR devices was reduced to 0.40±0.3 ms by applying a reverse pulse of -500 mV (Fig. S9a), which also did not perturb the state in the nonvolatile memristor (Fig.S9b). Therefore, a -500-mV reverse pulse can be employed after each programming for faster deactivation. Harnessing the above two processes together, the overall programming time in the integrated cell can be reduced to sub-millisecond (Fig. S10).

The continuous modulation of the conduction state in the integrated cell, which is important for implementing neuromorphic computing, was further investigated. This analogue programming was first demonstrated with *I-V* sweeps (Fig. 3e), in which the conduction state in the integrated cell was successfully modulated to different values by applying different compliance currents (I_{cc}).[29] An abrupt conductance jump in the sub-100 mV regime was always observed (inset), which corresponded to the activation of the BVMR. An increase in I_{cc} yielded the increased conductance in the programmed state (Fig. 3f). Applying I_{cc} to the pulse programming led to the continuous state modulation in the cell (Fig. 3g; Fig. S11), which serves as a means for weight adjustment in matrix-multiplication based computation.

The generality of the $1S_{tr}1R$ strategy was further demonstrated by integrating the BVMR with another type of non-MR (Ta-Ta_2O_5) that is also frequently employed for constructing neuromorphic systems.[30] The integrated $1S_{tr}1R$ cell showed successful programmability similar to that in the Ta-HfO_2 based cell (Fig. S12). The results suggest that the $1S_{tr}1R$ structure can be broadly applied to various memristors for constructing programmable cells.

Sneak-path analysis

With the successful validation of programmability in individual $1S_{tr}1R$ cells, we then implemented the cells in a crossbar array to evaluate the capability in addressing sneak-path issue. Without losing generality, we first performed analysis in a 2×2 array (Fig. 4a). Each cell in the array shared the same stacking structure as previous individual one (Fig. 3a). The middle Pd electrode was still used to assist probing individual device state during the process (Fig. 4a, inset). An amplifier circuit (gray) was designed to monitor the current passing through the sneak path (I_{sneak}). The unselected WL and BL were floated (*vs.* biased with V/2 or V/3)[7], which may simplify

the programming process. To consider the worst scenario during a reading process, the non-MRs along the sneak path were all programmed to LRS while the non-MR on the selected path was reset to HRS. Applied with 200 mV, the memristive state in the selected cell M1 was successfully read (~ 6 μA at t ~ 40 ms) after the BVMR was activated (red curve, Fig. 4b). In contrast, the sneak-path current (I_{sneak}) remained negligible (blue curve), because the unipolar BVMR in cell M4 was under reverse bias and maintained an Off state to suppress current passage.

Because of the current blockage in cell M4, a subsequent forward SET programming is expected to still yield negligible Off current in the sneak path. Thus, the voltage drop across each non-MR in the sneak path is also small. The collective effect can suppress state alteration in various non-MRs of different programming mechanisms (*e.g.*, driven by current, field, or combined effect). This analysis was confirmed in the test that the selected cell M1 was successfully programmed to a LRS without altering the states of the three cells (M2-M4) in the sneak path (Fig. 4c, #1→#2). The transient retention after the activation in the BVMR is expected to also allow a reserve RESET programming in selected M1, as was analyzed before (Fig. 3d). In contrast, because all the BVMRs in the sneak path are inactivated, the RESET pulse will yield two reverse-bias BVMRs (M2, M3) to prevent current and thus programming in the cells along the sneak path. This analysis was also confirmed in the test that the selected cell M1 was successfully reset to an HRS, whereas the rest three cells (M2-M4) in the sneak path maintained their initial states (Fig. 4c, #2→#3). Above RESET and SET programming in the selected cell was repeatedly performed without altering the states in unselected cells (Fig. S13), showing the reliability in selected programming. The reading errors were consistently below 0.015% for randomly assigned states in the array, as opposed to over 10% in most cases without the BVMR (Fig. S14).

Above analysis shows that the unipolar BVMR implemented in the proposed strategy effectively suppresses the sneak-path current for selected programming and reading. Since the sneak paths in a larger array are constituent from combinations of 2×2 paths, it suggests that the strategy will work effectively with general arrays. The Off resistance in the BVMR determines the sneak-path current level, which also means that its ratio to the upper-bound resistance in the non-MR will affect the size of scalability. For the Ta-HfO_2 non-MR used, our estimate showed that the read margin[31] maintained a value above 10 % with an array width $N > 10^5$ (Fig. 4d; Fig. S15).

Demonstration in an 8×8 programmable array

We then implemented the BVMR and strategy in an 8×8 array to show the general scalability (Fig. 5a). A peripheral multiplexing circuit was used to address selected WL and BL (Fig. 5a, Fig. S16), with the rest floated. All the Ta-HfO_2 memristors were reset to HRS initially (Fig. 5b). A pixeled cartoon character "Toad" made from 24×32 pixels by 10-level grayscales (0-9) was used as the targeting pattern to program (Fig. 5c). To demonstrate the reprogrammability in the array, the "Toad" image was divided into twelve 8×8 arrays (Fig. 5d), each of which was to be consecutively programmed with the same 8×8 memristor array. The grayscale (n) of the pixel was

converted to the reading current (I_{read}, at 200 mV) by I_{read} = 5+10×n. By using the same programming strategy employed in the 2×2 array (Fig. 4), the 8×8 array was consecutively programmed to twelve image components and restored an image close to the original one (Fig. 5e).

The quality of restoration was further evaluated by comparing the programmed state (dot) in each cell with the targeting value (dashed line, Fig. 5f). An average discrepancy ~2 μA was consistently shown in the series of twelve programming (Fig. 5g), which suggests that the discrepancy comes from the inherent stochasticity in memristors.[2]

DISCUSSION

The $1S_{tr}1R$ strategy proposed in the work provides an efficient and generic solution to address the sneak-path issue in two-terminal memristor network without previous constraints imposed by other selectors. For example, the threshold (V_{th}) in previous two-terminal selectors reduces the input (V_{in}) effectively to (V_{in}-V_{th}) and narrows the input window,[7,8] which then reduces the vector resolution for analogue computation. Transistor, as the device to enable full-range input, is less compatible to the two-terminal memristor structure for unveiling the full potential of compact integration.[8] The $1S_{tr}1R$ strategy operates in a transient retention window that does not need voltage support, it thus can harness the full amplitude of V_{in} for computation. Together, the strategy attains the combined merits in enabling 1) two-terminal structure in the programmable cell for compact integration, 2) bidirectional programming suited for various memory and neuromorphic systems, and 3) full-range analog input desirable for vector-matrix multiplication.

Filamentary VMR has a relaxation period associated with the rupture of the conducting filament,[19,21] naturally providing a transient retention window fitting into the proposed strategy. We therefore have employed a filamentary VMR and successfully demonstrated the feasibility for scalable integration. Among the different VMR candidates that may work for the strategy, the BVMR with ultralow switching voltage[22,23] contributes additional benefits for the broad applicability. Specifically, the switching voltage (*e.g.*, < 100 mV) in the BVMR is far below the programming threshold (*e.g.*, >0.5 V) in almost all existing non-MR,[32] making the current addressing strategy applicable in various systems. Similar to other VMR-based architectures,[19,20,33,34] the stochasticity intrinsic to the filamentary switching nature can put constraint on the long-term reliability. Improving reliability in VMRs through material/device engineering or seeking other two-terminal volatile (*e.g.*, charge based) devices can further improve the strategy for better implementation.

METHODS

Protein nanowire synthesis. The protein nanowires were harvested from *G. sulfurreducens* using method described previously.[35,36] Harvested nanowire preparations were dialyzed against deionized water to remove the buffer and stored at 4 °C.

Device fabrication. A silicon wafer covered with 600-nm thermal oxide (Nova Electronic Mater., Inc.) was used as the substrate. For the fabrication of the programmable cell/array, the bottom electrode (Ti/Pd, 3/22 nm) was defined by standard lithography, metal deposition, and lift-off processes. A 5-nm-thick HfO_2 dielectric layer was deposited by atomic layer deposition (ALD) at 250 °C. The middle electrode (Ta/Pd, 20/20 nm) was defined by lithographic fabrication similar to that of the bottom electrode. These steps defined the Ta-HfO_2 memristor. To stack the BVMR, another 5-nm-thick HfO_2 dielectric layer was deposited on top of the Ta-HfO_2 device by ALD (a 5-nm-thick Ta_2O_5 was deposited by a sputtering instead for the Ta-Ta_2O_5 based programmable cell in Fig. S12). A top electrode (Ti/Ag/Pd, 3/150/20 nm) was defined by lithographic fabrication similar to that of the bottom electrode. Reactive ion etching (RIE) was used to etch away HfO_2 outside the BVMR device region and expose the vertical edge of the device. Finally, the protein nanowire solution was drop-casted on the cell/array and dried at 80 °C. The Ag filament in the BVMR device forms at the interface between the protein nanowire film and the exposed HfO_2 vertical edge.[22]

Electrical measurements. The electrical measurements were performed in the ambient environment with a relative humidity ~45-50%. The *I–V* curves were measured by using a semiconductor parameter analyzer (Keysight B1500A). The sneak-path current was measured by using a home-built differential amplifier, which involved voltage followers constructed from LM358 (TI) and a differential amplifier constructed from AD620 (TI). A 100-Ω resistor was used to extract the current from the sneak path.

Material characterizations. The protein nanowires were imaged by using a transmission electron microscope (JEOL JEM2000FX). The optical device images were taken by an optical microscope (OLYMPUS MX61-F).

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Author contributions: T.F. and J.Y. conceived the project and designed experiments. T.F. and S.F. carried out experimental studies in device and circuit fabrication and measurement. L.S. prepared the protein nanowire solution. H.G helped in circuit testing. J.Y. and T.F. wrote the manuscript. All authors discussed the results and implications and commented on the manuscript.

Competing interests: The authors declare no competing interest.

Figure Legends

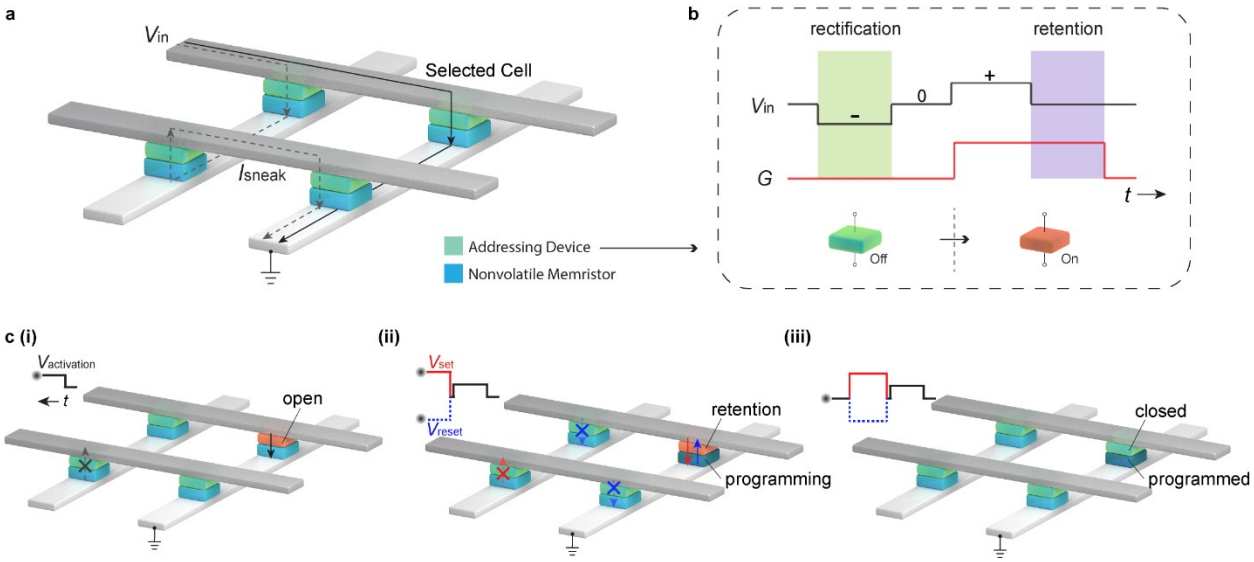

Figure 1. **General concept of the sneak-path solution based on the transient-relaxation dynamics of a unipolar switch**. **a**, Schematic of the selected path (solid line) and sneak path (dashed line) addressed between an input (V_{in}) and ground in a 2×2 array. **b**, Illustration of the general property of the addressing device (switch), with its conduction (G) maintaining an Off state under reverse bias (green region) and retaining an On state for some time (purple region) after the removal of the forward (activation) bias. **c**, Illustration of the programming scheme. (**i**) An input ($V_{activation}$) is first applied to turn On (orange) the switch in the selected path. Rest switches in the sneak path remain Off (green) due to the pinch-off switch (cross) under reverse bias. (**ii**) During the On retention (orange) in the selected switch, a subsequent programming voltage V_{set} or V_{reset} is directly applied to program the associated memristor (blue). Programming in the sneak path is suppressed because it has one pinch-off switch (red cross) or two pinch-off switches (blue cross) during V_{set} or V_{reset} operation, respectively. (**iii**) The selected memristor assumes a different state (dark blue) after the V_{set} or V_{reset} programming pulse. The associated switch returns to Off (green) after the transient retention.

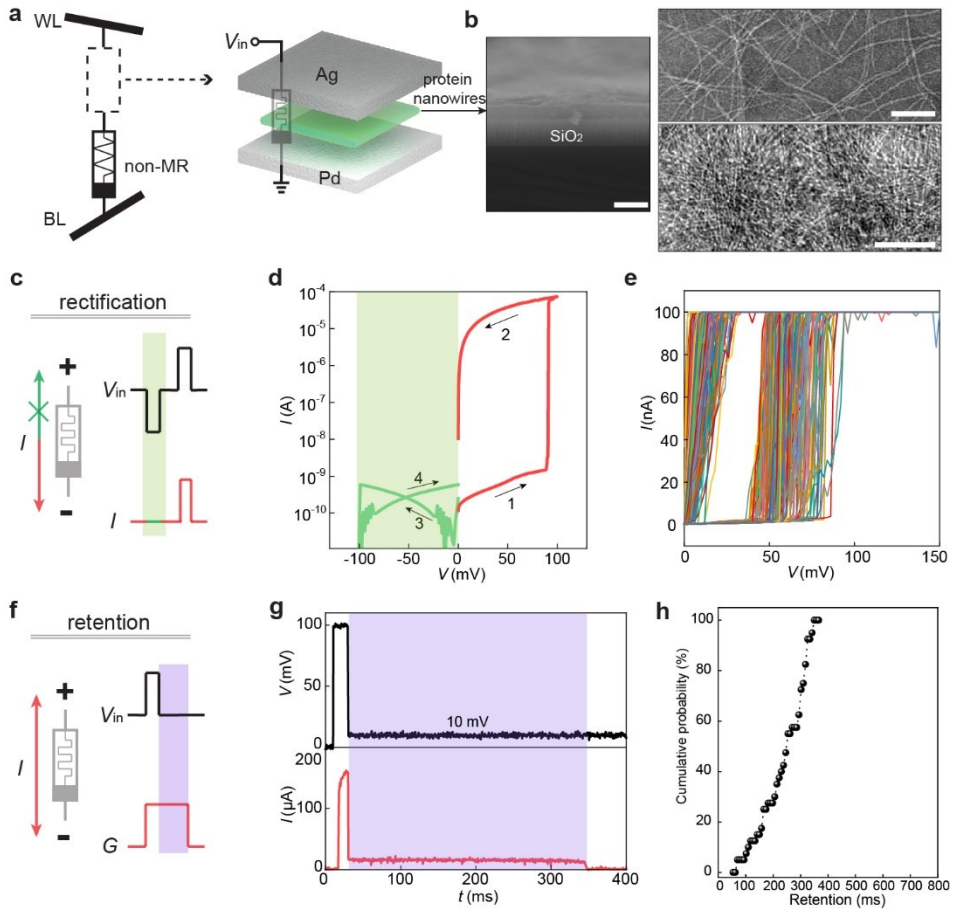

Figure 2. **Properties of BVMR devices**. **a**, The BVMR, with the general Ag-protein nanowires-Pd sandwich structure (right), is proposed to serve as the transient selector (left). **b**, (Left) Cross-sectional scanning electron microscope (SEM) image of the assembled protein nanowire thin film. Scale bar, 500 nm. (Right top) Transmission electron microscope (TEM) image of low-density protein nanowires. Scale bar, 100 nm. (Right bottom) TEM image of high-density protein nanowires, which can more closely represent the packing configuration in the actual assembled thin film. Scale bar, 100 nm. **c**, Schematic of the requirement of unidirectional current flow or rectification (green region) in the selector. **d**, Typical *I-V* sweeps in a BVMR featuring the unipolar switching property. The number and arrow indicate the sweeping order and direction, respectively. **e**, 500 continuous forward *I-V* sweeps in a BVMR. **f**, Schematic of the requirement of transient retention (purple region) and bidirectional conduction (red arrows) in the selector. **g**, A BVMR device showing transient retention (purple region) read by a sub-threshold (10 mV) voltage after the removal of the 100-mV activation pulse. **h**, Cumulative probability of the retention time obtained from 40 BVMR devices, with an average retention time of 238 ± 78 ms (± s.d.).

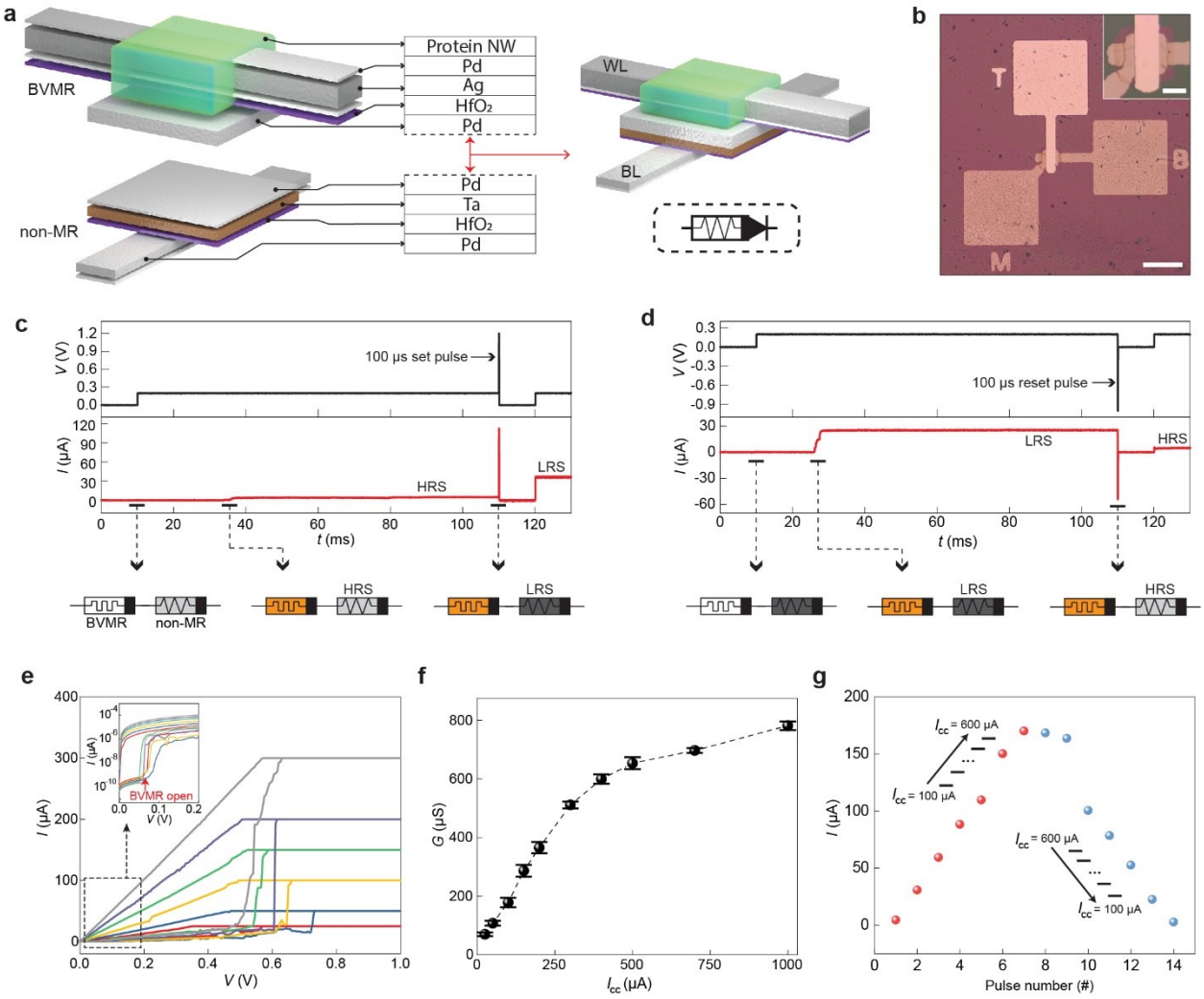

Figure 3. **Integrated cell and performance**. **a**, Structure of the integrated cell by stacking a BVMR device on a Ta-HfO_2 non-MR. A symbol (dashed enclosed area) is used to represent the integrated cell for convenience. **b**, An optical image of a fabricated cell having top (T), middle (M), and bottom (B) electrodes. Scale bar, 20 μm. The inset shows zoom-in active device region. Scale bar, 5 μm. **c**, A SET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR (orange), indicated by a current raise at t~35 ms. A subsequent programming pulse (1.2 V, 100 μs) sets the non-MR from a HRS (gray) to LRS (dark gray). The success of the SET programming is indicated by the increased current at t~120 ms by a 200-mV reading voltage. **d**, A RESET programming in the cell. A 200-mV pulse (100 ms) first activates the BVMR (orange), indicated by a current raise at t~26 ms. A subsequent programming pulse (-1 V, 100 μs) resets the non-MR from a LRS (dark gray) to HRS (gray). The success of the RESET programming is indicated by the decreased current at t~120 ms by a 200-mV reading voltage. **e**, I-V sweeps to program the cell to higher conduction state by applying increasing compliance currents (I_{cc}). The inset shows the activation processes in the BVMR device. **f**, Relationship between I_{cc} and programmed conductance (G) in the cell. **g**, Continuous modulation of the cell state by using pulse programming method shown in (c) and (d) with different I_{cc}. To reduce the conduction state (blue dot), a RESET process is first applied and followed by a SET process.

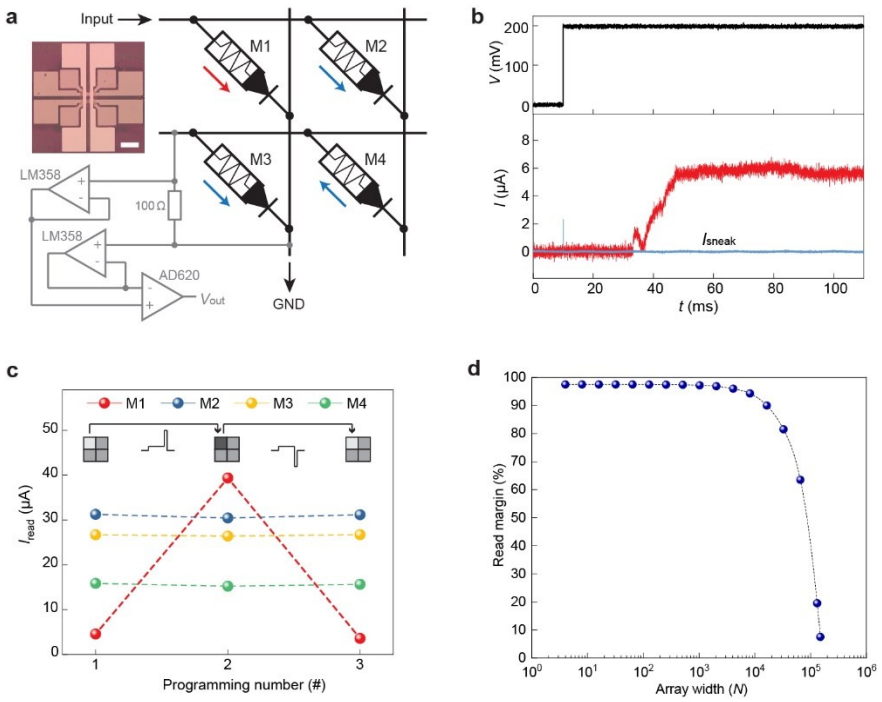

Figure 4. **Employment of the integrated cell for sneak-path analysis**. **a**, Circuit structure of a 2×2 array, with the red arrow and blue arrows indicating the selected path through cell (M1) and sneak path through other cells (M2-M4), respectively. A simplified symbol (see Fig. 3a) is used to represent the stacking cell. A differential amplifier circuit (gray) is used to measure the current in the sneak path. The inset shows the optical image of the array. Scale bar, 50 μm. **b**, In a worst scenario (*i.e.*, M2-M4 assuming LRS), the measured sneak-path current (blue) shows negligible value compared to the total current (red) between the selected WL (Input) and BL (GND). **c**, A consecutive HRS→ LRS→HRS programming in the target cell (M1) using pulse theme (Fig. 3c, d) does not alter the state in other cells (M2-M4). **d**, Estimated reading margin with different array sizes (N×N).

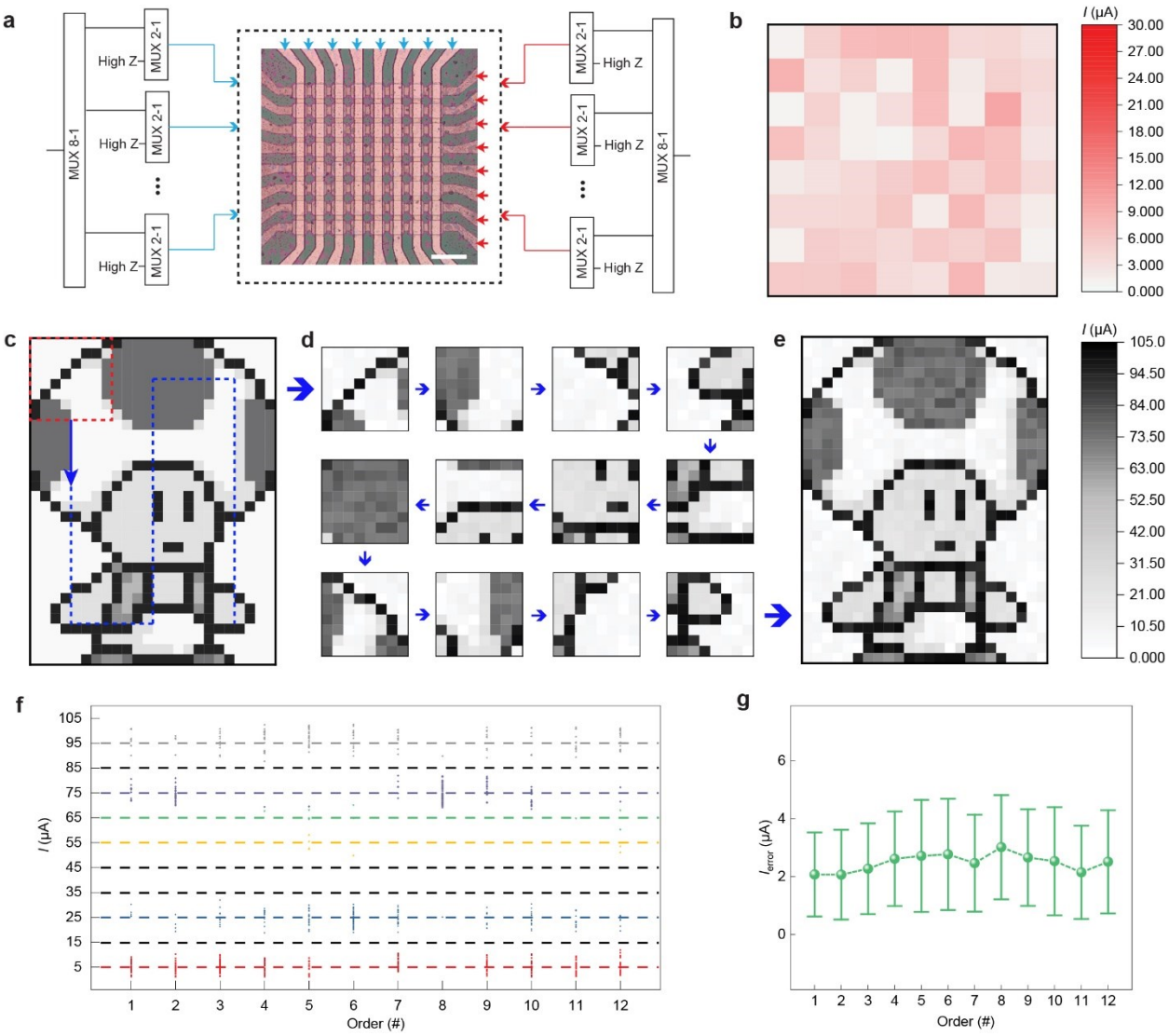

Figure 5. **Demonstration of programmable array**. **a**, An optical image of the 8×8 array, with the WLs and BLs addressed by a peripheral circuit. Scale bar, 50 μm. **b**, The initial HRS state in the cells of the array. **c**, The 24×32-pixel picture is divided into twelve 8×8-pixel arrays (red dashed box). **d**, The constituent twelve 8×8-pixel arrays following the sequence indicated by the blue-line path in (c). **e**, The reconstructed 24×32-pixel picture from the sequentially programmed 8×8 array. **f**, Comparison between the programmed value (dot) and targeting value (dashed line) in each cell during the 12 consecutive programming. **g**, The average reading error I_{read} (*i.e.*, the difference between programmed and targeting value) during the 12 consecutive programming. All the states are read by 200 mV.