An M-PSK Modulated Polar Transmitter Based on a Ring Oscillator with Low Power and Low Design Complexity for IoT Applications

Fariborz Lohrabi Pour, and Dong Sam Ha
Multifunctional Integrated Circuits and System (MICS) Group
Bradley Department of Electrical and Computer Engineering
Virginia Tech, Blacksburg, Virginia, 24061, USA
E-mail: {fariborzlp, ha} @vt.edu

***Abstract*—This paper proposes an M-PSK (M-ary Phase Shift Keying) polar transmitter, which features low power dissipation, low design complexity, and compact core size. The key blocks of the proposed transmitter are a ring oscillator and a charge control unit, which dynamically set the amount of charge to draw from the output node of the oscillator. The charge drawn from the output node effectively shifts the phase of the output voltage waveform of the oscillator. It enables the transmitter to perform the phase shift keying by controlling of the amount of the charge to draw. The transmitter is laid out in TSMC 180 nm CMOS process technology. Post layout simulations show that the transmitter can achieve the data rate of 40 Mbps with the error vector magnitude (EVM) of 3.7% for 16-PSK signals.**

***Index Terms*—Backscatter communication, Internet of Things (IoT), Modulation, Polar transmitter, PSK, Ring oscillator, Transmitter.**

I. Introduction

By rapidly growing the number of connected devices and nodes to the internet of things (IoT) network, there has been an increasing demand for compact, long range and low power with sufficiently high data rate designs targeting massive production of IoT gadgets [1]–[3]. This has motivated the researchers to introduce novel approaches to overcome the design challenges and pave the way toward responding the demands [4].

Fig. 1 represents the typical architecture of a self-sustainable IoT transmitter [5], [6]. The energy harvesting (EH) unit is responsible of providing a sufficient level of dc power for the μ-controller and the transmitter (TX) blocks to properly operate. The μ-controller programs the transmitter thorough the process of collecting information from the sensors and translate them into base-band (BB) signals. Finally, the BB signals are up-converted in the form of modulated signals and transmitted through the transmitting antenna. A battery is also adopted in the battery-assisted architecture that guaranties a continuous operation of the transmitter when the amount of the received power by EH block is not sufficient to supply the tag.

Several works have been introduced to improve the specifications of the transmitter such as communication range, power consumption, data rate and size [5]–[16]. Passive architectures offer design simplicity, ultra-low power dissipation with a moderate data rate [5]–[10]. The transmitter modulates the amplitude and phase of the received signal by adjusting the termination impedance. However, the structure introduces a considerable power loss due to their passive nature that limits the amplitude resolution of the modulated backscatter signal and hence, the data rate and communication range. Furthermore, the passive transmitters are unable to transmit at different frequency from the received signal. This can cause a self-jamming issue at the receiver or transmitter side and requires auxiliary circuits and additional power dissipation to suppress the jamming effect [17]. On the other hand, the active transmitters offer higher transmit power that makes them suitable for long range (LoRa) communication [13]–[15]. Moreover, they are able to transmit at a different frequency band from the received signal that alleviate the self-jamming issue presents in the passive architectures. The active transmitters mostly utilize frequency modulated (FM) signals to transmit the data that necessitates a stable frequency generator. However, the frequency drift free-running oscillators causes distortion in the transmitted signal and reduces the quality of the communication. Moreover, increasing the data rate requires higher frequency bandwidth that is not freely available in most of the dense frequency bands [18], [19]. It should be noted that this issue can be controlled and suppressed by employing a frequency control loop to stabilize the output frequency of the oscillator at the cost of more design complexity and power dissipation [20].

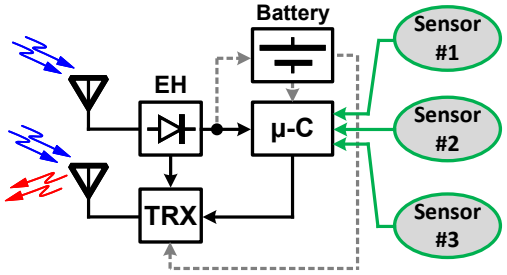


Fig. 1: Block diagram of a typical IoT tag.

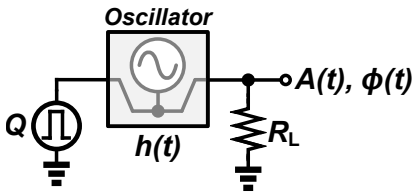
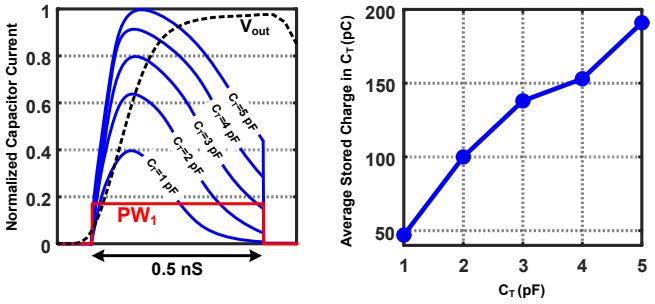


Fig. 2: Two port model of the oscillator.



(a) (b)

Fig. 3: (a) simulated current flowing into C_T, and (b) its corresponding stored charge.

In this paper, we propose a phase modulated (PM) transmitter architecture. It is composed of an oscillator along with an auxiliary control circuitry to draw a controlled amount of charge from a node in the signal path. Resultantly, the oscillation loop temporally changes the oscillation frequency that leads to a permanent shift in the phase of the output waveform. Therefore, the BB data can be transmitted using the phase modulated signals through a narrower frequency bandwidth. Further, the frequency drift of the free-running oscillator does not cause a significant error in transmitted signal, since it is negligible when translated to the oscillation phase.

This paper is organized as follows. Section II explains the preliminaries, describing the general linear time-varying analysis approach of the oscillator. Further it presents the design methodology of the transmitter, and Section III shows the post-layout simulation results. Finally, the paper is concluded in Section IV.

II. Design Methodology

In this section, we briefly discuss the charge to phase shift translation mechanism in the oscillator structure. We also present the detailed design methodology of the transmitter.

A. Preliminaries

Fig. 2 shows the two port model of an oscillator. The linear time-varying function of $h(t)$ describes the impulse response of the oscillator core. The input impulse charge of Q is injected to the output node of the oscillator, in the oscillation feedback loop. $A(t)$ and $\Phi(t)$ are the amplitude and phase response of the oscillator to the injected charge into the output port, respectively. However, due to the presence of the amplitude limiting mechanism in the oscillator structure, $A(t)$ will ultimately vanish and only a permanent phase shift of $\Phi(t)$ in the output waveform will remain [21]. The phase

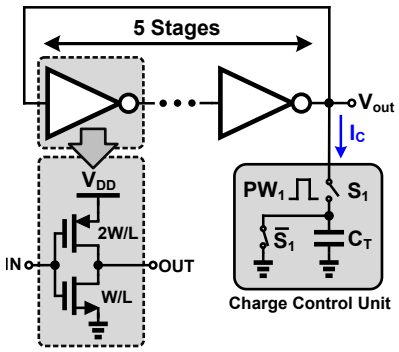


Fig. 4: Preliminary schematic of the transmitter.

response can be related to the excess injected current at the output using the following equation [22].

$$\Phi(t) = \int_{-\infty}^{t} h(\tau) i(\tau) d\tau \tag{1}$$

Equation (1) will be used in the next section to determine the relative phase shift in the output waveform of the oscillator and establish the foundation of the transmitter.

B. Transmitter Design

Fig. 4 shows the simplified schematic of the transmitter core. It is composed of a ring oscillator and a charge sinking circuit. Five inverter stages are cascaded to provide sufficient gain and phase shift in the feedback loop to satisfy the oscillation criteria [20]. The charge control unit is responsible for drawing a controlled amount of current from output node of the oscillator. The drawn current charges the capacitor through switch S_1, controlled by PW_1. Therefore, the amount of the charge can be adjusted by PW_1, and the capacitance value of C_T. However, utilizing variable capacitance is a more promising approach, due to the time varying nature of the oscillator, as will be discussed later in this section. Fig. 3 (a) shows the current flowing into C_T. The control pulse (PW_1) is applied at the rising edge of the output voltage V_{out}. It can be noticed that the amount of the current increases by the value of C_T, as long as the sinking current is not limited by the last inverter stage. The resultant charge stored in the capacitor corresponding to I_C is shown in Fig. 3 (b). It can be seen that the charge increases by increasing C_T, as expected from Fig. 3 (a). This indicates that the auxiliary charge control circuit is able to adjust the amount of the drawn charge from the output node of the oscillator, and hence can be exploited to the design of a variable phase oscillator.

In order to determine the impact of the drawn charge by C_T on the phase of the output waveform, the relationship between them must be studied. As it was discussed in Section II-A, the translation mechanism of I_C and the phase of the output waveform can be determined using (1). However, the impulse response $h(t)$ is required to be found for (1) to be used to calculate the amount of the phase shift.

Fig. 5 (a) shows the simulated $h(t)$ that represents the sensitivity of the output voltage to the injected/extracted current ($i(t)$). It can be seen that the voltage waveform is

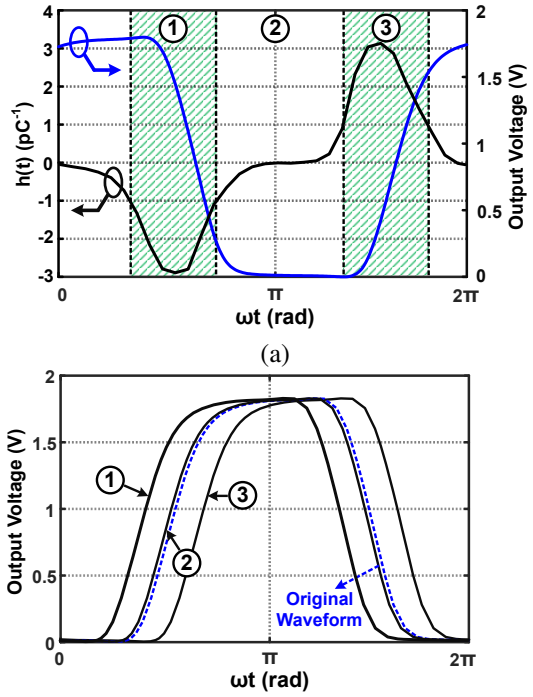


Fig. 5: Simulated (a) phase impulse response and its corresponding output voltage waveform of the oscillator, and (b) phase shift in the output voltage due to the extracted current at three different time windows.

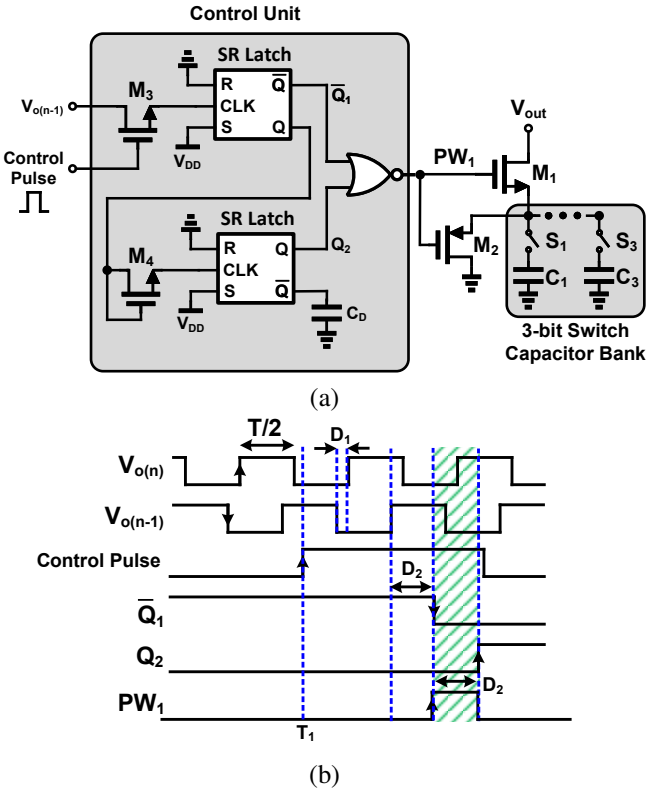


Fig. 6: (a) schematic of the charge control circuit (excluding the reset circuitry), and (b) its corresponding logic.

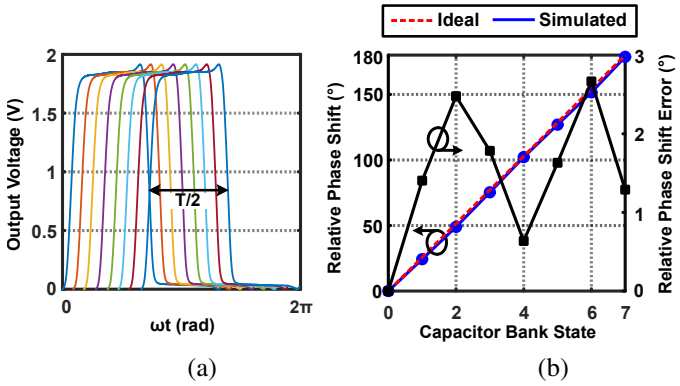
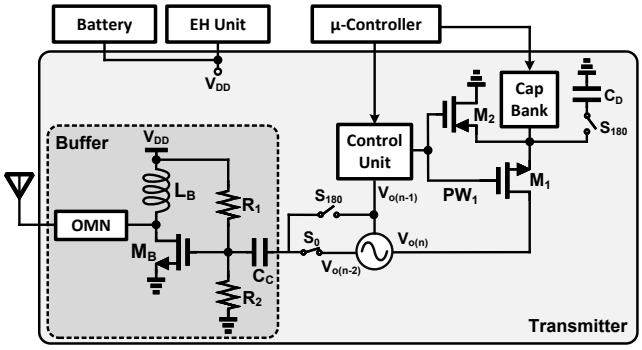


Fig. 7: (a) simulated time delay in the output waveform for 16 states of the capacitor bank, and (b) its corresponding relative phase shift.

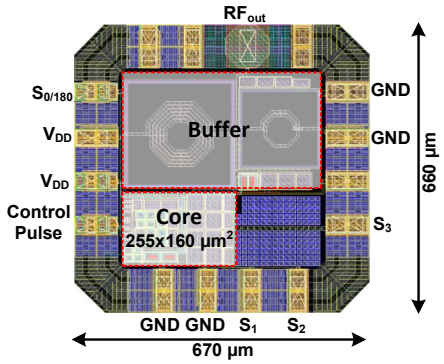
more sensitive to $i(t)$ around the rising and falling edges (hachured areas), while its sensitivity is negligible elsewhere in the voltage waveform. Fig. 5 (b) represents the impact of extracted current in different time windows in Fig. 5 (a). It can be seen that applying the control pulse (PW_1) in the flat areas of the voltage waveform causes a negligible phase shift in the waveform. On the other hand, sinking current in the areas near the rising and falling edges (i.e. ① and ③) has significant impact on the phase of the voltage waveform. Furthermore, sinking current at the rising and falling edges make a lagging and leading phase shift, respectively, corresponding to the sign of $h(t)$. Therefore, it is necessary to synchronize the applying time of PW_1 to desensitize the amount of phase shift to it.

The detailed design of the control circuit is shown in Fig. 6 (a) and its corresponding logic in Fig. 6 (b). $V_{o(n)}$ and $V_{o(n-1)}$ are the voltages at the output of n^{th} and $(n-1)^{th}$ stages, respectively, and D_1 represents the inverter delay time. The control pulse with an arbitrary width is applied at an arbitrary time (T_1). The switch M_3 connects $V_{o(n-1)}$ when the control pulse is applied that toggles the output of the latch at rising edge of $V_{o(n-1)}$. However, the change in the state of $\bar{Q}_1$ occurs with a delay equal to D_2. The complementary output of the latch then is fed into the second latch to toggle its output (Q_2). Finally, a NOR block creates a pulse with a width of D_2 when the output of the second lath toggles. Therefore, the pulse width of PW_1 is always remains constant and equal to D_2 that can be controlled by adjusting the delay of the latch blocks. Furthermore, it is independent from the applying time of the control pulse and its width as long as its width is longer that ($T = 1/f_{OSC}$). This relaxes the requirements of the μ-controller whose responsible of generating the pulse. As it can be seen in Fig. 6 (b), PW_1 spans around the rising edge of the output voltage waveform ($V_{o(n)}$). This maximizes the amount of phase shift due to the extracted charge from the output node of the oscillator, according to Fig. 5.

A 3-bit capacitor bank is adopted to tune the charging capacitance and hence, the amount of phase shift. Fig. 7 (a) shows the time domain output waveform of the oscillator for 8 states of the capacitor bank. Each individual bit is optimized to achieve the minimum the time delay error. The corresponding phase shift due to the drawn charge by the capacitor bank is shown in Fig. 7 (b). It can be seen that the maximum error



(a)



(b)

Fig. 8: (a) complete schematic of the transmitter, and (b) its layout.

of less than 3 degrees is obtained. This results in a relatively small value of error vector magnitude (EVM), as it will be discussed in the next section. This is important to relax the signal to noise ratio (SNR) requirement of the receiver in a wireless network [23]. It is also beneficial for improving the performance of the primary users in the wireless network [24].

III. Post-Layout Simulation Results

The complete schematic of the transmitter is shown in Fig. 8 (a). The switches S_0 and S_{180} are added to the schematic of Fig. 4 to double the phase shift range by switching between two complementary waveforms. Capacitor C_D is also added to compensate the delay of the inverter between the complementary nodes (D_1 in Fig. 6 (b)). The core oscillator is designed at the center frequency of 1 GHz. The buffer block is also designed to isolate the output of the oscillator from the antenna impedance. It should be noted that the buffer circuit can be eliminated according to the power budget of the tag.

The transmitter circuit is laid out in standard TSMC 180-nm CMOS process technology to consider for the parasitics of the active devices and interconnections, as shown in Fig. 8 (b). The core size is 0.04 mm^2 while the total size of the layout is 0.44 mm^2. The oscillator core dissipates a steady state dc power of 870 μW. Fig. 9 represents the simulated constellation diagram of the output RF signal for 16- phase shift keying (PSK) input BB signal. Assuming an ultra-low power μ-controller with an output clock frequency of 1 MHz, a data rate of 4 Mbps is obtained with an EVM of 3.7 %. In order to evaluate the performance of the transmitter and its sensitivity to the control

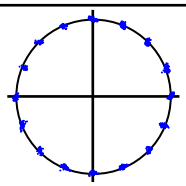
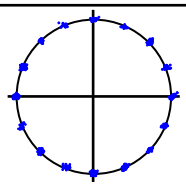
Clock Rate	1 MHz	10 MHz
Constellation		
Data Rate	4 Mbps	40 Mbps
EVM	3.7 %	3.7 %

Fig. 9: Simulated 16-PSK constellation diagram and its corresponding EVM for different μ-controller output clock frequency.

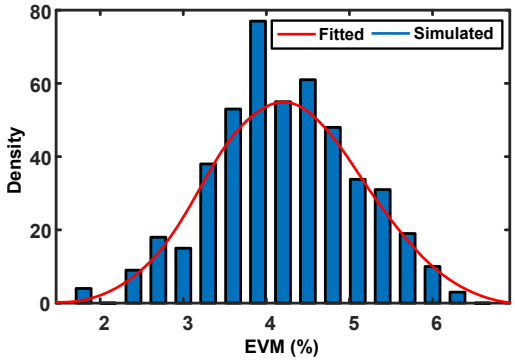


Fig. 10: Monte-Carlo simulation result for 16-PSK modulated signal and the clock rate of 10 MHz.

pulse [see Fig. 6], its frequency increased to 10 MHz. It can be seen that a data rate of 40 Mpbs is achieved while the EVM remains unchanged. This indicates the independency of the modulated signal to the width of the control pulse as it was discussed in Section II-B. The transmitter owes this feature to the fast settling time of the oscillator which is shorter than $3T$. This is beneficial for optimizing the maximum coverage distance by the users in a wireless network [25].

The Monte-Carlo simulation is also performed to investigate the impact of the device mismatches on the EVM performance. As it can be seen in Fig. 10, the EVM varies from 1.8 to 6.3% following a normal distribution with the standard deviation and mean of 1.1 and 4.2, respectively. Although the mismatch causes increasing in the EVM value, it is still satisfying for most of the applications.

IV. Conclusion

The design of a polar transmitter was described based on the LTV theory. In order to desensitize the amount of the drawn charge from the output node of the oscillator, a synchronizing circuit was designed. A 3-bit capacitor bank was also adopted to digitally control the time delay of the output waveform and hence, its corresponding phase shift. The transmitter circuit was laid out and post layout simulation results were performed that showed the capability of the transmitter to achieve a data rate of 40 Mbps with an EVM of 3.7 %.

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