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Novel Ka-Band Phase Shifter Design Based on Vanadium Dioxide Switches for 5G Applications

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***Abstract*—A novel design for a phase shifter at Ka-band on silicon and in coplanar wave guide (CPW) is presented. The proposed design incorporates a novel configuration of vanadium dioxide (VO_2) switches. A set of two shunt and two series VO_2 single pole single throw (SPST) switches are configured to be controlled via a single thermal actuator. The proposed design reduces the number of thermal actuators by a factor of four. Ultimately, the proposed design demonstrates a low maximum insertion loss of 6.5 dB with 32 selectable phase shifts and consistent phase response over the range of 37-40 GHz.**

I. Introduction

Phase shifters are an essential component of passive phased array antennas allowing for beam steering and beam shaping, among other applications. The proposed phase shifter design, shown in Fig. 1, is a CPW line length-based phase shifter. It uses switches to select between either a reference line or a longer line length to apply a relative phase shift.

To allow for multiple phase shifts, the design in Fig. 1 is cascaded as shown in Fig. 2. Each of the stages is referred to as a bit. The reference line length of each stage is equivalent, and each phase shift line length doubles throughout the cascade. The cascaded design can achieve any phase shift to within the resolution of the shortest phase shift line or smallest bit.

To minimize insertion loss, the phase shifter design utilizes VO_2-based switches. VO_2 is a thermally or electrically activated phase-change material that undergoes a large change in resistivity. This material has previously been demonstrated in low insertion loss switches in the mmWave band [1,2].

Lastly, the proposed design incorporates a novel configuration of both series and shunt versions of SPST VO_2 switches, as shown in Fig. 1, such that all four switches in a bit are controlled with a single thermal actuator.

II. Design Topology

The proposed design utilizes thermal actuation to change the resistivity of VO_2 and subsequently select which switches are open or closed. Typically, each switch would be designed with its own DC heater circuit to generate the heat inducing the phase transition. However, in the proposed design, only one heater circuit is used to manipulate four SPST switches simultaneously. Subsequently, the heater circuit is physically distanced from any individual switch. The separation distance reduces the parasitic capacitance from the heater that would otherwise degrade switch performance.

The single bit design topology is shown schematically in Fig. 3 illustrating the two states created by the thermal actuator. When all four switches are heated simultaneously, the path that applies a relative phase shift is selected. When the heater circuit is not active (cold switches), the reference path is selected.

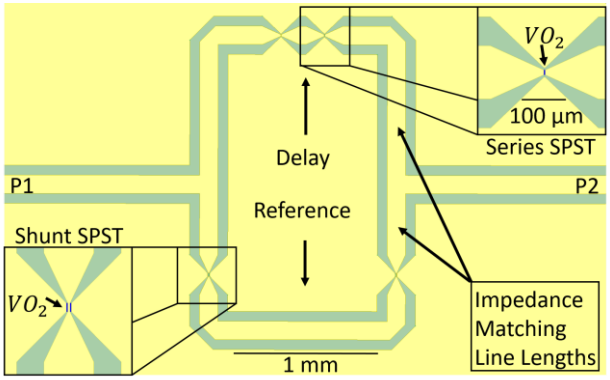

Fig. 1. A single bit in the novel vanadium dioxide switch-based phase shifter. Either the top or bottom path will pass the RF signal, with the top path imparting 11.25° of additional phase delay relative to the bottom. All switches are designed to be controlled by a single thermal actuator.

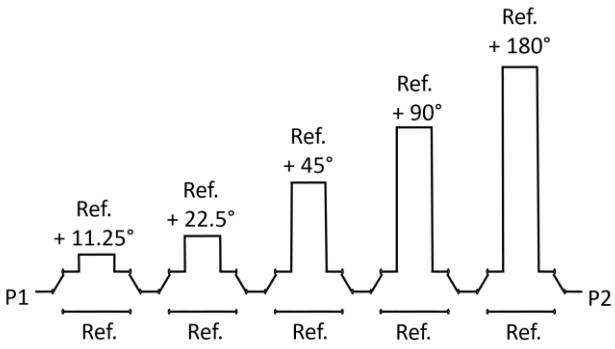

Fig. 2. Schematic diagram of the proposed phase shifter design, with five bits cascaded in series.

The phase shifter bit performance is optimal when the switches are placed such that the input impedance looking into the unused path is as near to an open circuit as possible. Subsequently, additional transmission line lengths are used to adjust the impedance seen at the junctions in Fig. 1.

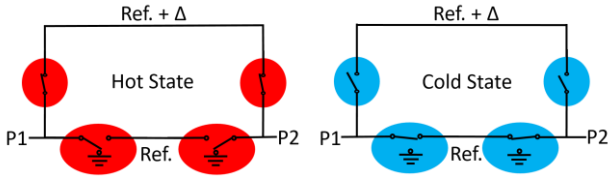

Fig. 3. By utilizing both series SPST (through or open) and shunt SPST (through or shunt GND), the thermal activation of all of the switches necessary for bit selection is controlled via a single thermal source.

Both the series and shunt SPST switches shown in Fig. 1 were designed for fabrication on a high resistivity silicon substrate for enhanced integration potential. Additionally, a thin layer of alumina is incorporated to enhance the lattice and properties of the VO_2 as demonstrated previously in our group [3].

III. Results

Each switch design was modeled and refined using full wave simulations in Ansys HFSS. Switch performance was generally optimized by maintaining 50 Ω CPW and minimizing VO_2 geometry. Scattering parameters for both states of the two switches were exported from HFSS and imported into Keysight ADS. A circuit diagram for each bit was created utilizing the scattering parameters and ideal transmission lines.

The insertion loss associated with each bit in the phase shifter is shown in Fig. 4. With the maximum phase shift selected, the maximum insertion loss for the phase shifter is 6.5 dB. The value for maximum insertion loss is consistent to within 0.5 dB throughout the operational bandwidth.

The phase shift from each bit's delay line, relative to each bit's reference line, is shown in Fig. 5. Each bit's relative phase shift is accurate to within ±3.5° of its intended phase shift, across the 37-40 GHz band. This error is less than the smallest bit phase shift of 11.25°.

The 5-bit phase shifter design demonstrates a 55°/dB figure of merit over the range of 37-40 GHz. This is comparable with current state-of-the-art phase shifter technology summarized in Table 1.

We have presented a low loss and high figure of merit phase shifter design. The design incorporates a novel configuration of VO_2 switches that reduces the number of required thermal actuators by a factor of four. A complete design, simulation, fabrication, and measurement results will be presented at the conference.

TABLE I. COMPARISION OF THE PHASE SHIFTER PERFORMANCE OVER INSERTION LOSS BETWEEN THIS WORK AND THE LITERATURE.

Reference	Technology	Frequency (GHz)	Figure of Merit (°/dB)
This Work	VO_2	37-40	55
[4]	GeTe	26-34	36.8
[5]	Liquid Crystal	20-40	6.3
[6]	RF MEMS	27-33	46.8
[7]	65 nm CMOS	20-30	26.7
[8]	RF MEMS	10-35	85.7
[9]	250 nm SiGe	10-50	4.4
[10]	RF MEMS	dc-40	100
[11]	180 nm SiGe	28-40	24.6

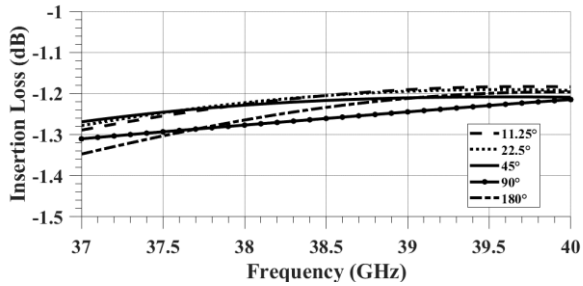

Fig. 4. Insertion loss for each of the five bits in the phase shifter design.

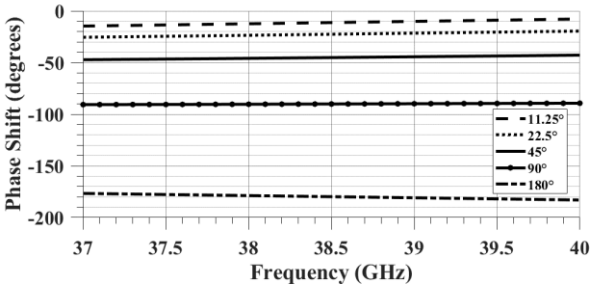

Fig. 5. Phase delay for each of the five bits in the phase shifter design.

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