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Gate Driver Circuits With Discrete Components For GaN-based Multi-Level Multi-Inductor Hybrid Converter

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***Abstract*—Gate driver circuits to ensure proper turn-on and turn-off for power switches are essential parts of a power converter design. They become significantly challenging for multilevel converters where multiple switches are operated at active voltage domains. Recent favorable use of Gallium-Nitride (GaN) devices for power switches makes gate driving even more difficult as the switch performance and reliability are very sensitive to variations of the gate driving signals and power rails compared with traditional power MOSFETs. This paper discusses gate driving methods using a multi-level multi-inductor hybrid (MIH) converter as the demonstration prototype to address two key challenges in designing gate drivers: 1) providing level-shifted PWM signals to active voltage domains and 2) powering schemes for gate driver circuits. To solve the first challenge, an optimal use of available half-bridge drivers is proposed to eliminate the need for separate signal isolator chips. This method was implemented and verified in a MIH converter prototype for 48-V Point-of-Load (PoL) applications using three different powering schemes for gate drivers, including isolated power modules, regulated supplies from switch blocking voltages, and cascaded bootstrap power rails with regulations. The gate driver techniques and powering schemes are compared experimentally in terms of performance to illustrate their benefits and trade-offs.**

I. Introduction

Multilevel hybrid DC-DC converters have made significant contributions to bolster the recent rapid expansion of power electronics impact. Their successful integration in power supply for high-performance computing, automotive applications, space devices, and domestic appliances, etc., has paved the path for a long-term strong establishment in the field. Particularly, they emerge as the most appealing candidate for non-isolated Point-of-Load (PoL) converters in data centers and telecommunications systems. Recently, a number of different multi-level hybrid converters have been demonstrated for this application where moderate to extreme step-up or step-down conversions are necessary, for example, 48V-to-12V [1]–[4], and 48V-to-1.8V [5]–[14], etc. These converters have been demonstrated with resonant operations for highly-efficient fixed conversion ratios [1]–[3], [5], [6] or regulated output operations with pulse-width modulation (PWM) duty cycle control [4], [7]–[10], [12]–[14]. With superior performance over conventional Buck converters, these hybrid converters promise significant improvement of the overall system efficiency and power density.

Despite their clear advantages in power conversion, their market penetration is still hindered with the concerns over a number of design challenges, especially gate drivers for a relatively large number of stacked power switches. The designs of these hybrid DC-DC converters share a common characteristic that they utilize more switches and passive components to reduce voltage stress on them individually. The lower voltage stress enables the use of devices with lower voltage ratings and higher density for higher system efficiency and smaller overall space. However, a large number of power switches means a challenge in the increased complexity of gate drivers. To make it worse, many power switches in these multi-level hybrid converters are operated at different voltage domains and shifted levels.

Figure 1 depicts a Multi inductor hybrid (MIH) converter [15], [16] as an example of multilevel hybrid converters, utilizing 12 switches, $Sw_{1\text{-}12}$. This converter can be operated in multiple ways with different operating numbers of inductor energizing phases. Fig. 1a and Fig. 1b show the configurations for 2 phases and 6 phases respectively. In this converter, switches $Sw_{7\text{-}12}$ are operated at the ground level, i.e. their Source terminals are connected to the ground, while the other 6 switches, $Sw_{1\text{-}6}$ are stacked on top switch Sw_7. Although there are various types of multilevel converters, such as duty cycle controlled flying capacitor multi-level (FCML) hybrid converters [7], [17], [18] and multi-phase multi-inductor hybrid (MIH) converters [10]–[15], [19], and a broad variety of resonant or hybrid switched converters [1]–[3], [6], [20], [21], the stacked switch structure similar to $Sw_{1\text{-}7}$ in Fig. 1 is common in these converter families. The ground switches $Sw_{7\text{-}12}$ are relatively straightforward to drive, but it is challenging to drive the six stacked switches $Sw_{1\text{-}6}$ while satisfying reliability and performance across all operating points. The most fundamental stacked switch configuration is a half-bridge. Since gate driver integrated circuits (gate driver ICs) are often intended for only one single switch or two half-bridge switches, there is no single gate driver IC product that can drive a large number of stacked switches in multilevel converters.

This paper presents an optimal use of half-bridge drivers that takes advantage of built-in signal isolators in Section II. In Section III, a review of traditional and discussion of new schemes to generate power rails for the multi-level converter

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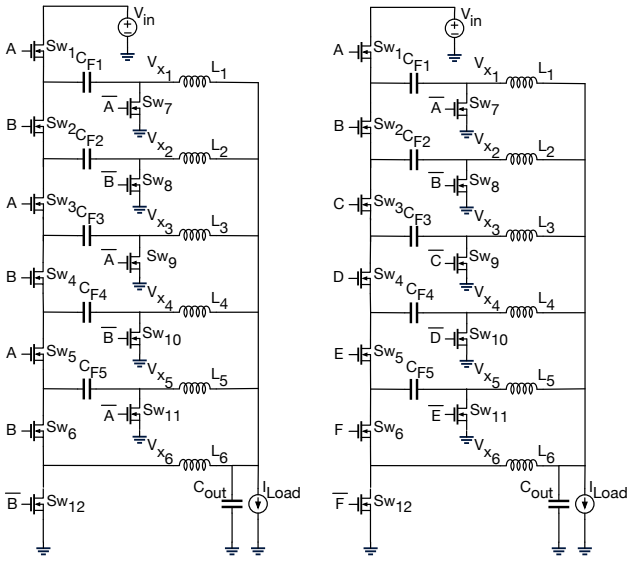

(a) 2-phase (b) 6-phase in ADBECF sequence

Fig. 1: Multilevel hybrid converter example: 6-level MIH converter

are provided. Section IV presents experimental results and verifications of the circuits presented in Section II and III. The paper is finally summarized and concluded in Section V.

II. Optimal use of half-bridge drivers

There are a number of techniques known for powering flying drivers, whose voltage domains are switched in normal operations of converters, some of which will be covered in Section III. However, techniques to level-shift control signals from the ground level to appropriate flying voltage domains using discrete components can still benefit from further improvements for a smaller discrete component count and space. Commercial signal isolators rely on inductive or capacitive couplings to convey control signals to different voltage levels [22], [23]. Because of the relatively large passives required for isolated coupling and the nature of being discrete components, signal isolator ICs are often area-consuming and can be even larger than the switches that they are driving. This is a common problem in many power converters that have multiple synchronous power switches such as multi-level converters. In addition, these isolators can also add significant delays to the critical signal path, leading to more complex timing control. It is, therefore, desirable to minimize the number of signal isolator ICs required in converter design.

It is widely known that typical commercial half-bridge driver ICs have a built-in capacitive signal isolator. This half-bridge driver is usually used to drive a half-bridge switch pair where the top driver drives the switch that is stacked immediately on top of the one driven by the bottom driver [1], [18], [24], [25]. However, it is much less recognized that the built-in signal isolator in a half-bridge driver is capable of a large voltage difference and can actually be used in place of a signal isolator. Utilizing this built-in capability can optimize half-bridge gate driver functionality and eliminate the need for all discrete signal isolators in multilevel hybrid converters.

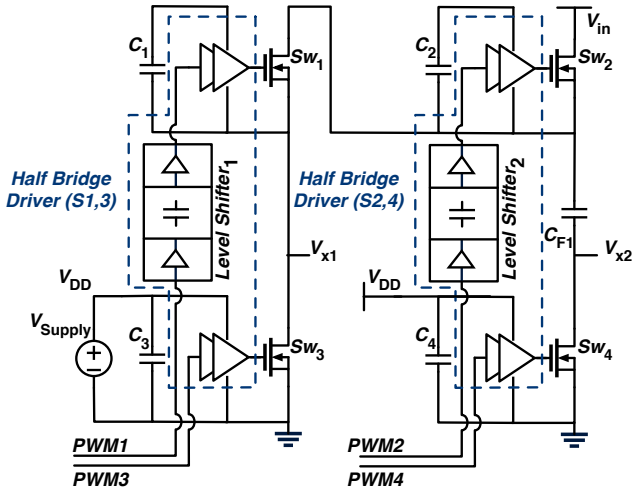

Fig. 2: Optimal use of half bridge drivers with integrated signal isolators.

Figure 2 depicts the switched capacitor (SC) part of a Series Capacitor Buck Converter (SCBC) [19] as an example where half-bridge driver ICs and their built-in signal isolators are proposed to be used in a new configuration to remove the need for discrete signal isolators. The power converter architecture has 4 switches in Fig. 3a, two of them, Sw_1 and Sw_2 are stacked on a ground-level switch Sw_3. Switch Sw_4 is at the ground level and operated in a complementary phase to Sw_2. Flying capacitor C_{F1} connects switch Sw_4 to Sw_1, Sw_2 and the rest of the circuit.

In this power converter, directly stacked switches Sw_1 and Sw_3 can be driven by a half-bridge driver IC. As switches Sw_2 and Sw_4 do not share a common switching node as in usual half-bridge switch pairs, they may not immediately appear to be controllable by a single half-bridge driver IC. However, the power-transfer capacitor C_{F1} connecting them acts as a DC voltage source in operation transient, ensuring that their operation is logically complementary in the same manner of a half-bridge switch pair with a DC voltage separation equivalent to the voltage across C_{F1}, $V_{C_{F1}}$. Recognizing that the signal isolator built in a half-bridge driver IC is capable of this voltage separation, only one driver IC is utilized to drive Sw_2 and Sw_4 Particularly, the built-in signal isolator can bring the gate control signal up for Sw_2 while the high-side driver for Sw_2 can operate at a $V_{C_{F1}}$ from the ground. This proposed method results in more optimal utilization of gate driver IC and removes the need for an additional signal isolator that would have been needed for Sw_2 in the traditional solution [24].

It is worth noting that the example circuits in Fig. 2 represents the lowest 2 levels of the SC stage in an N-level SCBC, where N can be a number greater than 2 [12], [14], [15]. This optimal use of half-bridge drivers can be extended to drive all other high-side switches in the stack in multi-level hybrid converters [10]–[12], [15], [26].

III. Power rail generation

Together with the new optimal half-bridge driver scheme presented in Section II, it is important to devise appropriate

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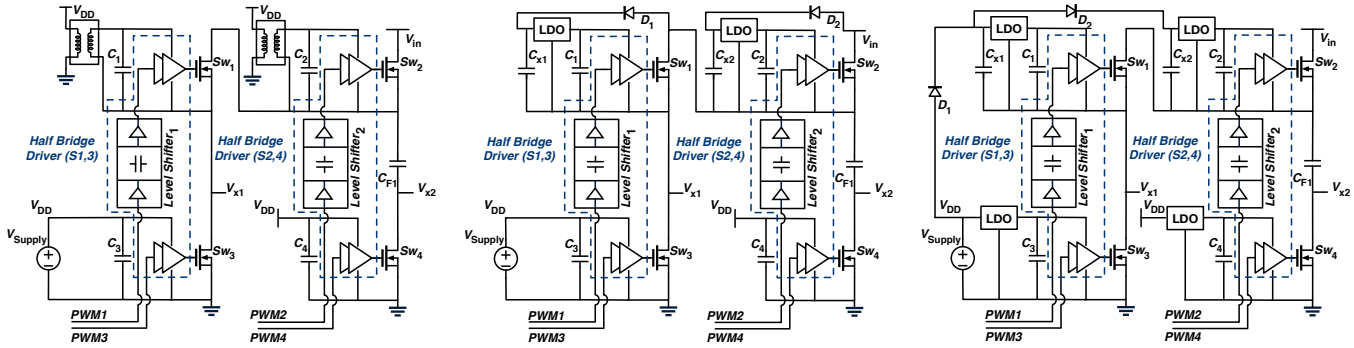

(a) Isolated modules (b) Regulated supplies from switch blocking voltages (c) Regulated supplies from cascaded bootstrap

Fig. 3: Optimal use of half-bridge drivers in multilevel hybrid converter with different powering schemes

methods to power high-side gate drivers operated at different voltage domains. There are many methods to achieve this goal as also presented in the comprehensive review reported in [24]. However, the methods have their own limitations which come in the way of practical implementation for a compact and reliable solution. This paper investigates three suitable powering schemes for the multi-inductor hybrid converter and provides more detailed comparison and design insights to help converter designers choose a suitable solution.

Three powering schemes of particular interest are isolated power modules (Fig. 3a), regulated supplies from switch blocking voltage (Fig. 3b), and regulated supplies from cascaded bootstrap (Fig. 3c). In this work, they are implemented and demonstrated with the optimal half-bridge driver scheme described above. This section will provide descriptions of their operations, trade-offs, and design insights, while experimental demonstrations and measured performances are provided in Section IV.

A. Use of isolated power modules

As a straightforward method, isolated power modules can be used for driving high side switches, Sw_1 and Sw_2, shown in Fig. 3a. When the SCBC is extended to a larger number of levels, i.e. more SC stages, this powering method can be reliable as will be shown in Section IV. However, isolated power modules often have relatively large parasitic capacitance between the primary and secondary ground which can significantly limit the switching frequency and transient performance of the converters, and increase switching loss. Therefore, an exhaustive search for isolated DC-DC converter modules is recommended to find the lowest possible isolation capacitance to improve converter performance [27]. A key drawback of isolated power modules is their sizes that are often significantly larger than other components of the circuit, including both power switches and gate driver ICs [27], [28]. In addition, they are relatively inefficient, with efficiency limited to below 60%, and capable of a relatively small load range [27]. The inefficiency increases gate driving losses that could be significant at light loads, which get worse when many modules are used for multiple high-side switches. It is therefore desirable to find a more compact and efficient method to power high-side switch drivers.

B. Regulated supplies from switch blocking voltages

In multi-level converters, there are many intermediate voltage nodes switching at levels that can be utilized to generate flying voltage domains to drive high-side switches. From this recognition, another method to generate flying power rails from the converter switching nodes is explored to replace the isolated power modules in Fig. 3a. In the circuit shown in Fig. 3b, the blocking voltages of high-side switches Sw_1 and Sw_2 when they are off can be used to generate its V_{GS} driving voltage. For example, when switch Sw_1 is off, the voltage between its drain and source terminals can be used to charge capacitor C_{x1} via diode D_1. In multilevel converters, this capacitor voltage is often larger and can then be regulated down to the required ~5-V level to drive Sw_1 using a linear low-dropout regulator (LDO). A similar operation can be observed for Sw_2 and its related circuit. Although this method consists of multiple discrete components, including an LDO, a diode, and two capacitors, because they are compact, the implementation space for this regulated flying supply domain is still significantly smaller compared to a standard isolated module. Therefore, this flying rail powering method helps reduce the overall area for gate driving circuits.

A key limitation of this powering method is the intrinsic nature of the LDO: its efficiency is low when there is a big difference between the blocking voltage ($\sim V_{C_{x1}}$) and the required V_{GS} level (~5 V). Unfavorably for this method, the blocking voltage depends on the converter topology, input voltage, and output current. When the input voltage increases, the blocking voltage increases linearly, and hence, the LDO efficiency decreases and gate driver power loss increases. Although having less impact, higher output currents also cause efficiency degradation in the LDOs and gate drivers as a consequence of larger voltage ripples on the main flying capacitors, leading to larger differences between the blocking voltages of high-side switches ($\sim V_{C_{x1}}$) and the LDOs' output (~5 V).

C. Regulated supplies from cascaded bootstrap circuits

To reduce the voltage difference between the input and output of gate driver LDOs and avoid the dependence on the converter's input voltage and output current, another powering

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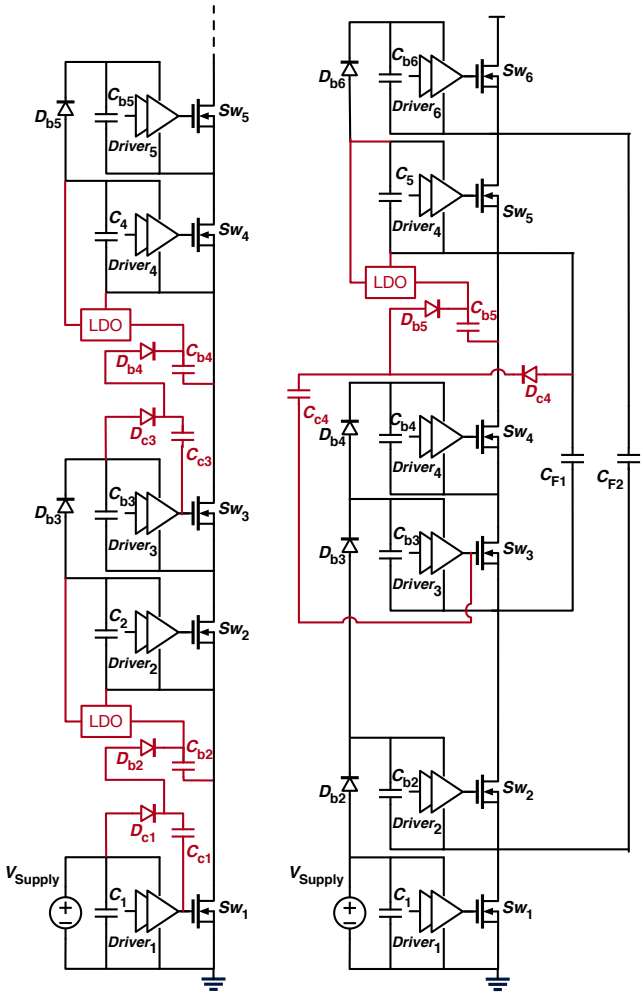
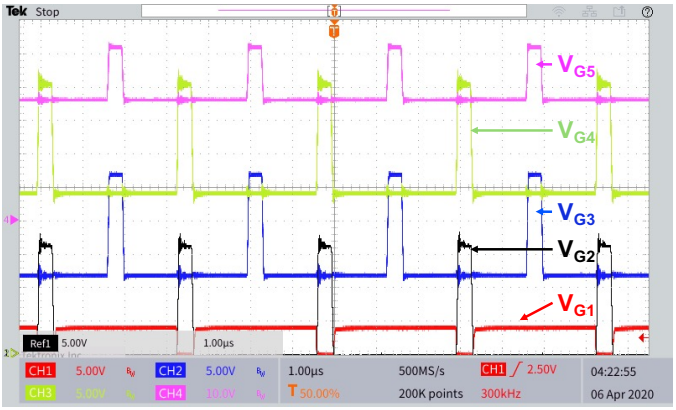
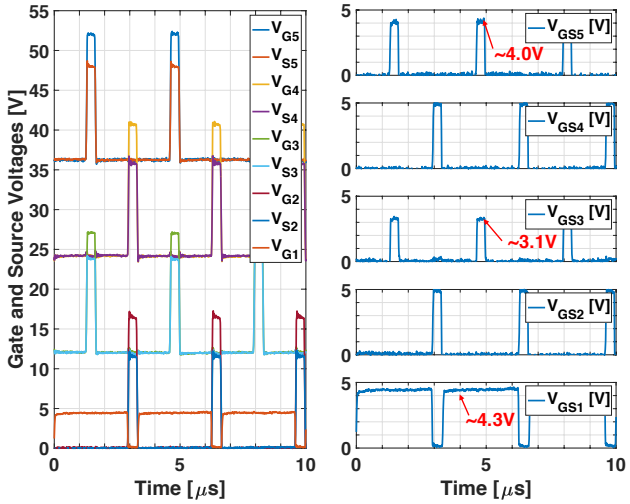


(a) Double charge-pump. (b) Gate driven charge-pump.

Fig. 4: Example of charge-pumps



(a) Measured gate signals of switches $Sw_{1\text{-}5}$.



(b) Measured gate and source voltages of switches $Sw_{1\text{-}5}$.

(c) Measured gate to source voltages of switches $Sw_{1\text{-}5}$.

Fig. 5: Experimental waveforms of gate to source voltages of stacked switches using modified charge pump method

scheme for high-side gate drivers is desirable. Figure 3c shows a circuit for a cascaded bootstrap circuit with additional LDOs added to all power domains of gate drivers. Although this cascaded bootstrap structure still has a diode voltage loss at every stack level, the input supply voltage V_{Supply} can be increased to overcome the series diode stack to support the top driver while the LDOs regulate the same safe driving voltage for all the gate drivers. Particularly, in the circuit shown in Fig. 3c, V_{Supply} is provided at ~5.6V, accounting for 0.5V diode drop in 2 cascaded stages to provide ~5.1 V at C_{x2}. From C_{x2}, the LDO can have a 100mV drop-out voltage margin to regulate a 5V supply for the flying voltage domain driving Sw_2.

In this method, cascading bootstrap circuits for a large number of stack switches will result in a large accumulation of multiple diode drops, requiring a large V_{Supply} for operation. A large V_{Supply}, in turn, put the LDOs at the bottom and lower voltage domains of the stack at low efficiencies because of large input/output voltage differences. Therefore, there have been new engineering efforts in both industry and academia to replace the bootstrap diodes with synchronous active devices in a more integrated approach [4], [29]. This can mitigate the requirement for high V_{Supply} and reduce the number of LDOs to improve gate driver efficiency. This paper focuses on commercially available parts for our developments, but it is still worth mentioning that ultimately, one would like to have a similar more integrated solution to achieve a more optimal power driving scheme which will need further investigations.

D. Discussion on recently popular charge-pump methods

Double charge-pump bootstrap circuit together with LDOs was proposed as an alternative [30] illustrated in Fig. 4a. This method uses a lower-level driver to charge-pump higher bootstrap voltage instead of using a separate switch as in [31], [32]. The key idea in double charge-pump circuits is to utilize two cascaded charge-pump to double the bootstrap voltage to overcome diode voltage drops, then use an LDO to regulate the driver supply voltage to the desired ~5V level. This method has been popular in recent days, and there is also a variation of this circuit named gate driven charge pump claimed preferred option for hybrid converters [24], [30]. This method is also shown in Fig. 4b.

While the operations of the charge pump circuits can use the same V_{Supply} level, they suffer from a serious practical

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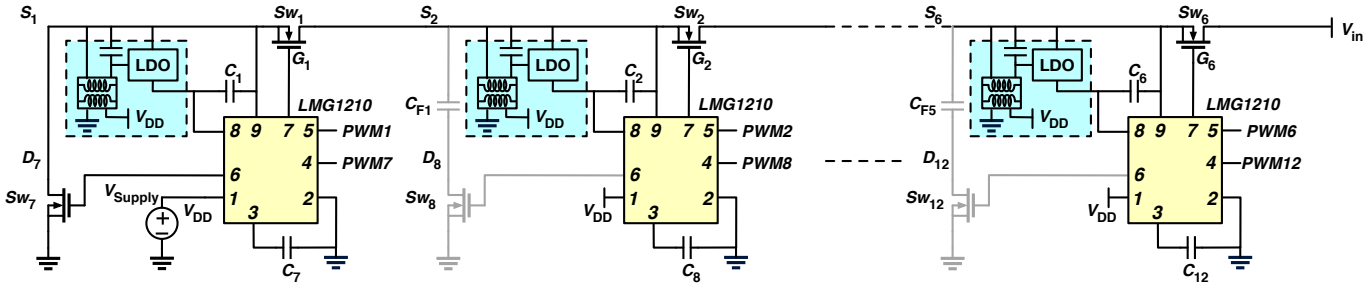
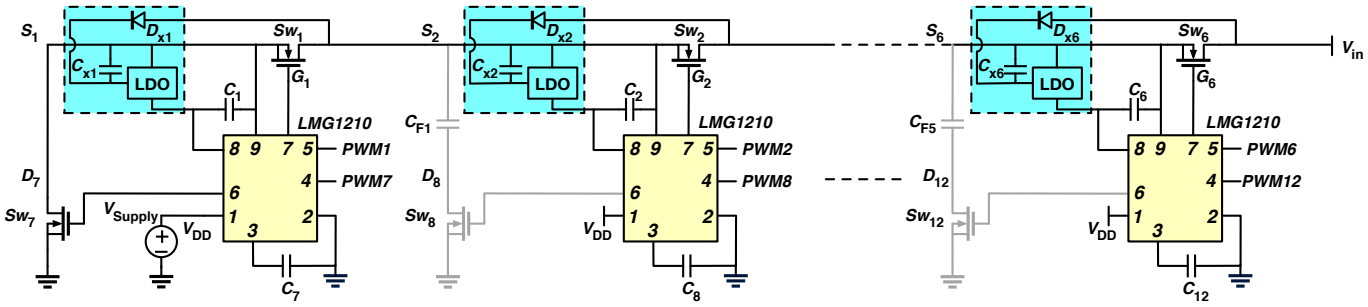
issue that comes from the loading effect on drivers at lower voltage domains. In today's gate driver ICs commercially available for GaN FETs, the drivers are generally designed to drive one switch. However, in the operations of double charge pump circuits, the bootstrapped driver ($Driver_{\rm j}$) of each voltage domain needs to also drive the charge to bootstrap capacitors for higher domains. Particularly, during the charging of C_{b2} and C_{b4} in the double charge-pump circuit of Fig. 4a, $Driver_1$ and $Driver_3$ carry turn-on current for switch Sw_1 and switch Sw_3 and the current required to charge capacitor C_{b2} and C_{b4} respectively. Furthermore, when more switches and stages are stacked on top of switch Sw_4, the very heavy accumulated loading comes to $Driver_3$ and ultimately $Driver_1$. In practice, as gate driver is not generally designed to carry this level of large loads, its ON resistance comes into the picture, lowering the actual V_{GS1} of Sw_1 and V_{GS3} of Sw_3. Because of these non-idealities, actual values of V_{GS1} and V_{GS3} can become as low as $\sim$4.3 V and $\sim$3.1 V. This $\sim$3.1V is far below the required level to properly turn on switch Sw_3, leading to low converter efficiency and failure of Sw_3. Note that, this effect is separate from the effect of the gate voltage drop from the bootstrap diode. In Fig. 4a, bootstrap diode has effect on V_{GS3} and V_{GS5}. The loading effect of the driver has effects on V_{GS1} and V_{GS3}. As non-ideality of V_{GS3} comes from both the sources, the worst case can be seen on the magnitudes of it, and it has higher chances of failures. Depending on the nature of a multilevel converter, a failure of one switch can expose other switches to voltage levels much higher than their ratings, causing cascaded failures and irreversible damages to the whole converter. Experimental demonstration of this phenomenon has been provided in Fig. 5. The circuit in Fig. 4 has been implemented, all the gate and source voltages have been measured, and the gate to source voltages have been calculated from the measurements.

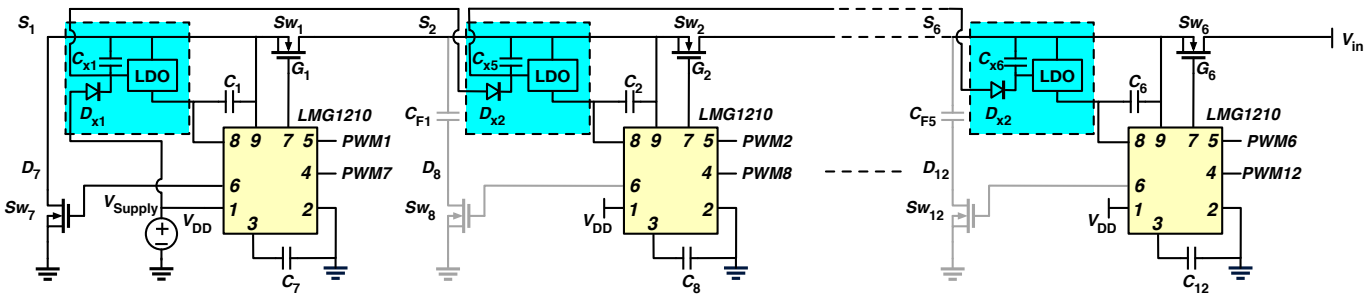
This practical problem is common in many double charge-pump circuits. The gate-driven charge pump method claimed as preferred in [24] and illustrated in Fig. 4b also suffers from the same problem. $Driver_3$ in Fig. 4b supply the currents to



(a) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and isolated power supply modules.



(b) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and regulated supplies from switch blocking voltages.



(c) Stacked switches of 6-Level MIH Converter using optimized half-bridge drivers and regulated supplies from the cascaded bootstrap method.

Fig. 6: Schematic diagrams of the implemented converter prototype using different driver, signal isolator, and powering schemes (Stacked Switches and their driver circuits are shown. Inductors, output capacitor and load are not shown.)

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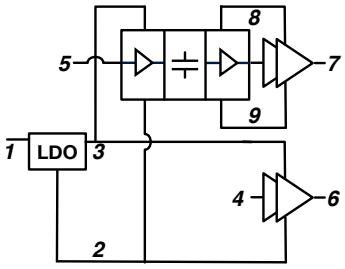


Fig. 7: Block diagram of LMG1210 [33], a half-bridge driver IC with integrated signal isolator and linear regulator (LDO), used in Fig. 6

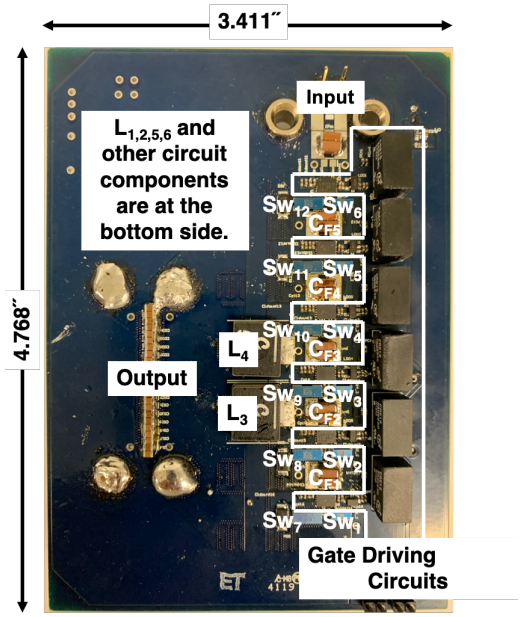


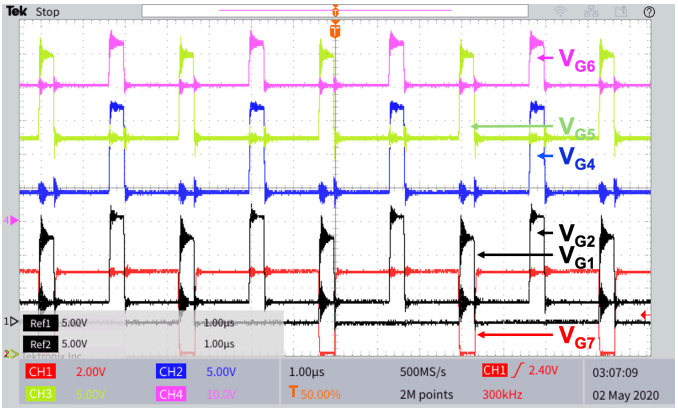
Fig. 8: Multi-level multi inductor hybrid converter prototype, reconfigurable for different schemes in gate driver, signal isolator, and powering flying voltage domains.

turn on switch SW_3 as well as Sw_5 and Sw_6 by charging C_{b5}. The key solution to this problem is to utilize the strong power switches of the converter, rather than those weaker transistors of the gate drivers, to drive the charge-pump capacitors, as shown in the two powering schemes discussed in subsection III-B (Fig. 3b) and Section III-C (Fig. 3c) above. The strength of the main power switches is capable of satisfying the current stress needed by multiple gate driver bootstrap circuits.

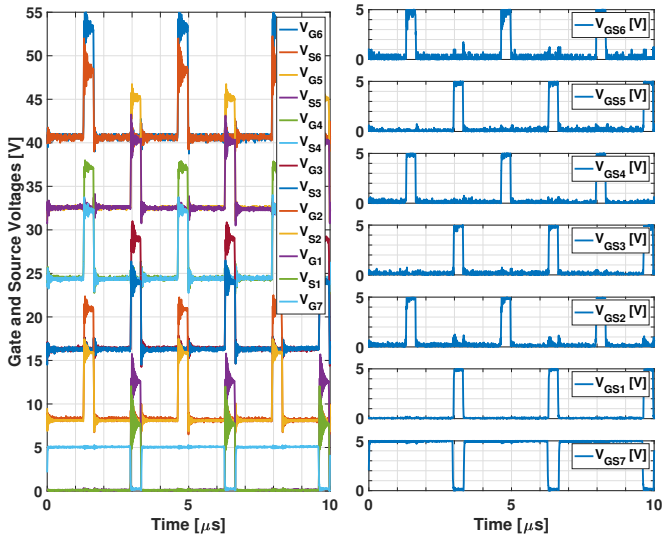
IV. Hardware Implementations and Experimental Results

In order to verify their steady-state and transient operations of the proposed level shifting method in Section II, a multilevel multi-inductor hybrid (MIH) converter has been implemented whose schematic is shown in Fig. 1. The hardware prototype, shown in Fig. 8, has been designed with careful layout considerations to have short gate driving loops decoupled from the power loops.

The prototype in Fig. 8 does not use any separate level shifters for the floating switches of multiple levels. Instead, it has been implemented with the isolator-less, optimized half-bridge driver method using the internal integrated level



(a) Measured gate signals of switches $Sw_{1\text{-}2,4\text{-}7}$



(b) Measured gate and source signals of switches $Sw_{1\text{-}7}$.

(c) Measured gate to source voltages of switches $Sw_{1\text{-}7}$.

Fig. 9: Experimental waveforms of the MIH converter using optimized half-bridge drivers and regulated supplies from cascaded bootstrap method. operating condition : Number of phases=2, V_{in}=48V, I_{Load}=10A and Duty cycle=10%

shifter of a standard commercial half-bridge gate driver IC LMG1210. A detailed diagram of LMG1210 is shown in Fig. 7. To compare the trade-offs of the powering methods, the prototype board has been reconfigured for different powering schemes as drawn in details on Fig. 6. Fig. 6 illustrates the main power components including all the switches and flying capacitor and the detailed connections of the gate driving circuits using a 9-pin block for the LMG1210 gate driver IC. Particularly, Fig. 6a, 6b and 6c show three different high-side driver powering schemes: isolated power supply modules, regulated supplies from switch blocking voltages, and regulated supplies from cascaded bootstrap method. With experimental demonstrations, the validity of the level-shifting technique have been shown and different powering schemes have been compared for trade-offs.

The hybrid converter in Fig. 1 can be operated with a minimum of 2 to a maximum of 6 energizing phases. Operating the converter at multiple phases, the ripple currents of the six inductors can be minimized to have low output

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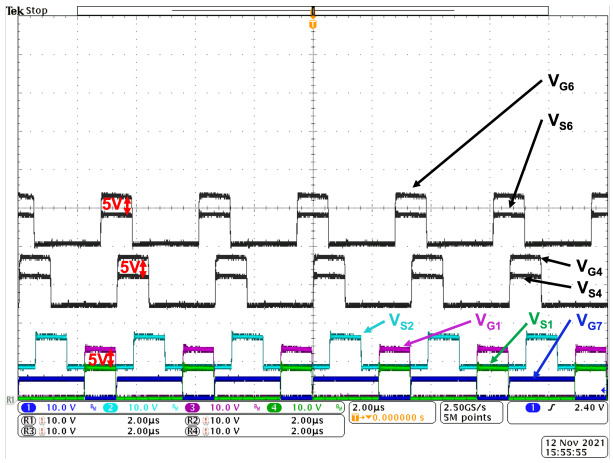
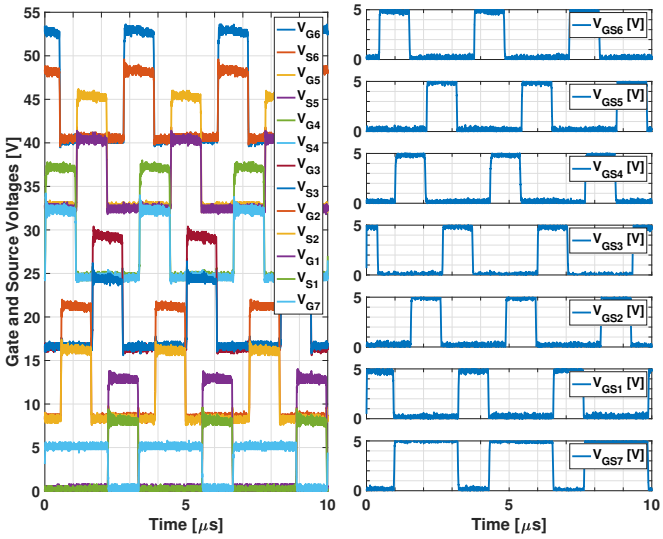


(a) Measured gate signals of switches $Sw_{1,4,6,7}$ and source signals of switches $Sw_{1,3,4,6}$



(b) Measured gate and source signals of switches $Sw_{1\text{-}7}$.

(c) Measured gate to source voltages of switches $Sw_{1\text{-}7}$.

Fig. 10: Experimental waveforms of the MIH converter using optimized half-bridge drivers and regulated supplies from cascaded bootstrap method. operating condition : Number of phases=6, V_{in}=48V, I_{Load}=10A and Duty cycle=32%

voltage ripple. The converter has twelve switches in total, six of which, $Sw_{7\text{-}12}$, are at the ground level and the other six, $Sw_{1\text{-}6}$, are stacked on Sw_7. Six half-bridge drivers LMG1210 ICs are employed to drive the 12 switches in this implementation. While Sw_1-Sw_7 pair is directly connected and operated as a conventional half-bridge, the remaining 5 switch pairs, Sw_2-Sw_6 to Sw_8-Sw_{12}, are connected via 5 flying capacitors, C_{F1} to C_{F5}, respectively. All the switch pairs which receive complimentary driving signals are driven with separate gate driver ICs. Hence, six half-bridge driver ICs are used for six switch pairs.

In the circuit in Fig. 6a, an LDO is used after each isolated power module to regulate the gate driver supply voltage at ~5.0-5.5 V, recommended for sensitive GaN switches [27], [34]. These LDOs can be avoided if the isolated power modules can maintain a tight voltage close to 5 V. As the implementation also targeted reconfiguribility for other powering scheme validation, these LDOs provide benefits of simple modification from one powering scheme to another described in Fig. 6. Note that the LMG1210 driver conveniently comes with an integrated LDO for its bottom driver. Therefore, no additional discrete LDO is needed for the ground switches Sw_7-Sw_{12}, while operating with cascaded bootstrap method shown in Fig. 6c.

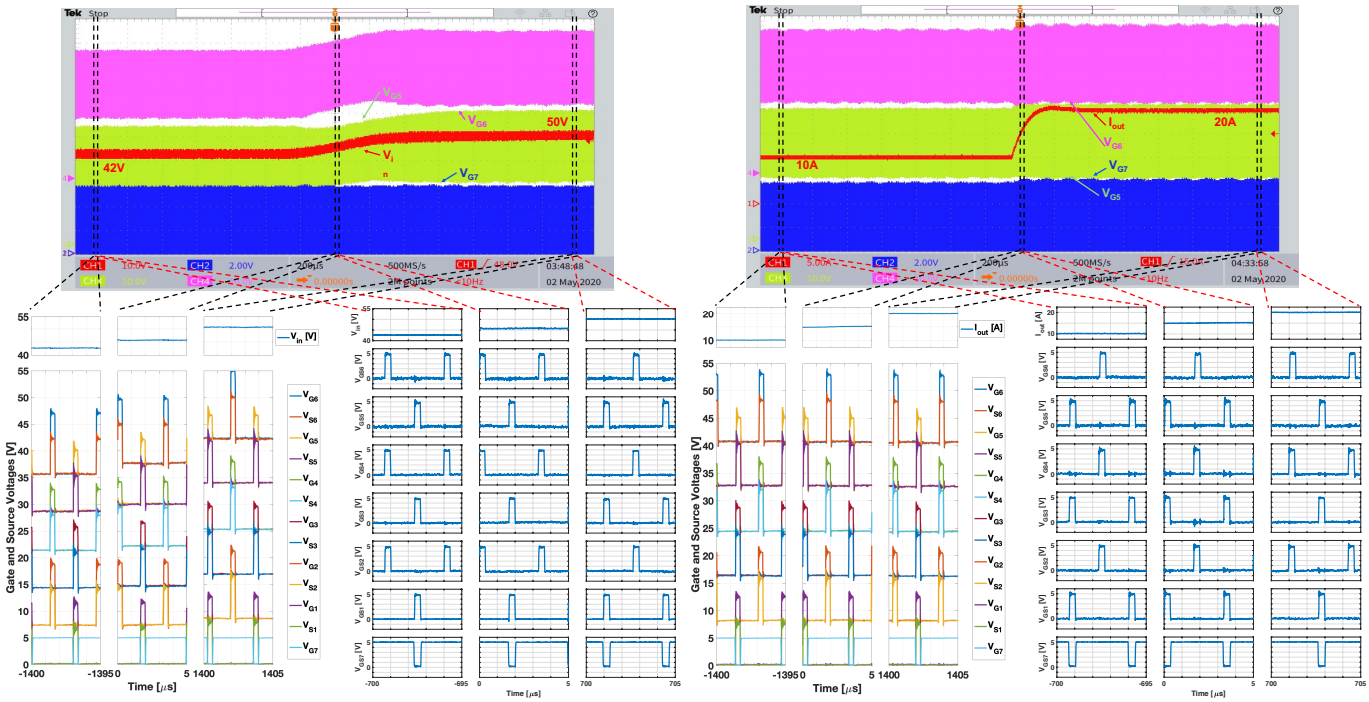
The powering method where switch blocking voltages are used to derive the power rails (Fig. 6b) does not work when the input voltage is low such that switch blocking voltages are reduced to less than 5 V, i.e. not enough voltage to provide to the LDOs. This scenario can be seen at startup when input voltage starts increasing from zero. In this particular implementation, this powering scheme starts working for an input voltage from ~18 V. In normal operations of the converter with V_{in} at 40-60 V, switch blocking voltages are at least ~6.5V for LDOs for $Sw_{1,6}$ and ~13V for LDOs for $Sw_{2\text{-}5}$. These voltages are high enough to warrant the intended operation of the circuits.

In Fig. 6c, the implemented cascaded bootstrap circuit involves a chain of seven drivers. Among these seven drivers, the top six are the high side drivers of six different gate driver ICs. This is a new demonstration of the cascaded bootstrap method where the cascading between the drivers involves both being the high side drivers. Previous implementations were only done within the half-bridge driver IC or from one sigh side driver of a lower level half-bridge driver IC to the low side of another higher level half-bridge driver IC.

The 2P6IHC prototype with all three driver powering schemes was also tested for durability and reliability in both steady state and transient conditions. These methods did not show any significant differences in their performances under the test conditions. As the cascaded bootstrap method is the most attractive one among them in terms of efficiency and area, test results associated with this method is particularly shown in this work. The steady-state operation is measured in Fig. 9 showing the intended operation to provide the right 5V V_{GS} for all stacked GaN switches. This measurement has been taken at 48 V input voltage with 10% duty cycle operation for all the phases. The gate and source signals are measured separately using separate probes with respect to the ground. Fig. 9a shows measurements of some of the gate signals, while the converter was in operation. Separately measured data were collected and plotted together in Fig. 9b to clearly show the distinctive levels of the different gate and source signals. Fig. 9c illustrates the gate to source voltages of each of the stacked switches separately. This validates the proposed level shifting method for the application of a multi-level converter along with the powering scheme.

To show the effectiveness of this method over a broader range of duty cycle and multi-phase operations, this experiment has been repeated in Fig. 10 with the converter operating in 6 phases with 32% duty cycle. Fig. 10a includes the measurements of multiple gate and source voltages of the converter, Fig. 10b includes the plot of all the gate and source voltages of the stacked switches and Fig. 10c includes the gate to source voltages of each individual stacked switches.

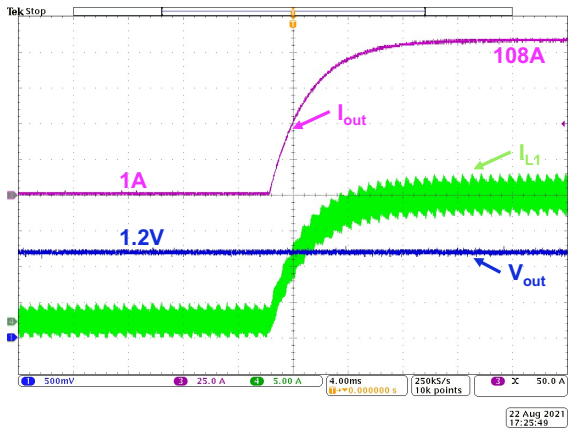
It is also desirable to verify the performance of the proposed



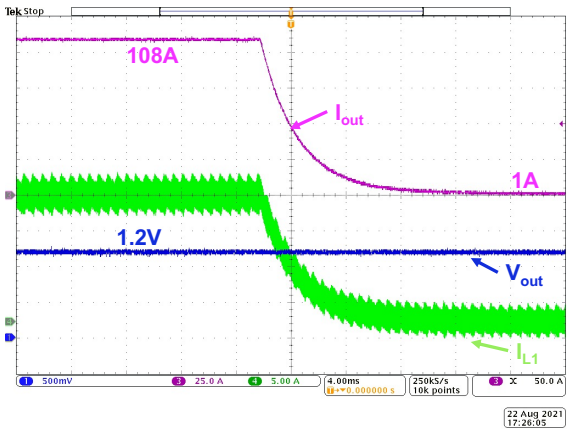
(a) 42V to 50V line transient waveforms.

(b) 10A to 20A load transient performance.

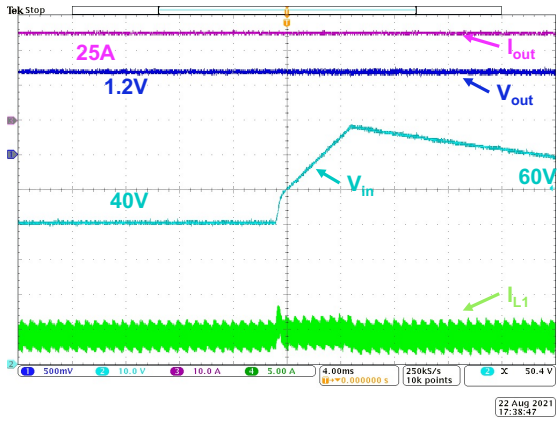
Fig. 11: Measured transient gate signals of the MIH converter prototype using optimized half-bridge driver and regulated supplies from cascaded bootstrap method.



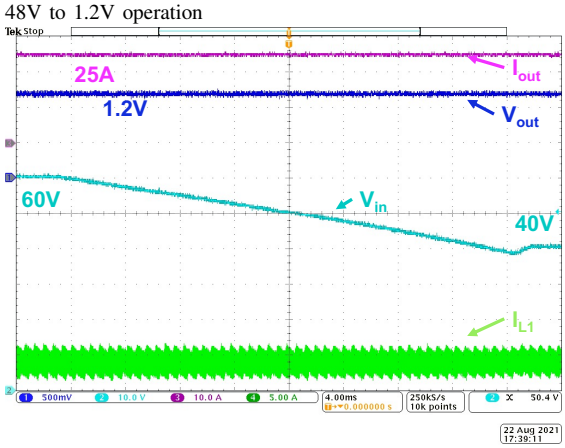
(a) Load transient of 1A to 108A of 6-level MIH converter for 48V to 1.2V operation



(b) Load transient of 108A to 1A of 6-level MIH converter for 48V to 1.2V operation



(c) Line transient of 40V to 60V of 6-level MIH converter for 1.2V/25A operation



(d) Line transient of 60V to 40V of 6-level MIH converter for 1.2V/25A operation

Fig. 12: Reliability testing of the demonstrated gate driving circuits at very high transients

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TABLE I: List of components and comparison for different gate drivers and powering schemes

Gate driver	Half-bridge drive	Optimized half-bridge driver		
Powering scheme	Modified double charge-pump	Isolated supply modules	Regulated supplies from switch blocking voltages	Cascaded bootstrap + LDOs
Converter prototype	2-Phase 4-inductor Hybrid Converter [12]	2-Phase 6-Inductor Hybrid Converter [16]		
Number of levels	4	6	6	6
Total number of switches	8	12	12	12
Ground level switches	4 (2xEPC2023)	6 (2xEPC2023)	6(EPC2023)	6(EPC2023)
Stacked switches	4 (2xEPC2015c)	6 (2xEPC2015c)	6(EPC2015c)	6(EPC2015c)
Single gate drivers	4 (LM5114)	0	0	0
Half-bridge drivers	2 (LMG1205)	6 (LMG1210)	6 (LMG1210)	6 (LMG1210)
Isolated supply modules	0	6 (CRE1S0505S3C)	0	0
Signal isolators	2 2-channel (Si8423BB-D-IS)	0	0	0
Diodes	4 (CRS08)	0	6(CRS08)	6(CRS08)
LDOs	2 (TPS70950DBVR)	6 optional (TPS70950DBVR)	6 (TPS70950DBVR)	6 (TPS70950DBVR)
Driver supply voltage and current	5V/123mA	5V/247mA	5V/37mA + 48V/6mA	6.7V/53mA
Gate switching power*	0.332W	0.498W	0.249W	0.249W
Driver efficiency***	54%	40.32%	52.64%	70.1%
Implementation area†	265 mm^2	520.54 mm^2	124.8 mm^2	124.8 mm^2
Performance	poor	moderate	good	good
Favorable solution	no	Area dependent	yes	yes

*Calculated with gate charge provided in the switch data sheets.
** Measurements are taken at no load.
*** Efficiency $= \frac{\text{Gate Switching Power}}{\text{Drive supply voltage} \times \text{Drive supply current}}$
† Calculated without the area of the capacitors used in gate driving circuits.

level shifting technique during operation transients. 8V line transients and 10A load transients with cascaded bootstrap method are also shown in 11a, and 11b. In these figures, all the gate and source voltages are measured. Gate to source voltages are calculated from these measurements and plotted before, during and after the transients. Steady 5V for all the V_{GS} suggests this method reliable during all the transient states. The converter has been also exposed to very high line voltage and load current change, and the converter was reliable during the measurements. These measurements are included in Fig. 12. Figs. 12a-12b show the load change of ~100A and Fig. 12c-12d show the line voltage change of ~20V. Fixed output voltages with large transients proves the effectivity of the demonstrated method with dynamic duty cycle changes during the transients. These measurements have been conveyed with the converter operating in 6 phases.

Table I includes a comparison of the gate driving and powering methods investigated in this paper on a number of characteristics and trade-offs. Optimal utilization of the signal isolator built-in to commercial half-bridge drivers creates new opportunities to save significant areas of discrete signal isolators. This method combined with either regulated power supplies from switch blocking voltages or regulated power supplies with cascaded bootstrap can yield an overall significantly smaller area while achieving both high driving efficiency and reliability. In these better powering schemes, the cascaded bootstrap and LDO regulation for every stage produces a high driving efficiency of ~70% because of the flexibility to set small voltage drops across the LDOs. The driving efficiency is calculated from the gate driving loss from the data sheet and the measured driving power in the experiment.

V. Conclusion

In summary, a number of methods to power and drive stacked switches in a GaN-based multi-level multi-inductor (MIH) hybrid converter have been discussed and experimentally demonstrated in this work. Their trade-offs and challenges have been discussed from different aspects of practical implementations to help designers choose a suitable solution for particular design needs. In practice, gate driver circuits can cause faults and failures in converters using sensitive GaN FETs. Hence, it is desirable to choose a set of proper level shifting techniques for PWM signals and powering schemes for reliable operations while maintaining an overall compact and efficient implementation. An isolator-less method has been devised for small area implementation and demonstrated with different powering schemes for elevated domains. A 6-level 6-inductor hybrid converter prototype was used to demonstrate the gate driving and powering schemes, validate their operations, and discuss performance and design trade-offs. The experiments, circuits, and discussions in this paper are aimed to be a good source of reference for future engineering efforts in designing multi-level hybrid converters.

References

[1] J. Zhu and D. Maksimović, "A Family of Transformerless Stacked Active Bridge Converters," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 19–24.

[2] S. Webb, T. Liu, and Y.-F. Liu, "A Two-Phase Zero-Inductor Voltage Converter for Datacenter and Server Applications," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 2255–2262.

[3] S. Khatua, D. Kastha, and S. Kapat, "Novel Transformer-Less DAB Converters for the Regulated First-Stage of a Two-Stage 48 V VRM," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 5258–5264.

[4] S. Biswas and D. Reusch, "GaN Based Switched Capacitor Three-Level Buck Converter with Cascaded Synchronous Bootstrap Gate Drive Scheme," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 3490–3496.
[5] S. Khatua, D. Kastha, and S. Kapat, "A New Single-Stage 48-V-Input VRM Topology Using an Isolated Stacked Half-Bridge Converter," *IEEE Transactions on Power Electronics*, vol. 35, no. 11, pp. 11 976–11 987, Nov. 2020.
[6] A. Kumar, S. Pervaiz, and K. K. Afridi, "Single-stage isolated 48V-to-1.8V point-of-load converter utilizing an impedance control network and integrated magnetic structures." IEEE, Jul. 2017, pp. 1–7.
[7] J. S. Rentmeister and J. T. Stauth, "A 48V:2V flying capacitor multilevel converter using current-limit control for flying capacitor balance," in *2017 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2017, pp. 367–372.
[8] P. Jain, A. Prodić, and A. Gerfer, "Wide-input high power density flexible converter topology for dc-dc applications," in *2016 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2016, pp. 2553–2560.
[9] S. Khatua, D. Kastha, and S. Kapat, "A Non-Isolated Single-Stage 48V-to-1V VRM with a Light Load Efficiency Improvement Technique," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 143–148.
[10] G.-S. Seo, R. Das, and H.-P. Le, "Dual Inductor Hybrid Converter for Point-of-Load Voltage Regulator Modules," *IEEE Transactions on Industry Applications*, vol. 56, no. 1, pp. 367–377, Jan. 2020.
[11] R. Das, G. Seo, D. Maksimovic, and H.-P. Le, "An 80-W 94.6%-Efficient Multi-Phase Multi-Inductor Hybrid Converter," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 25–29.
[12] R. Das and H.-P. Le, "A Regulated 48V-to-1V/100A 90.9%-Efficient Hybrid Converter for POL Applications in Data Centers and Telecommunication Systems," in *2019 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Mar. 2019, pp. 1997–2001.
[13] O. Kirshenboim and M. M. Peretz, "High-Efficiency Nonisolated Converter With Very High Step-Down Conversion Ratio," *IEEE Transactions on Power Electronics*, vol. 32, no. 5, pp. 3683–3690, May 2017.
[14] K. Matsumoto, K. Nishijima, T. Sato, and T. Nabeshima, "A two-phase high step down coupled-inductor converter for next generation low voltage CPU," in *8th International Conference on Power Electronics - ECCE Asia*, May 2011, pp. 2813–2818.
[15] K. Abe, K. Nishijima, K. Harada, T. Nakano, T. Nabeshima, and T. Sato, "A Novel Three-Phase Buck Converter with Bootstrap Driver Circuit," in *2007 IEEE Power Electronics Specialists Conference*, Jun. 2007, pp. 1864–1871.
[16] R. Das and H.-P. Le, "A Two-Stage 110VAC-to-1VDC Power Delivery Architecture Using Hybrid Converters for Data Centers and Telecommunication Systems," *Techrxiv Preprints, DOI: 10.36227/techrxiv.16557711.v1*, Sep. 2021.
[17] V. Yousefzadeh, E. Alarcon, and D. Maksimovic, "Three-level buck converter for envelope tracking applications," *IEEE Transactions on Power Electronics*, vol. 21, no. 2, pp. 549–552, Mar. 2006.
[18] Y. Liu, A. Kumar, D. Maksimovic, and K. K. Afridi, "A High-Power-Density High-Efficiency Three-Level Buck Converter for Cellphone Battery Charging Applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 5265–5270.
[19] P. S. Shenoy, M. Amaro, J. Morroni, and D. Freeman, "Comparison of a Buck Converter and a Series Capacitor Buck Converter for High-Frequency, High-Conversion-Ratio Voltage Regulators," *IEEE Transactions on Power Electronics*, vol. 31, no. 10, pp. 7006–7015, Oct. 2016.
[20] J. Zhu, R. Schuess, and D. Maksimovic, "General Properties and Synthesis of Transformerless Stacked Active Bridge Converters," in *2019 20th Workshop on Control and Modeling for Power Electronics (COMPEL)*, Jun. 2019, pp. 1–6.
[21] L. Zhang and S. Chakraborty, "An Interleaved Series-Capacitor Tapped Buck Converter for High Step-Down DC/DC Application," *IEEE Transactions on Power Electronics*, vol. 34, no. 7, pp. 6565–6574, Jul. 2019.
[22] "Si8410/20/21 (5 kV) Si8422/23 (2.5 & 5 kV) Data Sheet," Silicon Laboratories, Inc., Tech. Rep.
[23] "3.0 kV rms, Dual-Channel Digital Isolator ADuM120N/ADuM121N," Analog Devices, Inc., Tech. Rep.
[24] Z. Ye, Y. Lei, W.-C. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Improved Bootstrap Methods for Powering Floating Gate Drivers of Flying Capacitor Multilevel Converters and Hybrid Switched-Capacitor Converters," *IEEE Transactions on Power Electronics*, vol. 35, no. 6, pp. 5965–5977, Jun. 2020.
[25] A. Kumar and K. K. Afridi, "Single-stage isolated 48V-to-1.8V point-of-load converter utilizing an impedance control network for wide input range operation," in *2017 IEEE Energy Conversion Congress and Exposition (ECCE)*, Oct. 2017, pp. 2003–2009.
[26] L. Pham-Nguyen, V.-Q. Nguyen, D.-M. Nguyen, H.-D. Han, K.-H. Nguyen, and H.-P. Le, "A 14-W 94%-Efficient Hybrid DC-DC Converter with Advanced Bootstrap Gate Drivers for Smart Home LED Applications," in *2018 IEEE Energy Conversion Congress and Exposition (ECCE)*, Sep. 2018, pp. 4744–4749.
[27] "CRE1 Series:isolated 1W Single Output Isolated DC-DC converters," Murata Power Solutions Inc., Tech. Rep.
[28] "DC/DC Converter," Recom Power, Tech. Rep.
[29] "EPC2107 – Enhancement-Mode GaN Power Transistor Half-Bridge with Integrated Synchronous Bootstrap," Efficient Power Corporation, Tech. Rep.
[30] Z. Ye, Y. Lei, W.-c. Liu, P. S. Shenoy, and R. C. N. Pilawa-Podgurski, "Design and implementation of a low-cost and compact floating gate drive power circuit for GaN-based flying capacitor multi-level converters." IEEE, Mar. 2017, pp. 2925–2931.
[31] S. Park and T. Jahns, "A self-boost charge pump topology for a gate drive high-side power supply," *IEEE Transactions on Power Electronics*, vol. 20, no. 2, pp. 300–307, Mar. 2005.
[32] M. Kovacic and S. Krishnamurthy, "Gate drive power supply for multilevel converter," US Patent US20 150 318 788A1, Nov., 2015.
[33] "LMG1210 200-V, 1.5-A, 3-A half-bridge MOSFET and GaN FET driver with adjustable dead time for applications up to 50 MHz," Texas Instruments Inc., Tech. Rep.
[34] A. Lidow and J. Strydom, "eGaN® FET Drivers and Layout Considerations," Efficient Power Corporation, Tech. Rep., 2016.

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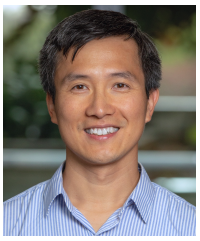

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