Robustness of Passivated ALD Zinc Tin Oxide TFTs to Aging and Bias Stress

Christopher R. Allemang, *Member, IEEE*, Tae H. Cho, Neil P. Dasgupta, and Rebecca L. Peterson, *Senior Member, IEEE*

***Abstract*— Thin-film electronics fabricated with amorphous oxide semiconductors (AOS) are being studied for beyond-display technologies because of their superior electron transport. To widen the commercial applications, robust devices fabricated using scalable deposition techniques are required. Here, we fabricate bottom-gate, top contact thin-film transistors (TFTs) using zinc tin oxide, an AOS deposited by atomic layer deposition (ALD), and study robustness to aging and bias stress for devices stored in a dark air ambient with and without Al_2O_3 passivation. All samples exhibit excellent mobility (μ_{FE}) and subthreshold swing (*SS*) robustness to aging. Most of the device aging occurs within the first 25 days, after which the performance stabilizes. Changes due to positive bias stress, which are dominated by interactions with ambient molecules, are greatly reduced by passivation. Passivation, however, results in an increase in contact resistance (R_C), *SS*, and negative bias illumination stress (NBIS) instability. The increase in R_C is attributed to the diffusion of oxygen vacancies that occurs during the passivation process, while the increase in *SS* and NBIS instability is attributed to subgap interface defects. The experimental results are compared to Silvaco ATLAS simulations to confirm the proposed physical mechanisms and allow quantification of the associated defects and non-idealities.**

***Index Terms*— Amorphous semiconductors, current–voltage characteristics, stability, thin-film transistors.**

I. Introduction

ELECTRONIC circuits comprised of thin-film transistors (TFTs) are essential to nearly every modern display technology. For decades, the TFT industry relied on amorphous silicon for the active layer; however, increasing performance demands require semiconductors with superior electron transport. Amorphous oxide semiconductors (AOS) can meet those performance demands [1] and sputtered indium-gallium-zinc-oxide (IGZO), a widely studied AOS, has been successfully commercialized as the active layer of display backplane TFTs [2]. Furthermore, there is a growing interest in developing thin-film electronics for beyond-display technologies, enabled by the superior performance of AOS. These include monolithic 3-D integration on Si CMOS integrated circuits (ICs) [3]. All of these applications require devices with excellent robustness to aging (i.e., stability under ambient conditions) and robustness to electrical bias stress.

While In_2O_3 [4] and IGZO [5] TFTs with low process temperature and excellent performance have been demonstrated, here we focus on an indium-free AOS material, zinc tin oxide (ZTO), because indium is comparatively scarce and costly [6], [7], [8]. ZTO has been studied using various deposition techniques including solution [9] and vacuum-based processes [10], [11], [12], [13], [14]. Here we use atomic layer deposition (ALD) because it is a low-temperature vapor-phase deposition method allowing for conformal and uniform thin-films with precise control over interfaces, stoichiometry, and thicknesses [15]. Previous work on aging of ZTO TFTs used ZTO films made by sputtering [16] or solution-based processes [17], [18]. These works attributed observed increases in subthreshold swing and threshold voltages as well as changes in ON and OFF current to water or oxygen adsorption or desorption at the back channel. The only investigation of aging with back channel passivated devices (using TiO_2) was limited to 20 days of aging [16]. No study has been done linking ZTO process conditions to aging effects, and no aging study has been done using ZTO films made by ALD. Similarly, for bias stress measurements, most of the existing work is on ZTO films deposited by sputtering [19], [20] or solution processing [21]. The only known work on bias stress in ALD ZTO TFTs tested only negative bias stress (NBS) up to 3000 s [10], which does not allow assessment of the ionization of bulk oxygen vacancies, which is traditionally done in AOS by negative bias illumination stress (NBIS) [22]. Since it is known that device robustness varies with deposition technique [23], here, we seek to address these knowledge gaps by investigating aging, positive bias stress (PBS), and NBIS in ALD ZTO.

In this study, we examine the robustness of ALD ZTO TFT threshold voltage, V_t, field-effect mobility, μ_{FE}, hysteresis, ΔV_c, and subthreshold swing, *SS*, to aging and bias stress prepared under two different sets of process conditions, with and without a passivation layer. Devices without a passivation

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Christopher R. Allemang was with the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI 48109 USA. He is now with Sandia National Laboratories, Albuquerque, NM 87185 USA.

Tae H. Cho is with the Department of Mechanical Engineering, University of Michigan, Ann Arbor, MI 48109 USA.

Neil P. Dasgupta is with the Department of Mechanical Engineering and the Department of Materials Science and Engineering, University of Michigan, Ann Arbor, MI 48109 USA.

Rebecca L. Peterson is with the Department of Electrical Engineering and Computer Science and the Department of Materials Science and Engineering, University of Michigan, Ann Arbor, MI 48109 USA (e-mail: blpeters@umich.edu).

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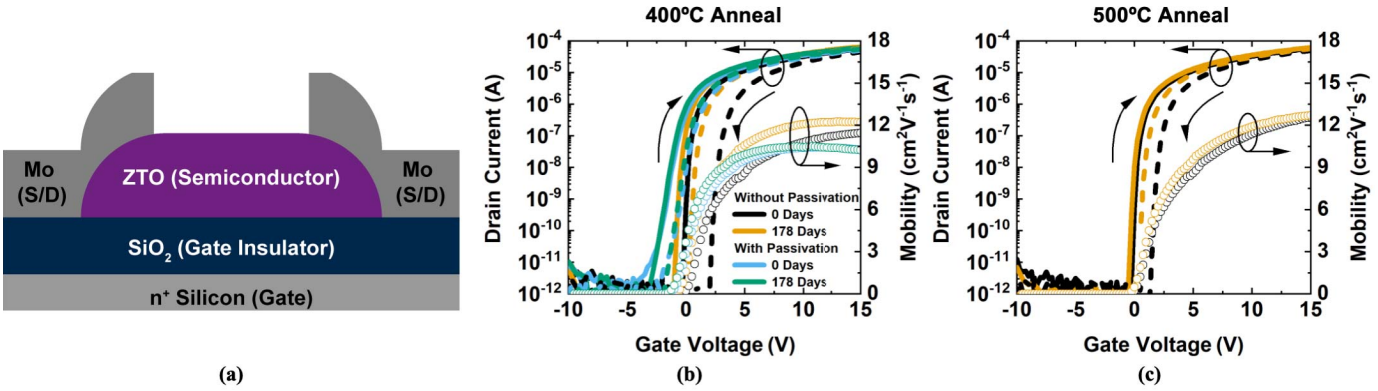

Fig. 1. (a) Schematic illustration of a ZTO TFT cross section with bottom-gate top-contact structure. Representative transfer characteristics (I_D–V_{GS}) with $V_{DS} = 1$ V are plotted on the left y-axis for devices without passivation on the first day of measurement (black) and after 178 days of aging (yellow) with ZTO annealed at (b) 400 °C and (c) 500 °C. In (b), we show traces for 400 °C annealed devices with passivation on the first day of measurement (blue) and after 178 days of aging (green). The forward I–V curves are indicated by the solid lines and the reverse I–V curves are indicated by the dashed lines. Linear field effect mobility extracted from these I–V curves are plotted on the right y-axis using open circles.

layer show minor changes in V_t and ΔV_c during the first 25 days of aging in a dark air ambient, after which they stabilize. Passivation greatly improves robustness to aging and PBS but also results in a one-time decrease in V_t and increases in SS and contact resistance, which are extracted using the transmission line method (TLM). Silvaco Atlas simulations are used to show that these one-time changes in V_t and SS are likely due to back-channel interface states induced during the deposition of the passivation layer. NBIS is reduced by using optimal ZTO process conditions but is not eliminated by passivation. The work presented here demonstrates the robustness of passivated ALD ZTO TFTs to aging and bias stress, which paves the way for their adoption in thin-film electronics for beyond-display technologies.

II. Experimental Methods

TFTs were fabricated on heavily doped n^+-Si with approximately 100 nm of thermal oxide grown to form the gate and gate insulator, respectively, in a bottom-gate top-contact structure schematically illustrated in Fig. 1(a). The active layer, approximately 12 nm of ZTO, was deposited by ALD using a Veeco Fiji G2 flow-type ALD tool at a deposition temperature of 150 °C with a hybrid thermal H_2O and O_2-plasma process and a 45% Sn cycle ratio which is expected to yield a film with approximately 21 at. % Sn content, as described in [24]. The ZTO films were then wet-etched for device isolation before being annealed at either 400 °C or 500 °C on a hotplate in an air ambient in a custom-built moisture-controlled glovebox with less than 20% relative humidity [25]. Finally, approximately 100 nm of molybdenum was deposited by sputtering and patterned by lift-off to form source–drain ohmic contacts [26]. Devices have channel lengths, L, and widths, W, of 10 and 120 μm, respectively, unless otherwise stated. Passivated devices were encapsulated with approximately 30 nm of Al_2O_3 deposited by ALD at 100 °C in a Veeco/Cambridge Nanotech Savannah system using an ozone process [27], chosen to reduce the V_t shift introduced by passivation [28]. Samples were stored and aged at room temperature in a dark air ambient between measurements.

Temporal stability and TLM measurements were taken using a Keysight B1505A power device analyzer while bias stress measurements were taken using an HP4156A semiconductor parameter analyzer. All measurements were taken at room temperature in an air ambient using continuous voltage sweeps. When both forward and reverse I–V curves are shown, the measurement was first taken in the forward direction, negative to positive V_{GS}, immediately followed by the reverse direction, positive to negative V_{GS}. PBS was applied by biasing the gate at +20 V while the source and drain were kept at 0 V. NBIS was applied by biasing the gate at −20 V while the source and drain were kept at 0 V under the illumination of a green LED (520 nm) with an optical power density of 900 μW cm^{-2}. All other measurements were taken in the dark.

The linear field-effect mobility, μ_{FE}, is extracted using the equation $\mu_{FE} = (dI_D/dV_{GS})L(WC_{ox}V_{DS})^{-1}$ where C_{ox} refers to the oxide capacitance per unit area and dI_D/dV_{GS} is the slope of the I_D–V_{GS} curve in the linear region. μ_{FE} values were extracted from the I_D–V_{GS} curve over the range 13 V $< V_{GS} <$ 15 V with $V_{DS} = 1$ V, unless otherwise stated. The threshold voltage, V_t, was found to be the x-axis intercept of a linear fit to the linear region of an I_D–V_{GS} sweep with $V_{DS} = 1$ V. The subthreshold swing, SS, is the inverse of the logarithmic rate of device current turn-on, in units of volts per decade of current. Hysteresis, ΔV_C, is defined as the difference in the value of V_{GS} at $I_D = 100$ nA between the forward and reverse sweeps when V_{GS} is swept between −10 and 30 V.

Silvaco ATLAS was used to conduct 2-D numerical simulations of the TFTs to understand the changes in device performance with the addition of a passivation layer. Simulation parameters and fitting processes from [29], [30] were used as a starting point and then iterated to fit the device characteristics presented here, similar to the method described in [31]. The final band model of the subgap states is shown in Fig. 2 (parameters found in Table I) where BG refers to the ZTO/gate insulator interface, BC refers to the ZTO/passivation interface, and IT refers to parameters applied to both BG and BC where BC parameters were only applied to simulations that include a passivation layer.

III. Results and Discussion

The transfer characteristics for devices without passivation and annealed at 400 °C and 500 °C are shown in Fig. 1(b) and (c), respectively, and are summarized in Table II for 0 and 178 days of aging. The excellent performance of unaged devices has been discussed in [24]. For both samples without passivation, the μ_{FE} and SS before and after 178 days

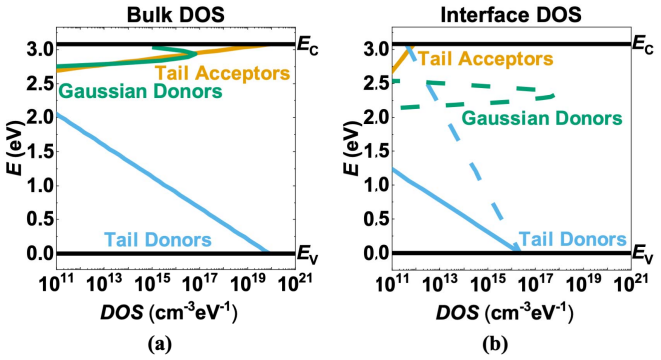

Fig. 2. (a) Band structure of bulk ZTO and (b) interfaces used in Silvaco ATLAS simulations. For (b), solid lines indicate the semiconductor/gate insulator interface (BG) used in all simulations while the dashed lines indicate the semiconductor/passivation interface (BC) used in simulations including a passivation layer.

TABLE I
PARAMETERS USED IN SILVACO ATLAS SIMULATIONS

Symbol (Unit)	Description	Value
μ_n ($cm^2V^{-1}s^{-1}$)	Electron Mobility	13.46
N_C/N_V (cm^{-3})	Conduction/Valance Band Effective DOS	4.14×10^{18}
E_G (eV)	Band Gap	3.08
N_{TA}/N_{TD} ($cm^{-3}eV^{-1}$)	Tail Acceptor/Donor State Peak Density	8.25×10^{19}
W_{TA} (eV)	Tail Acceptor State Width	0.019
W_{TD} (eV)	Tail Donor State Width	0.1
N_{GD} ($cm^{-3}eV^{-1}$)	Gaussian Donor State Peak Density	6.5×10^{16}
E_{GD} (eV)	Gaussian Donor State Peak Position	2.93
W_{GD} (eV)	Gaussian Donor State Peak Width	0.05
$N_{TA,IT}$ ($cm^{-3}eV^{-1}$)	IT Tail Acceptor State Peak Density	8.34×10^{11}
$N_{TD,IT}$ ($cm^{-3}eV^{-1}$)	IT Tail Donor State Peak Density	2.25×10^{16}
$W_{TA,IT}$ (eV)	IT Tail Acceptor State Width	0.19
$Q_{F,BG}$ (cm^{-2})	BG Fixed Charge	-5.20×10^{10}
$W_{TD,BG}$ (eV)	BG Tail Donor State Width	0.1
$Q_{F,BC}$ (cm^{-2})	BC Fixed Charge	2.38×10^{11}
$W_{TD,BC}$ (eV)	BC Tail Donor State Width	0.28
$N_{GD,BC}$ ($cm^{-3}eV^{-1}$)	BC Gaussian Donor State Peak Density	6.5×10^{17}
$E_{GD,BC}$ (eV)	BC Gaussian Donor State Peak Position	2.334
$W_{GD,BC}$ (eV)	BC Gaussian Donor State Peak Width	0.05

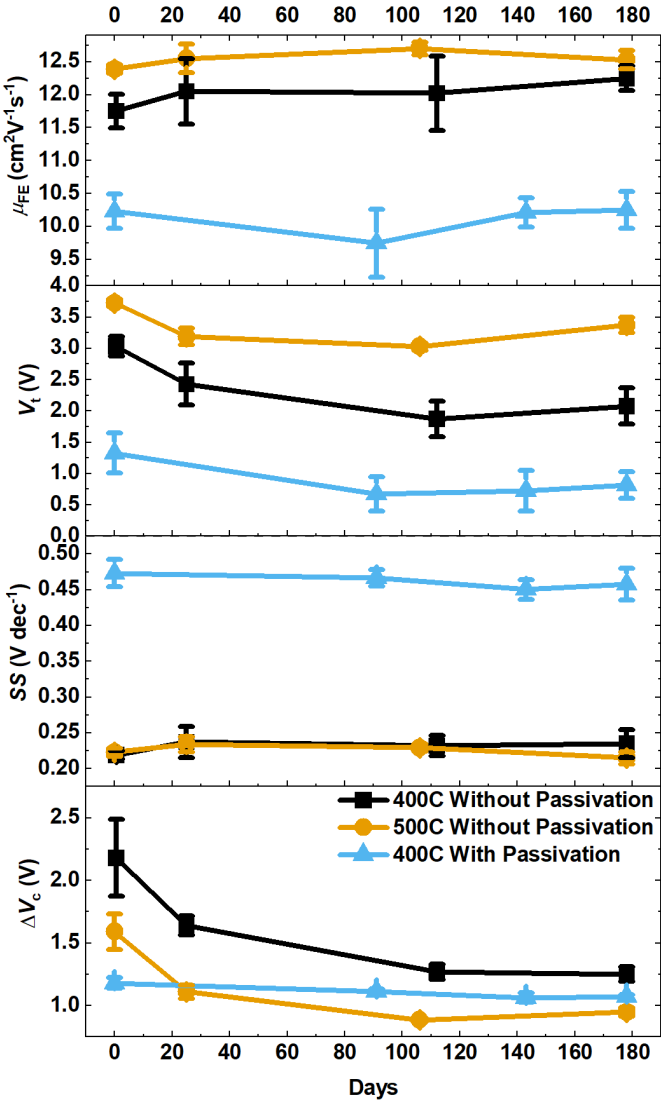

Fig. 3. Electrical characteristics of TFTs as they age. Symbols indicate the average of five measured devices and error bars indicate the standard deviation. The devices were aged at room temperature in a dark air ambient.

of aging agree within the measured standard deviation. (Five devices of each type were measured on each date.) The stability of μ_{FE} indicates the bulk tail acceptors at the conduction band edge do not change with time [32], while the stability of *SS* indicates a stable semiconductor/gate insulator interface [33]. There are, however, statistically significant decreases in V_t and ΔV_c within the first 25 days of aging (see Fig. 3).

It has previously been found for AOS TFTs that robustness to aging and bias stress varies with the ambient atmosphere [34], the thickness of the active layer [35], [36], active layer structure [37], and passivation [38], [39]. Ambient interactions can include the exchange of water and oxygen molecules, where water can act as an electron donor [35], [36] or an acceptor-like trap [40] and oxygen acts as an electron trap [35], [36], [40]. Passivation layers have been applied to prevent interactions with ambient molecules [35], [38], [39], [41]. Building on this literature, there are at least two possible explanations for the decrease in V_t with aging observed here. The first is the adsorption of water molecules that would then act as electron donors [35], [36]. This explanation is unlikely to apply here because water has been shown to act as an electron donor only in thicker AOS films [36] and adsorption/desorption of water should also correspond to an increase in hysteresis [40], which is not seen for these devices (see Fig. 3). The other, more likely explanation is an increase in the oxygen vacancies that are native defect dopants and the main contributor to free electrons in AOS materials [42]. As V_t stabilizes after 25 days of aging (see Fig. 3), the concentration of oxygen vacancies must reach an equilibrium value during that time due to kinetic constraints or a self-limiting reaction [43]. Hysteresis, however, continues to vary after 25 days of aging (see Fig. 3) because of interactions between ambient molecules and the exposed AOS surface, commonly referred to as the back-channel, requiring passivation to inhibit these interactions [27], [36].

TABLE II
AVERAGE ELECTRICAL CHARACTERISTICS OF TFTS. THE STANDARD DEVIATION FOR EACH VALUE IS SHOWN IN FIG. 3

		μ_{FE} ($cm^2V^{-1}s^{-1}$)	V_t (V)	SS (V dec^{-1})	ΔV_c (V)
400°C without passivation	**0-day**	11.8	3.03	0.220	2.18
	178-days	12.2	2.08	0.235	1.25
	Change	0.4	-0.95	0.015	-0.92
500°C without passivation	**0-day**	12.4	3.73	0.223	1.59
	178-days	12.5	3.37	0.215	0.949
	Change	0.1	-0.36	-0.008	-0.641
400°C with passivation	**0-day**	10.2	1.32	0.473	1.18
	178-days	10.3	0.815	0.458	1.07
	Change	0.1	-0.505	-0.015	-0.11

As the 400 °C and 500 °C annealed devices without passivation show similar trends with aging, studies implementing an Al_2O_3 passivation layer were only performed on devices with a 400 °C anneal as that process is within the 450 °C thermal budget for 3-D monolithic integration [44]. Like the samples without passivation, the passivated TFTs' μ_{FE} and SS values are largely invariant with aging, and V_t shows an initial shift and then stabilizes (see Fig. 3). The passivated TFTs show a smaller initial value of ΔV_C compared to the unpassivated devices, but ΔV_C shows the same trend: it decreases to a value of ∼1 V during the first 100 days of aging. Since the passivation layer is expected to largely inhibit ambient interactions, the residual ∼1 V of hysteresis observed may be due to the trapping and detrapping of electrons into defect states at the BC [43], [45].

Transfer characteristics for 400 °C annealed devices with and without passivation are shown in Fig. 4(a). From these transfer curves, there is a notable decrease in V_t and ΔV_c and an increase in SS with passivation. The reduction of ΔV_c with passivation is an expected result because the main contributor to hysteresis for devices without passivation–interactions between ambient molecules and the back-channel–is blocked by passivation, and is now attributed to BC defect states [40]. Silvaco ATLAS simulations [see Fig. 4(a)] performed with the parameters listed in Table I were used to explain the change in SS and V_t with passivation. The simulated Gaussian distribution of donor states at the BC [see Fig. 2(b)] creates a second parallel channel that results in a kink in the subthreshold I_D between −5 and −2 V V_{GS} [see Fig. 4(a)], while the tail donors increase the SS of the main channel [46]. The parallel negative shift in V_t was modeled by a positive fixed charge at the BC that may result from reactions with highly reactive trimethylaluminum or ozone [41], positive fixed charge in the bulk Al_2O_3 passivation layer [47], or defect modulation doping [48]. The kink in the subthreshold I_D is no longer present in the aged sample, indicating the reduction of BC states with time.

The TFT mobility after passivation was measured for five devices at each gate length. For TFTs with $L = 10$ μm, passivation reduces the average μ_{FE} from 11.8 to 10.2 $cm^2V^{-1}s^{-1}$, a reduction of ∼14%. The percentage change in μ_{FE} with passivation increases as L decreases, as shown in Fig. 4(b). This apparent μ_{FE} degradation as L decreases may be caused by non-negligible contact resistance, R_C. That is, as L decreases, R_C becomes a larger portion of the total resistance, effectively reducing the voltage, V_{DS}, across the channel by $I_{DS}R_C$. The μ_{FE} equation given above neglects R_C. It can be included by replacing V_{DS} with $V_{DS}-((R_C V_{DS})R_{Tot}^{-1})$, where $R_{Tot} = R_C + r_{ch}L$ and r_{ch} is the channel resistance [26]. To assess the impact of contact resistance, TLM measurements were used to extract r_{ch} and R_C values for devices with and without passivation, as shown in Fig. 4(c). As expected, r_{ch} decreases as V_{GS} increases (as the channel charge increases), while R_C stays constant. The fact that r_{ch} does not change with passivation indicates that the bulk ZTO is unchanged. In contrast, the value of R_C increases by approximately a factor of five after passivation. The measured R_C values are used to correct the extracted values of μ_{FE}. The analysis is plotted in Fig. 4(b). The corrected μ_{FE} values show no dependence on gate length, indicating that the 5× increase in R_C likely causes the apparent decrease in μ_{FE} following passivation.

During the passivation process, the sample is placed in an ALD chamber and exposed to a vacuum environment at 100 °C. These conditions may cause an increase in contact resistance with passivation. To test whether these conditions would increase the contact resistance, a sample with identical ZTO film was prepared and R_C was estimated. The fresh sample has an estimated contact resistance of about 6.89 Ω-cm, similar to the 0 day device without passivation (4.19 Ω-cm). To test whether a vacuum treatment would impact R_C, the sample was placed in a vacuum chamber for one hour and re-measured in an air ambient. Vacuum treatment caused the estimated R_C to increase to about 13.5 Ω-cm. Subsequently, the sample was annealed for one hour in a vacuum at 100 °C to test whether a vacuum anneal would change the contact resistance. After the vacuum annealing, the estimated R_C further increases to about 19.8 Ω-cm, similar to the 0-day device with passivation (20.0 Ω-cm). Therefore, the increase in contact resistance with passivation may be attributed to the coincidental vacuum anneal of the ALD passivation process. Contact resistance may increase during a vacuum anneal because the oxygen vacancies induced by the top metallization process [26], [49] will readily diffuse from the metal/semiconductor junction increasing the potential barrier and, therefore, the interfacial contact resistance [50]. Further work is required to verify these proposed mechanisms. Nonetheless, from the aging stability of μ_{FE} we can conclude that the contact resistance—after undergoing the one-time change induced during passivation—appears stable under aging.

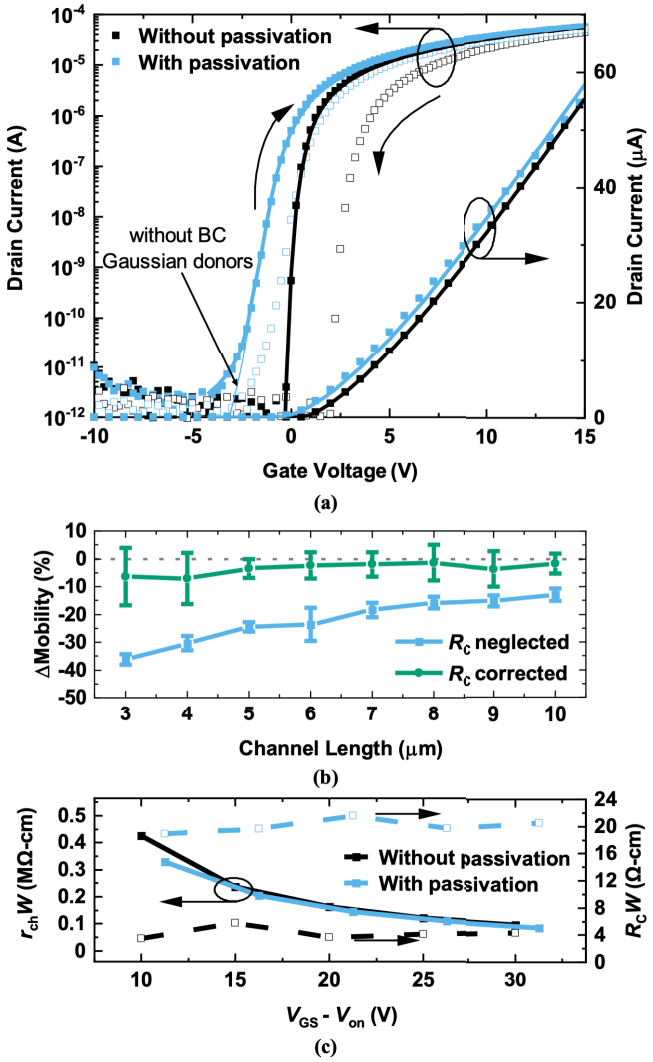

Fig. 4. (a) Experimental (symbols) and simulated (lines) I_D–V_{GS} curves of 0 day 400 °C annealed ZTO devices. Closed symbols indicate forward sweeps while open symbols indicate reverse sweeps. The experimental data is the same as that shown in Fig. 1(b). (b) Percent change in μ_{FE} due to passivation as a function of channel length for 0 day 400 °C annealed ZTO devices. R_C neglected (blue) does not account for V_{DS} dropped across the contacts while R_C corrected (green) does. Symbols and error bars indicate averages and standard deviations of five devices, respectively. (c) Width-normalized channel resistance (left y-axis) and contact resistance (right y-axis) as a function of V_{GS}-V_{on} as extracted using TLM for 0 day 400 °C annealed ZTO devices.

In contrast, the bias stress stability is dependent on the stress time and magnitude, where longer stress times and larger magnitudes generally result in larger changes [35], [36]. These changes can result from creation of defect states near the gate insulator/semiconductor interface [51], charge trapping in the gate insulator [52], or interactions with ambient molecules [53]. The reliability of the aged devices was studied by PBS and NBIS, and the results are shown in Fig. 5. Under PBS, there is an increase in V_t with increasing stress time for all samples. The source of the PBS for the 400 °C device without passivation is related to the interaction between the ambient oxygen and the back channel and can be described by the stretched exponential, $\Delta V_t(t) = \Delta V_{t0}[1-\exp(-(t/\tau)^{\beta})]$ where $\Delta V_{t0} = V_{\text{stress}} - V_t(t = 0\text{ s})$, β is the stretched exponential, and τ is the characteristic trapping time of carriers [53]. In the ΔV_t plot in Fig. 5, the filled symbols indicate the measured change in V_t with time while the line indicates the

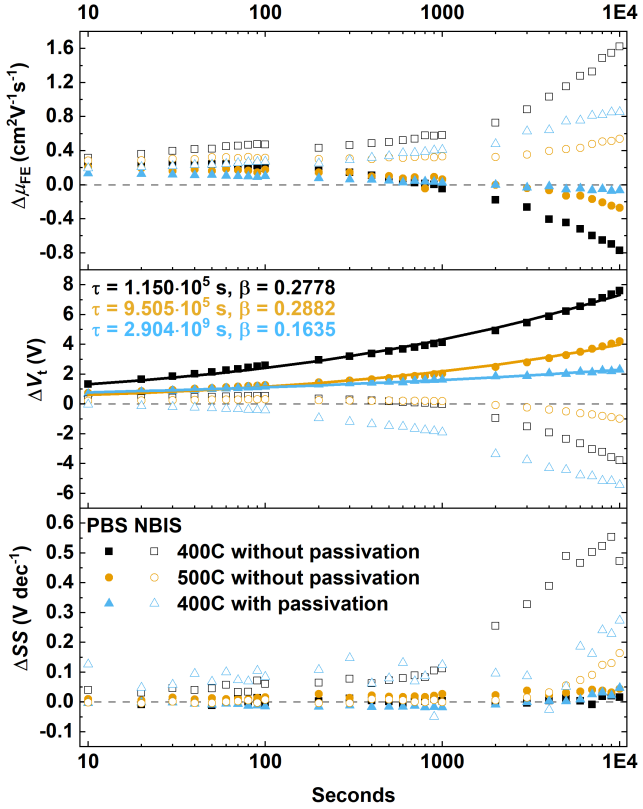

Fig. 5. Change in μ_{FE}, V_t, and SS with stress time. The filled symbols indicate PBS, the open symbols indicate NBIS, and the lines in the plot of ΔV_t are fits to the stretched-exponential equation for PBS ΔV_t.

$\Delta V_t(t)$ fit equation. For the devices without passivation, τ is on the order of 10^5 s which is in line with previous ZTO results attributed to oxygen adsorption [54]. After passivation, however, τ increases to approximately 10^9 s, indicating a significant increase in stability, as observed previously in IGZO [55]. Recent work on RF sputtered and microwave annealed IGZO reports a value of τ on the order of 10^8 s significantly better than our devices without passivation but an order of magnitude lower than our passivated devices, indicating our passivation process may offer a way to improve stability to PBS [56]. Without passivation, β is approximately 0.28 while after passivation it decreases to 0.16. These changes in τ and β indicate that the dominant charge trapping shifts from oxygen adsorption without passivation to interface states (likely the shallow Gaussian donors) after passivation, and that an improved passivation layer, with reduced interface states, could further reduce ΔV_t from PBS.

Under NBIS, there is a decrease in V_t with increasing stress time for all samples. The source of negative V_t shift in AOS materials with NBIS has been attributed to the photo-ionization of oxygen vacancy sites from V_O to V_O^{2+} which occurs under the combination of visible light ~2.3 eV and negative gate bias. These V_O^{2+} states contribute free electrons, causing parallel negative V_T shifts and persistent photoconductivity [57]. The neutral oxygen vacancy sites and/or local under-coordination of oxygen can be correlated with the simulated valence band tail-states with a density of $\sim 10^{20}$ cm^{-3} (see Fig. 2), and are experimentally observable in absorption spectra as subgap absorption [58], [59]. The larger negative V_t shift of the 400 °C samples with and without passivation, compared to that of the 500 °C sample, maybe due to a greater concentration of subgap defects. The

passivated sample exhibits the largest negative V_t shift with NBIS, likely due to the presence of donor-like tail states at the back channel/passivation interface [see Fig. 2(b)] [22], [60]. Between 1000 and 2000 s, $|\Delta V_t|$ exceeds 2.5 V, while similar work on ALD IGZO devices passivated with ALD Al_2O_3 showed $|\Delta V_t| = 2.5$ V after 3600 s [61] indicating there is room to improve our devices by lowering the interface state density at the passivation interface. In addition to a negative V_t shift, the 400 °C annealed sample without passivation shows a large increase in *SS* with increased NBIS time. The other two samples also show an increase in *SS* for stress times greater than approximately 4000 s. These *SS* increases may be due to changes in subgap defect states or interface states [51].

The mobility values for Fig. 5 were extracted using the same gate over-drive voltage for every measurement for a given sample to reduce the impact of ΔV_t on mobility extraction. Even with this method of extraction, there are clear trends in the mobility for samples without passivation where PBS causes a decrease in μ_{FE} and NBIS causes an increase in μ_{FE}. The decrease in μ_{FE} with PBS can be understood from the interaction of carriers with the chemisorbed oxygen that also causes the positive V_t shift. As the passivated sample does not suffer from interaction with ambient molecules, the $\Delta\mu_{\mathrm{FE}}$ with PBS is significantly reduced for that sample. The increase in $\mu_{\mathrm{FE}}$with NBIS can be understood as the increase in free carriers resulting in more band-like conduction with higher mobility.

IV. Conclusion

Understanding and improving the robustness of AOS TFTs fabricated using promising techniques such as ALD to aging and bias stress is critical for their adoption in beyond-display technologies. Here, we have investigated the robustness of BEOL-compatible zinc tin oxide n-TFTs with and without back-channel passivation. Devices without passivation exhibit slight changes within the first 25 days of aging and then excellent temporal stability. PBS instability, predominately caused by interactions with ambient molecules in samples without passivation, is significantly reduced for samples with passivation. However, the passivation method used here also causes an increase in contact resistance and *SS*, and does not completely eliminate NBIS instabilities. Future experiments considering different passivation/etch stop layer materials and processes, and informed by simulation, are needed to reduce the interface defect density at the back channel, and to confirm the physical mechanism driving the increased contact resistance following Al_2O_3 deposition.

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