This article has been accepted for publication in IEEE Electron Device Letters. This is the author's version which has not been fully edited and content may change prior to final publication. Citation information: DOI 10.1109/LED.2022.3219351

59.9 mV·dec^{-1} Subthreshold Swing Achieved in Zinc Tin Oxide TFTs with *in situ* Atomic Layer Deposited Al_2O_3 Gate Insulator

Tonglin L. Newsom, *Member, IEEE,* Christopher R. Allemang, *Member, IEEE*, Tae H. Cho, Neil P. Dasgupta, and Rebecca L. Peterson, *Senior Member, IEEE*

***Abstract*— Here, by depositing both the zinc tin oxide (ZTO) channel and Al_2O_3 gate dielectric layer using atomic layer deposition (ALD) without breaking vacuum, we made TFTs with a steep subthreshold swing (*SS*) of 59.9 mV·dec^{-1}, near the room temperature Boltzmann limit. An extremely low interface trap density of 9.59×10^9 cm^{-2}eV^{-1} was extracted from the measured *SS* value, and was corroborated by the high-low frequency capacitance method. Comparison with other TFT processes shows that both the higher-*k* gate dielectric and the *in situ* ALD process are required to obtain the low *SS* value. The device made with *in situ* dielectric deposition exhibits a maximum linear mobility of 19.2 cm^{2}V^{-1}s^{-1}, an ON/OFF current ratio > 10^8, and a threshold voltage of 1.3 V. The sharp *SS* achieved here will enable low voltage electronics using this scalable ALD technology.**

***Index Terms*—Amorphous semiconductors, semiconductor-insulator interfaces, thin film transistors**

I. Introduction

Over the past several decades, thin film transistor (TFT) development has been driven by the requirements of modern display technology. While today's high definition, high frame rate displays are enabled by amorphous metal oxide semiconductors (AOS) TFTs, AOS also have great potential for back-end-of-line (BEOL) 3D monolithic integration and flexible electronics [1]–[3]. There have been many studies of different AOS materials, such as In_2O_3 [4], InGaZnO (IGZO) [5]–[7], InZnO (IZO) [8], InGaSnO (IGTO) [9], and ZnSnO (ZTO) [2], [3], [10]. However, IGZO, IZO, and IGTO all contain indium, which is comparatively rare [11]. ZTO, in contrast, is made of common elements and has demonstrated excellent electron transport [2], [12]. ZTO can be deposited by many common process techniques including magnetron sputtering [13], solution processing [3], [14], pulsed laser deposition [15], [16], and atomic layer deposition (ALD) [2], [17], [18]. Our group has developed a BEOL-compatible ALD process to deposit ZTO thin films for n-type TFTs with mobility as high as 22.1 cm^{2}V^{-1}s^{-1} [2]. As future implementation of thin film circuitry requires energy-efficient, low-voltage switching, it is crucial to lower the subthreshold swing (*SS*) [3], [19]. In previous studies of ZTO TFTs, the lowest *SS* reported was 70 mV·dec^{-1}, achieved by solution processing using HfO_2 as the gate dielectric [20]. Given that the Boltzmann limit of *SS* at room temperature is ~60 mV·dec^{-1}, there is still potential to improve the *SS* in combination with adopting more scalable ZTO deposition technologies, such as ALD. The device community has explored various techniques to lower the *SS*, including tunneling FET architectures [21], incorporating a charge trapping layer [22], or using a negative capacitance (e.g. ferroelectric) gate material [23]. However, the adoption of these techniques in oxide TFTs faces significant challenges such as non-standard material integration or complex processes.

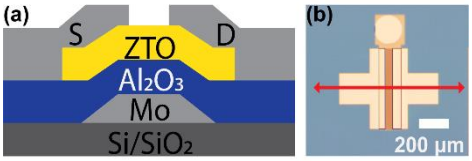

Fig. 1. (a) *in situ* ALD Al_2O_3 ZTO TFT device cross-section. (b) Optical image of the top-down view of a 500 × 50 μm ZTO TFT device.

In this work, we demonstrate a facile *in situ* process for ALD of the ZTO semiconductor and Al_2O_3 gate dielectric without breaking vacuum. The fabricated bottom-gate, top-contact TFTs operate using standard transistor physics and materials, and exhibit a high mobility and low threshold voltage. By minimizing the density of interface defects through the *in situ* process, we achieved a room temperature subthreshold swing value of 59.9 mV·dec^{-1} using a BEOL-compatible process.

This work was supported by National Science Foundation Scalable Nanomanufacturing award #1727918 and National Science Foundation Graduate Research Fellowship Program. Any opinion, findings, conclusions, or recommendations expressed in this publication are those of the authors and do not necessarily reflect the views of NSF. Portions of this work were performed in the Lurie Nanofabrication Facility, which is supported by the University of Michigan College of Engineering.

T. Newsom is with the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI 48109-2122 USA.

R. L. Peterson is with the Departments of Electrical Engineering and Computer Science, and Materials Science and Engineering, University of Michigan, Ann Arbor, MI 48109-2122 USA (e-mail: blpeters@umich.edu).

C. R. Allemang was with the Electrical Engineering and Computer Science Department, University of Michigan, Ann Arbor, MI 48109-2122 USA. He is now with Sandia National Laboratories, Albuquerque, NM 87185 USA.

T. Cho is with the Mechanical Engineering Department, University of Michigan, Ann Arbor, MI, MI 48109-2125 USA.

N. Dasgupta is with the Departments of Mechanical Engineering, and Materials Science and Engineering, University of Michigan, Ann Arbor, MI, MI 48109-2125 USA (email: ndasgupt@umich.edu).

II. Experimental Procedure

Bottom-gate, top-contact TFTs with channel width (W) of 500 μm and length (L) of 50 μm were fabricated. A schematic cross-section is shown in **Fig. 1(a)**. First, a heavily-doped silicon wafer with a 100 nm thermally-grown SiO_2 film was used as the substrate. To create the patterned gate electrode, approximately 100 nm of molybdenum (Mo) was sputtered onto the substrate and then patterned by XeF_2 etching. Then, approximately 30 nm Al_2O_3 was deposited for the gate insulator using an O_3-based ALD process at 200ºC. Next, without breaking vacuum, approximately 11 nm of ZTO with a Sn content of 21 at. % was deposited by ALD at 200ºC using a hybrid process for the active layer. The hybrid process uses H_2O as the oxidant following the Zn precursor, and O_2 plasma as the oxidant after the Sn precursor [2]. The ZTO film was then wet etched for device isolation before being annealed in a moisture-controlled glovebox for one hour at 400ºC in air with relative humidity < 20% [24]. Next, a via opening in the gate insulator was created by wet etch to allow probing of the gate electrode. Finally, approximately 100 nm of Mo was deposited by sputtering and patterned by lift-off to form the source and drain electrodes. The final fabricated device is shown in **Fig. 1(b)**. The devices were aged for > 6 months in air ambient to stabilize their performance [25]. Electrical measurements were taken in the dark at room temperature in air ambient using a HP4156A semiconductor parameter analyzer.

III. Results and Discussion

The transfer characteristics (I_D-V_{GS}) of an *in situ* ZTO TFT are shown in **Fig. 2(a)**. There is a hysteresis of around 61 mV. The ALD Al_2O_3 gate dielectric has a low leakage current density of 2.44×10^{-9} A/cm^2 at V_{GS} of +5 V, which is limited by measurement noise. Using metal-insulator-metal capacitors, a minimum breakdown voltage of 23.5 V was obtained, which corresponds to an applied electric field of 7.83 MV/cm. **Fig. 2(b)** shows the extracted *SS* value based on the experimental data. The *SS* of the forward sweep is 59.9 mV·dec^{-1}, while the *SS* of the reverse sweep is 61.7 mV·dec^{-1}. Since these values are nearly the same, we conclude that the low *SS* value is due to the ultra-clean interface between the *in situ* ALD Al_2O_3 and ALD ZTO. From six measured devices, the average minimum *SS* is 60.1 mV·dec^{-1} with a standard deviation of 0.3 mV·dec^{-1}. This is the lowest *SS* ever reported for ZTO TFTs.

The maximum linear mobility measured is 19.2 cm^{2}V^{-1}s^{-1} (**Fig. 2(c)**) at a gate voltage of 3.9 V, which was extracted using the method reported in [2]. This linear mobility value is in good agreement with the extracted saturation mobility of 15.6 cm^{2}V^{-1}s^{-1}. The high electron mobility is achieved through deposition of a dense ZTO film obtained by high-quality ALD growth combined with post-deposition annealing, as described in [2]. The measured threshold voltage is 1.3 V, obtained from the forward sweep. In **Fig. 2(a)**, the drain current reached 0.30 mA·mm^{-1}, while the off current is < 4×10^{-11} mA·mm^{-1}, which brings the ON/OFF current ratio >10^8.

A density of interface states, D_{it}, value of 9.59×10^9 cm^{-2}eV^{-1} was calculated directly from the measured *SS*, using **(1)**:

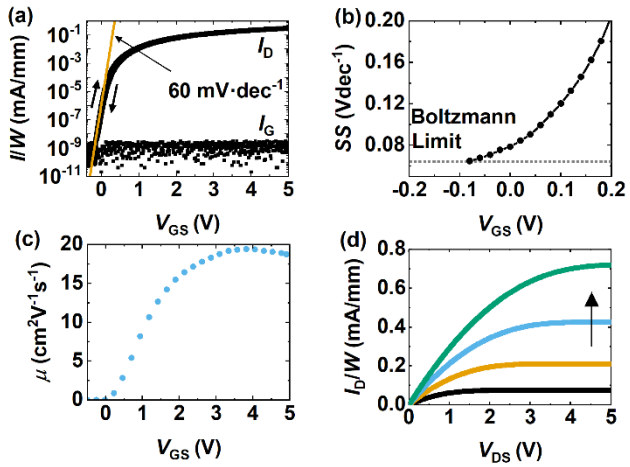

Fig. 2. Electrical characteristics of *in situ* ZTO TFT. (a) Transfer characteristic at a drain-source voltage (V_{DS}) of 1 V, where V_{GS} is the gate-source voltage with V_{GS} step of 20 mV, the drain current is I_D, the gate leakage current is I_G, and the fitted line indicates a *SS* value of 60 mV·dec^{-1} from the forward sweep. (b) *SS* and (c) linear mobility (μ) as a function of V_{GS}, extracted from the forward sweep data in (a). (d) Output characteristics for V_{GS} = 2, 3, 4, and 5 V.

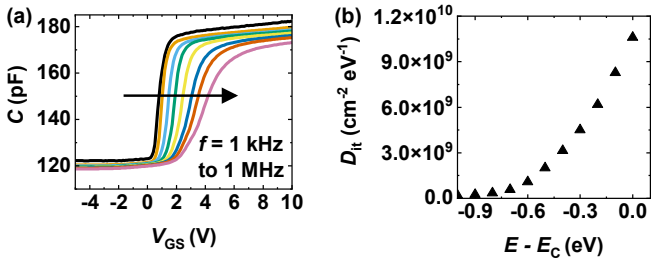

Fig. 3. (a) Measured *C-V* data for the *in situ* ZTO TFT. (b) Density of interface states (D_{it}), extracted using the high-low frequency method, as a function of position in the bandgap.

$$D_{it} = \frac{C_{ox}}{qWL}\left(\frac{SS}{kTln10} - 1\right). \quad (1)$$

Here, we used a C_{ox} value of 2.12×10^{-7} F·cm^{-2}. This capacitive density, which corresponds to a relative dielectric constant of 7.2, was measured using metal-insulator-metal structures (Mo/Al_2O_3/Mo). To corroborate this D_{it} value, capacitance-voltage (*C-V*) sweeps were performed over a frequency range of 1 kHz to 1 MHz (**Fig. 3(a)**). D_{it} as a function of position within the bandgap (**Fig. 3(b)**)was calculated using the high-low frequency analysis method [26]. The observed D_{it} value of 1.06×10^{10} cm^{-2}eV^{-1} near the edge of the conduction band is in good agreement with the D_{it} value obtained from *SS*.

To further clarify the importance of the *in situ* gate dielectric/semiconductor ALD process, we compared two other TFTs fabricated during previous process characterization. The first (**Fig. 4(a)**) uses a blanket layer of 100 nm Mo as the bottom gate and 30 nm of Al_2O_3 deposited with the same O_3 ALD process as the gate insulator. The second (**Fig. 4(b)**) uses a heavily-doped Si wafer as the bottom gate and 100 nm thermally-grown SiO_2 layer as the gate dielectric. The ZTO layer is deposited *ex situ* for both samples, i.e., vacuum is broken after the gate insulator deposition and the surface is exposed to atmosphere before active layer deposition. The ZTO layer for both *ex situ* devices was deposited at 150ºC, rather

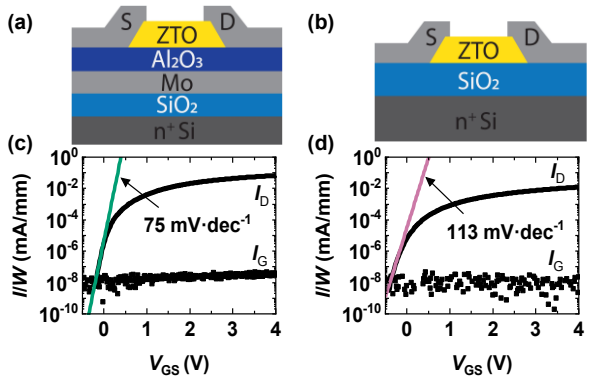

Fig. 4. Two other TFTs, shown for comparison. (a) Cross-sectional schematic and (c) transfer characteristics of *ex situ* Al_2O_3 TFT with V_{GS} step of 20 mV; (b) Cross-sectional schematic and (d) transfer characteristics of *ex situ* SiO_2 TFT with V_{GS} step of 20 mV.

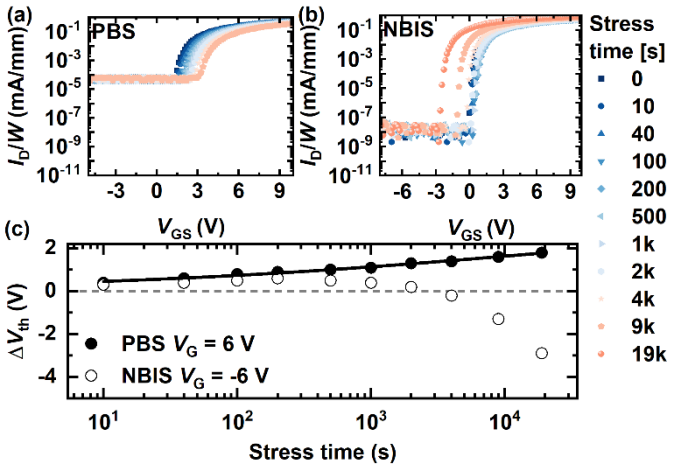

Fig. 5. Transfer characteristics during (a) PBS test (gate stress voltage of +6 V) and (b) NBIS test (gate stress voltage of -6 V). During stress, both the source and drain electrodes were grounded. In the transfer curve measurements for both (a) and (b), V_{DS} = 1 V and V_{GS} was swept with a step of 150 mV. (c) ΔV_{th} for PBS and NBIS, plotted against stress time. Measured data are indicated by symbols. The solid line indicates a fit to the PBS data using the stretched exponential function with fitting parameters of ΔV_{th0} = 2.6 V, τ = 9697 s, and β = 0.24. The large off current compared to Fig. 2a and change in off current floor in (a) and (b) are due to differing measurements conditions.

than at 200ºC, which was used for the *in situ* TFT to achieve higher TFT mobility. The post-deposition anneal conditions were identical to those used for the *in situ* sample. Based on our previous study [2], we do not expect the change in ZTO process temperature to affect the *SS* value.

The *ex situ* Al_2O_3 gate insulator TFT yields a *SS* of 75.3 mV·dec^{-1} (**Fig. 4(c)**) and D_{it} (extracted using **(1)**) of 3.66×10^{11} cm^{-2} eV^{-1}. The *ex situ* SiO_2 gate insulator TFTs yield a *SS* of 113 mV·dec^{-1} (**Fig. 4(d)**) and extracted D_{it} of 1.9×10^{11} cm^{-2} eV^{-1}. Compared to the *in situ* Al_2O_3 gate insulator, the comparison samples have D_{it} values that are a factor of 20 to 40 higher. We note that by replacing the low-*k* thermal SiO_2 gate insulator with a higher-*k* *ex situ* Al_2O_3 layer, the device *SS* is reduced due to the increased capacitive coupling, however D_{it} increased slightly. In contrast, the *in situ* ALD deposition process, in which the surface of Al_2O_3 is kept in vacuum and is not exposed to ambient air before ZTO deposition, dramatically reduces the D_{it}. This leads to an *SS* of 59.9 mV·dec^{-1}, which is very close to the theoretical Boltzmann limit at room temperature (**Fig. 2(b)**).

TABLE I
COMPARISON WITH OTHER BEOL-COMPATIBLE TFTS

Semiconductor Material & Deposition Method	Gate Insulator	*SS* [mV·dec^{-1}]	Ref.
ALD ZTO	***in situ* O$_3$-based ALD Al_2O_3**	**59.9**	**This Work**
	***ex situ* O$_3$-based ALD Al_2O_3**	**75.3**	**This Work**
	Thermal SiO_2	**113**	**This Work**
Solution-processed ZTO	AlO_x	96	[27]
	HfO_2	70	[20]
RF Sputtered IGZO	HfO_2	70	[28]
	Al_xO_y	68	[29]
	SiO_2/HfO_2	96	[30]
Exfoliated MoS_2	HfO_2	74	[31]
	Y_2O_3/HfO_2	65	[32]

Positive bias stress (PBS) and negative bias illumination stress (NBIS) tests were done to assess device stability (**Fig. 5**). For PBS, the positive shift in threshold voltage, ΔV_{th} versus stress time was fit to the stretched exponential function $\Delta V_{th} = \Delta V_{th0}\ \{1 - \exp[-(t/\tau)^{\beta}]\}$, where ΔV_{th0} is the ΔV_{th} at infinite time, τ is the trapping time of carriers, and β is the stretched-exponential exponent [33]. This model is based on the hypothesis that trapped charges redistribute into deep states within the dielectric during stress. For our data, ΔV_{th0} = 2.6 V, τ = 9697 s, and β = 0.24, within the expected range [33], [34].

For NBIS, a green LED (520 nm) with a power density of 957 μW/cm^2 was used. The NBIS data in **Fig. 5(b)** shows a negative V_{th} shift as stress progresses. The NBIS shifts, which have been observed previously for amorphous oxides, are typically attributed to ionization of oxygen vacancies, leading to an increase in donor-like states [34].

When compared to other reports (**Table I**), the *in situ* ZTO TFTs demonstrated here have the lowest *SS* value of all BEOL-compatible TFTs made using non-steep slope transistor architectures. Moreover, the *in situ* ALD process demonstrated here allows BEOL 3D monolithic integration of low voltage thin film electronics within a low thermal budget, using standard process modules.

IV. Conclusion

In this work, bottom-gate, top-contact n-TFTs were fabricated using an *in situ* ALD Al_2O_3 and ALD ZTO process without breaking vacuum. The TFTs exhibit a high linear mobility of 19.2 cm^{2}V^{-1}s^{-1}, a low threshold voltage of 1.3 V, and an ON/OFF current ratio greater than 10^8. By using an *in situ* O_3-based ALD Al_2O_3 gate insulator with a low interface defect density, we achieved a *SS* of 59.9 mV·dec^{-1}, the steepest *SS* reported to date for BEOL-compatible TFTs, and very close to the theoretical Boltzmann limit at room temperature. This low *SS* ZTO TFT fabrication process paves the way for future BEOL-compatible, low-voltage TFT technologies to support 3D monolithic integration.

V. References

[1] H. Hosono, "Transparent amorphous oxide semiconductors: Materials design, electronic structure, and device applications," in *2017 75th Annu. Device Res. Conf. (DRC)*, Jun. 2017, pp. 1–2. doi: 10.1109/DRC.2017.7999387.

[2] C. R. Allemang *et al.*, "High-Performance Zinc Tin Oxide TFTs with Active Layers Deposited by Atomic Layer Deposition," *Adv. Electron. Mater.*, vol. 6, no. 7, p. 2000195, Jun. 2020, doi: 10.1002/aelm.202000195.

[3] Y. Son, B. Frost, Y. Zhao, and R. L. Peterson, "Monolithic integration of high-voltage thin-film electronics on low-voltage integrated circuits using a solution process," *Nat. Electron.*, vol. 2, no. 11, pp. 540–548, Nov. 2019, doi: 10.1038/s41928-019-0316-0.

[4] M. Si, A. Charnas, Z. Lin, and P. D. Ye, "Enhancement-Mode Atomic-Layer-Deposited In_2O_3 Transistors With Maximum Drain Current of 2.2 A/mm at Drain Voltage of 0.7 V by Low-Temperature Annealing and Stability in Hydrogen Environment," *IEEE Trans. Electron Devices*, vol. 68, no. 3, pp. 1075–1080, Mar. 2021, doi: 10.1109/TED.2021.3053229.

[5] J. Sheng *et al.*, "Amorphous IGZO TFT with High Mobility of ~70 $cm^2/(V\ s)$ via Vertical Dimension Control Using PEALD," *ACS Appl. Mater. Interfaces*, vol. 11, no. 43, pp. 40300–40309, Oct. 2019, doi: 10.1021/acsami.9b14310.

[6] M. H. Cho, C. H. Choi, H. J. Seul, H. C. Cho, and J. K. Jeong, "Achieving a Low-Voltage, High-Mobility IGZO Transistor through an ALD-Derived Bilayer Channel and a Hafnia-Based Gate Dielectric Stack," *ACS Appl. Mater. Interfaces*, vol. 13, no. 14, pp. 16628–16640, Apr. 2021, doi: 10.1021/acsami.0c22677.

[7] L. Zhu *et al.*, "High-Performance Amorphous InGaZnO Thin-Film Transistor Gated by $HfAlO_x$ Dielectric With Ultralow Subthreshold Swing," *IEEE Trans. Electron Devices*, vol. 68, no. 12, pp. 6154–6158, Dec. 2021, doi: 10.1109/TED.2021.3117492.

[8] S. Hu *et al.*, "Effect of Al_2O_3 Passivation Layer and Cu Electrodes on High Mobility of Amorphous IZO TFT," *IEEE J. Electron Devices Soc.*, vol. 6, pp. 733–737, 2018, doi: 10.1109/JEDS.2018.2820003.

[9] M. Nakata *et al.*, "A method for shortening effective channel length in oxide TFT by partial formation of conductive region," *Jpn. J. Appl. Phys.*, vol. 58, no. 9, p. 090602, Apr. 2019, doi: 10.7567/1347-4065/ab12f1.

[10] H. Yang, J. Li, X. Zhou, L. Lu, and S. Zhang, "Self-Aligned Top-Gate Amorphous Zinc-Tin Oxide Thin-Film Transistor With Source/Drain Regions Doped by Al Reaction," *IEEE J Electron Devices Soc*, vol. 9, pp. 653–657, 2021, doi: 10.1109/JEDS.2021.3094281.

[11] P. Schlupp, F.-L. Schein, H. von Wenckstern, and M. Grundmann, "All Amorphous Oxide Bipolar Heterojunction Diodes from Abundant Metals," *Adv. Electron. Mater.*, vol. 1, no. 1–2, p. 1400023, 2015, doi: 10.1002/aelm.201400023.

[12] M. R. Shijeesh, P. A. Mohan, and M. K. Jayaraj, "Complementary Inverter Circuits Based on p-Cu_2O and n-ZTO Thin Film Transistors," *J. Electron. Mater.*, vol. 49, no. 1, pp. 537–543, Jan. 2020, doi: 10.1007/s11664-019-07704-7.

[13] S. Yu, W. Xu, H. Zhu, W. Qiu, Q. Fu, and L. Kong, "Effect of sputtering power on structure and properties of ZTO films," *J. Alloys Compd.*, vol. 883, p. 160622, Nov. 2021, doi: 10.1016/j.jallcom.2021.160622.

[14] Q. Zhang, G. Xia, L. Li, W. Xia, H. Gong, and S. Wang, "High-performance zinc-tin-oxide thin film transistors based on environment friendly solution process," *Curr. Appl. Phys.*, vol. 19, no. 2, pp. 174–181, Feb. 2019, doi: 10.1016/j.cap.2018.10.012.

[15] B. Lu *et al.*, "Memristors based on amorphous ZnSnO films," *Mater. Lett.*, vol. 249, pp. 169–172, Aug. 2019, doi: 10.1016/j.matlet.2019.04.086.

[16] S. Yue *et al.*, "Ultrathin-Film Transistors Based on Ultrathin Amorphous InZnO Films," *IEEE Trans. Electron Devices*, vol. 66, no. 7, pp. 2960–2964, Jul. 2019, doi: 10.1109/TED.2019.2913866.

[17] B. D. Ahn, D. Choi, C. Choi, and J.-S. Park, "The effect of the annealing temperature on the transition from conductor to semiconductor behavior in zinc tin oxide deposited atomic layer deposition," *Appl. Phys. Lett.*, vol. 105, no. 9, p. 092103, Sep. 2014, doi: 10.1063/1.4895102.

[18] J. Heo, S. Bok Kim, and R. G. Gordon, "Atomic layer deposited zinc tin oxide channel for amorphous oxide thin film transistors," *Appl. Phys. Lett.*, vol. 101, no. 11, p. 113507, Sep. 2012, doi: 10.1063/1.4752727.

[19] L. Zhang, J. Huang, and M. Chan, "Steep Slope Devices and TFETs," in *Tunneling Field Effect Transistor Technology*, L. Zhang and M. Chan, Eds. Cham: Springer International Publishing, 2016, pp. 1–31. doi: 10.1007/978-3-319-31653-6_1.

[20] A. Liu *et al.*, "Redox Chloride Elimination Reaction: Facile Solution Route for Indium-Free, Low-Voltage, and High-Performance Transistors," *Adv. Electron. Mater.*, vol. 3, no. 3, p. 1600513, 2017, doi: 10.1002/aelm.201600513.

[21] G. Musalgaonkar, S. Sahay, R. S. Saxena, and M. J. Kumar, "Nanotube Tunneling FET With a Core Source for Ultrasteep Subthreshold Swing: A Simulation Study," *IEEE Trans. Electron Devices*, vol. 66, no. 10, pp. 4425–4432, Oct. 2019, doi: 10.1109/TED.2019.2933756.

[22] A. Daus *et al.*, "Charge Trapping Mechanism Leading to Sub-60-mV/decade-Swing FETs," *IEEE Trans. Electron Devices*, vol. 64, no. 7, pp. 2789–2796, Jul. 2017, doi: 10.1109/TED.2017.2703914.

[23] M. Si *et al.*, "Steep-slope hysteresis-free negative capacitance MoS_2 transistors," *Nat. Nanotechnol.*, vol. 13, pp. 24–28, Jan. 2018, doi: 10.1038/s41565-017-0010-1.

[24] Y. Son, A. Liao, and R. Peterson, "Effect of Relative Humidity and Pre-Annealing Temperature on Spin-Coated Zinc Tin Oxide Film Made via Metal-Organic Decomposition Route," *J Mater Chem C*, vol. 5, Jul. 2017, doi: 10.1039/C7TC02343J.

[25] C. R. Allemang, T. H. Cho, N. P. Dasgupta, and R. L. Peterson, "Robustness of Passivated ALD Zinc Tin Oxide TFTs to Aging and Bias Stress," *IEEE Trans. Electron Devices*, in press 2022, doi: 10.1109/TED.2022.3216791.

[26] D. K. Schroder, *Semiconductor Material and Device Characterization*, 3rd edition. Hoboken, NJ: John Wiley & Sons, Inc., 2015.

[27] C. Avis and J. Jang, "High-performance solution processed oxide TFT with aluminum oxide gate dielectric fabricated by a sol–gel method," *J. Mater. Chem.*, vol. 21, no. 29, pp. 10649–10652, Jul. 2011, doi: 10.1039/C1JM12227D.

[28] S. Samanta *et al.*, "Low Subthreshold Swing and High Mobility Amorphous Indium–Gallium–Zinc-Oxide Thin-Film Transistor With Thin HfO_2 Gate Dielectric and Excellent Uniformity," *IEEE Electron Device Lett.*, vol. 41, no. 6, pp. 856–859, Jun. 2020, doi: 10.1109/LED.2020.2985787.

[29] W. Cai *et al.*, "One-Volt IGZO Thin-Film Transistors With Ultra-Thin, Solution-Processed Al_xO_y Gate Dielectric," *IEEE Electron Device Lett.*, vol. 39, no. 3, pp. 375–378, Mar. 2018, doi: 10.1109/LED.2018.2798061.

[30] L.-Y. Su, H.-Y. Lin, H.-K. Lin, S.-L. Wang, L.-H. Peng, and J. Huang, "Characterizations of Amorphous IGZO Thin-Film Transistors With Low Subthreshold Swing," *IEEE Electron Device Lett.*, vol. 32, no. 9, pp. 1245–1247, Sep. 2011, doi: 10.1109/LED.2011.2160931.

[31] B. Radisavljevic, A. Radenovic, J. Brivio, V. Giacometti, and A. Kis, "Single-layer MoS_2 transistors," *Nat. Nanotechnol.*, vol. 6, pp. 147–50, Jan. 2011, doi: 10.1038/nnano.2010.279.

[32] X. Zou *et al.*, "Interface Engineering for High-Performance Top-Gated MoS_2 Field-Effect Transistors," *Adv. Mater.*, vol. 26, no. 36, pp. 6255–6261, 2014, doi: https://doi.org/10.1002/adma.201402008.

[33] I.-T. Cho, J.-M. Lee, J.-H. Lee, and H.-I. Kwon, "Charge trapping and detrapping characteristics in amorphous InGaZnO TFTs under static and dynamic stresses," *Semicond. Sci. Technol.*, vol. 24, no. 1, p. 015013, Jan. 2009, doi: 10.1088/0268-1242/24/1/015013.

[34] S.-J. Seo, J. H. Jeon, Y. H. Hwang, and B.-S. Bae, "Improved negative bias illumination instability of sol-gel gallium zinc tin oxide thin film transistors," *Appl. Phys. Lett.*, vol. 99, no. 15, p. 152102, Oct. 2011, doi: 10.1063/1.3646388.