NANO LETTERS

pubs.acs.org/NanoLett

Letter

An Ultra-steep Slope Two-dimensional Strain Effect Transistor

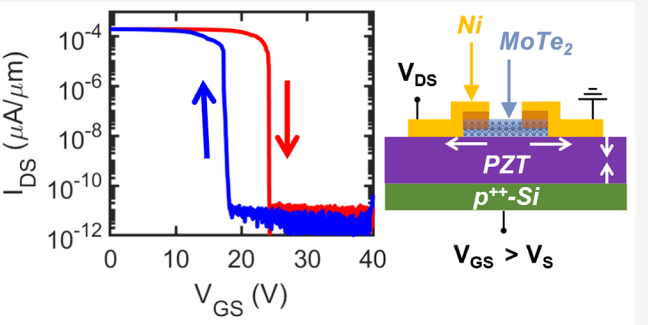
Sarbashis Das and Saptarshi Das*

Cite This: *Nano Lett.* 2022, 22, 9252–9259

Read Online

ACCESS | Metrics & More | Article Recommendations | Supporting Information

ABSTRACT: We introduce a high-performance and ultra-steep slope switch, referred to as strain effect transistor (SET), with a subthreshold swing < 0.68 mV/decade at room temperature for 7 orders of magnitude change in the source-to-drain current based on atomically thin 1T′-$MoTe_2$ as the channel material, piezoelectric lead zirconate titanate (PZT) as the gate dielectric, and nickel (Ni) as the source/drain contact metal. We exploit gate-voltage induced strain transduction in PZT leading to abrupt and reversible cracking of the metal contacts to achieve the abrupt switching. The SET also exhibits a low OFF-state current < 1 pA/μm, a high ON-state current > 1.8 mA/μm at a supply voltage of 1 V, a large current ON/OFF ratio > 1 × 10^9, and a high transconductance of > 100 μS/μm. The switching delay for the SET was found to be < 5 μs, and no device failure was observed even after 1 million (1 × 10^6) switching cycles.



KEYWORDS: *2D material, $MoTe_2$, straintronics, transistor, steep slope*

For more than eight decades, the semiconductor industry has witnessed relentless growth across all sectors of modern society driven by the advancements in silicon-based complementary metal oxide semiconductor (CMOS) technology, which in turn has been aided by material discoveries,[1] improvements in device structures,[2] optimizations at the circuit and architectural levels,[3] and progress in micro- and nano-lithography techniques.[4] Aggressive channel length scaling of metal oxide semiconductor field effect transistors (MOSFETs), allowing more devices to be assembled per unit area while keeping the power density almost constant, has been the driving philosophy behind the CMOS technology in the Dennard era, leading to orders of magnitude improvements in the computing capabilities of modern processors compared to their performance at their inception.[5] Unfortunately, the golden era of MOSFET scaling has now ended since both energy and dimension scaling appear to be fundamentally challenged.[6]

The stagnation in energy scaling is a direct consequence of nonscalability of the subthreshold swing (SS), which is defined as the gate voltage (V_{GS}) required to change the source-to-drain current (I_{DS}) of a MOSFET by 1 order of magnitude, to below 60 mV/decade at room temperature, also known as the Boltzmann tyranny.[7] This leads to an exponential increase in the OFF-state current (I_{OFF}) when scaling the threshold voltage (V_T) of the MOSFET, $I_{OFF} = 10^{-V_T/SS}$. To mitigate this challenge, novel devices and structures have been proposed. Tunnel field effect transistor (TFET), which exploits the electrostatic control of band-to-band tunneling to achieve steep slope switching is the forerunner in this context.[8] Ever since the first TFET based on carbon nanotube (CNT) achieved an SS = 40 mV/decade,[9] the field has grown to include Si TFETs,[10] III−V material-based TFETs,[11,12] MoS_2−Ge TFET,[13] and black phosphorus TFETs[14,15] among others. While extensive research in this field has produced some very impressive results like SS = 3.9 mV/decade[13] and an ON current value of ∼15 μA/μm,[15] only a countable number of studies (< 25) report sub-60 mV/decade SS and almost all studies observe steep slope for only 1−2 orders of magnitude change in the I_{DS}. While the concept of TFET is fundamentally sound, limited experimental success has stymied the progress in this field in recent years.[16]

Negative capacitance field effect transistors (NCFETs), which exploit a ferroelectric gate stack to achieve steep slope switching, offer another alternative for low-power circuits[17] where SS < 20 mV/decade has been reported experimentally.[18] NCFETs triumph over TFETs in their ability to achieve high ON current. In addition, this field has recently gained momentum owing to the development of doped hafnium oxide (HfO_2)-based ferroelectrics, which can be aggressively scaled and integrated with silicon.[19−21] However, material and interface nonidealities including defects, charge trapping, etc., can severely limit HfO_2-based NCFETs from achieving steep

Received: May 31, 2022
Revised: October 21, 2022
Published: November 23, 2022

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

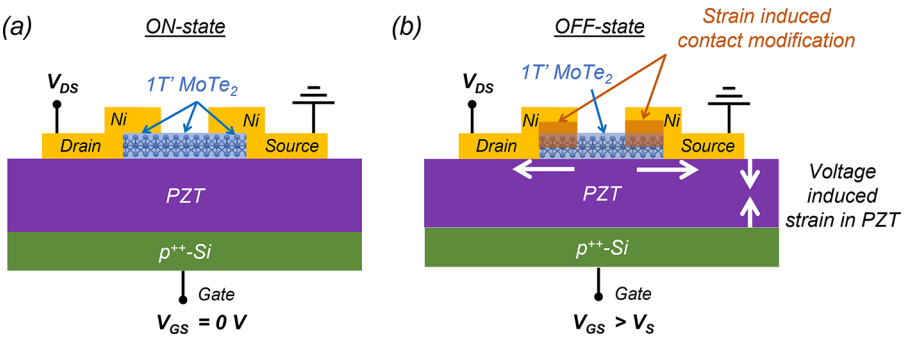


Figure 1. Operating principle of the strain effect transistor (SET). Schematic representation of SET operation in (a) ON-state and (b) OFF-state. When no gate voltage (V_{GS}) is applied to the PZT, the device is in the ON-state allowing current to flow between the source and the drain terminal owing to the semimetallic nature of 1T′-$MoTe_2$. With any finite $V_{GS} > 0$ V, the PZT is subjected to an out-of-plane electric field resulting in an out-of-plane strain, which is translated as in-plane strain on the 1T′-$MoTe_2$ channel and the Ni contacts since the volume of PZT must remain constant. As V_{GS} increases, the strain also increases, and finally, when V_{GS} exceeds a critical value, V_S, the strain crosses the threshold where the Ni contact physically cracks or delaminates from the $MoTe_2$ channel and abruptly breaks the electrical conduction path, leading to steep slope switching from the ON- to the OFF-state.

slope switching. Moreover, the community still appears to be divided over the fundamental concept of negative capacitance with both sides having valid arguments.[22,23]

Phase change materials (PCMs) show abrupt phase transition from metal to insulator phase. They form another major class of devices where steep slope switching has been explored.[24,25] However, since they are two-terminal devices, they cannot be gate modulated. Devices like the phase change TFET use a PCM in series with a TFET to mitigate the aforementioned challenge but fail to achieve high ON/OFF current ratio.[26] While TFET, NCFET, PCM are promising steep slope devices, they still present nonzero I_{OFF}. Nano electromechanical switches (NEMS) can mitigate this challenge as these are contact-based switches comprising a mobile structure that is deflected using electrostatic forces until it reaches physical contact with an electrode, forming a path that allows current to flow. The no-contact OFF state of NEMS ensures near zero I_{OFF} and at the same time the switching can be infinitely abrupt. In fact SS as low as 0.285 mV/decade has been achieved using CMOS/NEMS hybrid designs.[27] Finally, while steep slope and low-I_{OFF} are critical needs for future low-power devices, transconductance (g_m) is an equally important metric that determines whether a switch can offer signal amplification. Unfortunately, NEMS devices cannot be used for this purpose. Nevertheless, the above discussion summarizes the basic technology requirements for a low-power and high-performance switch, which include steep slope switching (SS < 60 mV/decade), large current ON/OFF ratio, low OFF-state current, high ON-state current, and high transconductance.[28]

In this work, we demonstrate a novel switching device, referred to as two-dimensional (2D) strain effect transistor (SET) that not only overcomes the nonscalability of SS imposed by thermodynamic limitations in MOSFETs and achieves SS < 0.68 mV/decade at room temperature for 7 orders of magnitude change in I_{DS} but also exhibits a record high ON current of ∼1.8 mA/μm at a supply voltage of 1 V, a current ON/OFF ratio of > 1×10^9, a low OFF current of 1 pA/μm, and a record high transconductance of > 100 μS/μm. The SET operates on the principle of voltage-induced strain transduction via a piezoelectric gate stack leading to a reversible cracking or delamination of the metal contacts. We also found that the device can switch in faster than 5 μs and no catastrophic failure occurs even after 1 million (1×10^6) switching cycles. Earlier studies have shown that electrically reversible nanoscale cracks can occur in an intermetallic thin film grown on a ferroelectric substrate driven by a small electric field.[29] Here, we observe a similar phenomenon but at the metal/2D van der Waals interface.

Figure 1 explains the operation of the SET schematically. We have used molybdenum ditelluride ($MoTe_2$) in its orthorhombic (1T′) crystal structure, which is a layered 2D semimetal as the channel material, lead zirconate titanate (PZT), which is a well-known piezoelectric as the gate dielectric, and nickel (Ni), which is a high tensile strength material as the source/drain contact. A 2 μm film of PZT is grown on a p^{++}-Si substrate using the sol−gel growth technique to serve as the back-gate.[30] Commercially available ultra-thin flakes of 1T′-$MoTe_2$ are exfoliated on top of the PZT layer. Source/drain contacts are subsequently patterned on the flakes using electron beam (e-beam) lithography followed by e-beam evaporation of 40/30 nm Ni/Au and finally lift-off. Details about the fabrication and characterization processes of these devices can be found in the Fabrication Methods section in the Supporting Information. Clearly, the device structure resembles that of a MOSFET, yet a radically different approach is used by the SET to switch between the ON and the OFF state. When no gate voltage (V_{GS}) is applied to the PZT (Figure 1a), the device is in the ON-state since a large I_{DS} flows between the source and the drain terminal owing to the semimetallic nature of 1T′-$MoTe_2$. With any finite $V_{GS} > 0$ V, the PZT is subjected to an out-of-plane electric field resulting in an out-of-plane strain, which is translated as an in-plane strain on the channel and the source/drain contacts since the volume of the PZT must remain constant. $MoTe_2$ has a van der Waals layered structure with the absence of dangling bonds, while Ni crystallizes in the form of a face-centered cubic structure. The dissimilarities between the $MoTe_2$ in the channel and the Ni in the contacts make the interface between the contact and the channel less adhesive. As V_{GS} increases, the strain also increases, and finally, when V_{GS} exceeds a critical value, V_S, the strain crosses the threshold where the Ni contact physically cracks/delaminates from the $MoTe_2$ channel and abruptly breaks the electrical conduction path leading to steep slope switching from the ON to the OFF state (Figure 1b).

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

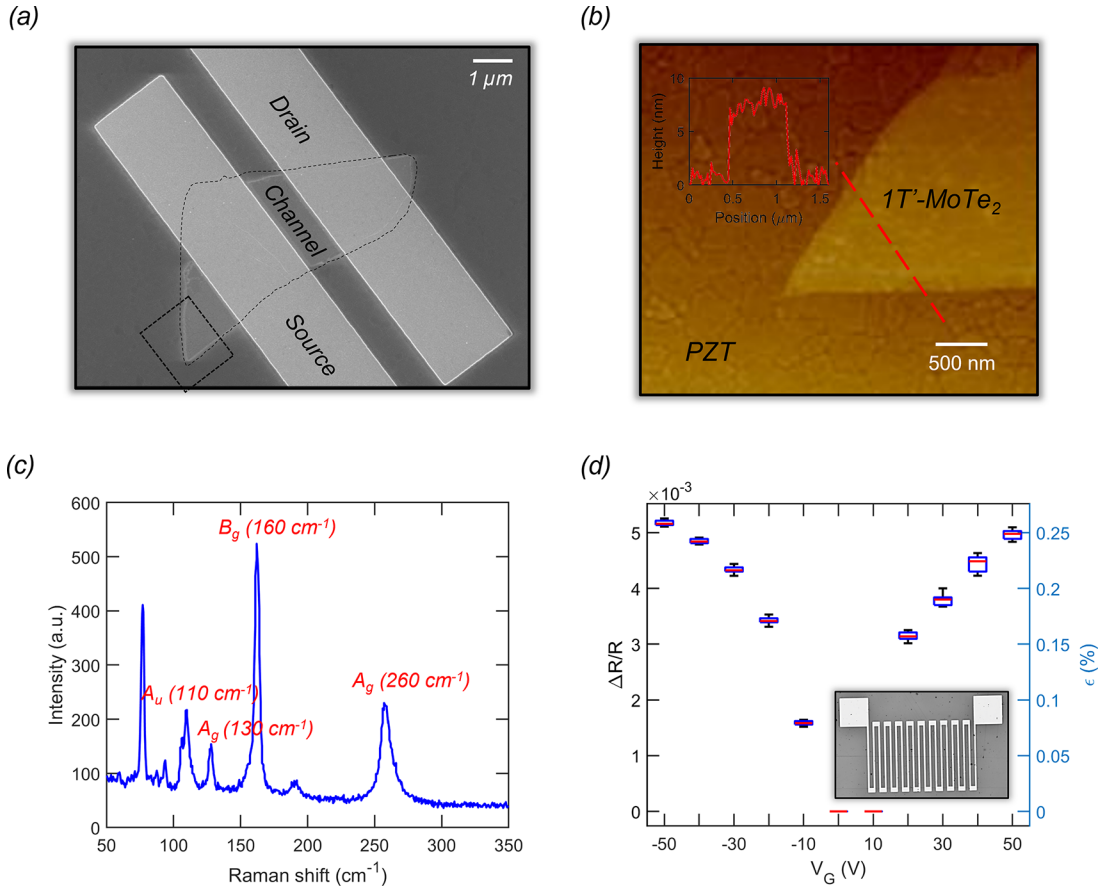


Figure 2. Characterization of $MoTe_2$ and PZT. (a) Scanning electron microscope (SEM) image of a representative SET. (b) Atomic force microscope (AFM) image and the height profile of the $MoTe_2$ showing 7.6 nm flake thickness. (c) Raman spectra of the $MoTe_2$ flake with the prominent peak corresponding to the B_g mode at 160 cm^{-1}, whereas the weaker A_g mode has peaks at 130 and 260 cm^{-1}, and the A_u mode has a peak at 110 cm^{-1}, confirming that the flake is in the 1T′ phase with few layers. (d) Fractional change in the resistance of a Ni-based strain gauge structure (shown in the inset) as a function of the voltage across the PZT film (V_G) used for calibrating the in-plane strain (ϵ). A gauge factor of 2 was used for the Ni thin film.

Figure 2a shows the scanning electron microscope (SEM) image of a representative SET and Figure 2b shows the atomic force microscope (AFM) image of the flake with the height profile shown in the inset. The flake thickness was found to be ∼7.6 nm. Figure 2c shows the Raman spectra of the $MoTe_2$ flake with the prominent peak corresponding to the B_g mode at 160 cm^{-1}, whereas the weaker A_g mode has peaks at 130 and 260 cm^{-1}, and the A_u mode has a peak at 110 cm^{-1}, confirming that the flake is in the 1T′ phase with few layers.[31] The X-ray diffraction (XRD) of the PZT film indicates a strong (100) orientation with a Lotgering factor > 98%.[32] The capacitance versus electric field measurement for the PZT film, was found to follow the characteristic butterfly shape with the relative dielectric constant reaching a maximum value of ∼1350.[30] Finally, Figure 2d shows the fractional change in resistance ($\Delta R/R$) of a Ni-based strain gauge structure (shown in the inset) as a function of the gate voltage (V_G) used for calibrating the in-plane strain (ϵ). A gauge factor of 2 was used for Ni considering its thin film nature.[33]

Figure 3a shows the room temperature transfer characteristics, i.e., I_{DS} versus V_{GS} for V_{DS} = 100 mV, in the logarithmic scale, for a representative SET with 1 μm channel length (L) and 1.5 μm channel width (W). Since the starting material is metallic, the device is in the ON-state at V_{GS} = 0 V with ON current of ∼0.2 mA/μm. When V_{GS} is increased, the electric field across the PZT leads to an in-plane strain on the 1T′-$MoTe_2$ underneath the contacts. Once V_{GS} reaches V_S, the Ni contact to the $MoTe_2$ channel delaminates/cracks and loses electrical contact which switches off the device with I_{OFF} ∼ 1 pA/μm. Note that I_{OFF} is determined by the noise floor of the instrument. When V_{GS} is swept back from 40 to 0 V, the reverse process is triggered at a lower V_S, resulting in a clockwise hysteresis in the transfer characteristics of the SET.

Figure 3b shows the zoomed-in region where the device is turning off. Note that a V_{GS} step size of 4 mV was used for this measurement. The SS was found to be 1.6 mV/decade and 6 mV/decade when averaged over 3 and 6 orders of magnitude change, respectively, in the I_{DS}. In fact, as shown in Figure S1a, b, another device demonstrated SS value < 0.68 mV/decade for 7 orders of magnitude change in the I_{DS}, although V_S was found to be ∼45 V for the forward sweep and ∼40 V for the reverse sweep. The device-to-device variations seen in V_S can be attributed to the variations in the thickness of the exfoliated 1T′-$MoTe_2$ flakes and their adhesion with Ni, and PZT substrate, as well as the multigrain nature of the PZT film, which we believe can be mitigated through large area growth of 1T′-$MoTe_2$. Nevertheless, SS values reported here are found to be among record low numbers comparable to NEMS switches[27] and at least an order of magnitude better than TFETs,[34,35] NCFETs,[18,36] and PCMs[26] and almost 2 orders of

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

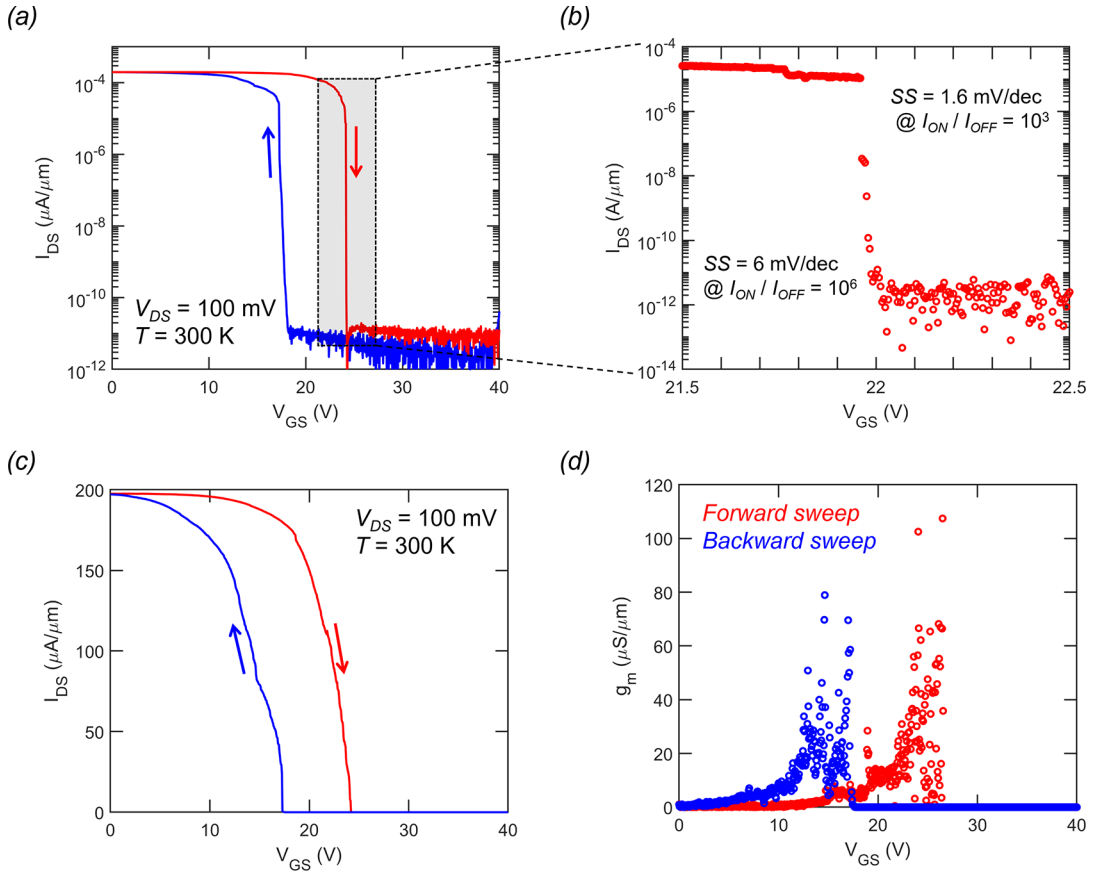


Figure 3. Experimental demonstration of ultra-steep slope and high transconductance in the SET. (a) Room-temperature transfer characteristics, i.e., source-to-drain current, I_{DS} versus V_{GS}, in logarithmic scale, for a representative SET with L = 1 μm and W = 1.5 μm measured using source-to-drain voltage, V_{DS} = 100 mV. Since the starting material is metallic, the device is in the ON-state at V_{GS} = 0 V with an ON-state current of ∼0.2 mA/μm. When V_{GS} is increased, the electric field across the PZT leads to an in-plane strain at the Ni/$MoTe_2$ contact interface. Once V_{GS} reaches V_S, the Ni contact to the $MoTe_2$ channel cracks or delaminates and loses electrical contact, which turns off the device with OFF-state current values of ∼1 pA/μm (red curve). Note that the OFF-state current is determined by the noise floor of the instrument. When V_{GS} is swept back the reverse process is triggered at a lower V_S, resulting in a clockwise hysteresis in the transfer characteristics of the SET (blue curve). (b) Zoomed-in region where the device is turning off during the forward sweep. Note that a V_{GS} step size of 4 mV was used for this measurement. The SS was found to be 1.6 mV/decade and 6 mV/decade when averaged over 3 and 6 orders of magnitude change, respectively, in I_{DS}. (c) Transfer characteristics in the linear scale with forward (red) and backward (blue) sweeps. (d) Extracted transconductance, g_m, versus V_{GS}.

magnitude better than state-of-the-art silicon FinFETs.[37,38] Unlike a conventional FET, the gate terminal of the SET does not induce a conducting channel between the source and the drain terminal. Therefore, this phenomenon is better characterized as a "strain effect" rather than a field effect. Hence this device is called a SET. Also note that unlike MOSFETs, where the interface between the dielectric and the channel significantly influences the SS, the absence of the field effect eliminates such impact on the SS in the SET.

Figure 3c shows the transfer characteristics in the linear scale and Figure 3d shows the extracted transconductance, g_m, versus V_{GS} for the SET shown in Figure 3a, b. Peak g_m was found to be > 100 μS/μm for V_{DS} = 100 mV. Note that high g_m leads to high gain when a switch is used as an amplifier. In conventional MOSFETs, the mobility of the channel material determines g_m. For example, a record high g_m = 3.45 mS/μm has been reported for high mobility InGaAs quantum-well MOSFET at V_{DS} = 0.5 V.[39] Similarly, g_m = 282 μS/μm at V_{DS} = 2 V has been reported for high mobility black phosphorus FETs.[40] Given that g_m scales linearly with V_{DS}, it is remarkable to find such a high g_m in our SET device, which is comparable to record high values reported in the literature.

Figure 4a, b shows the output characteristics of the representative SET, i.e., I_{DS} versus V_{DS} for different V_{GS} in the linear and logarithmic scales, respectively. The color gradient runs blue to red for ascending values of V_{GS}. The initial state of the channel, which is semimetallic and behaves as a resistor, is evident from the linearI_{DS} versus V_{DS} characteristics. However, for V_{GS} > 10 V, the slope of the line in Figure 4a reduces, marking the beginning of the delamination/cracking process which manifests itself as an increase in the resistance. In Figure 4b, for V_{GS} = 18 V, there is an abrupt drop in the I_{DS}, which is when the 1T′-$MoTe_2$ flake abruptly loses electrical contact with Ni. For all subsequent (higher) values of V_{GS}, the device stays in the OFF state with current levels of ∼1 pA/μm. Our device exhibits ON currents of ∼1.8 mA/μm at V_{DS} = 1 V, which is ∼2× higher than even the most aggressively scaled Si nano CMOS devices.[41] This translates to an ON/OFF current ratio of 3 × 10^9. Owing to the high ON current, the SET can be operated with ultra-low V_{DS} values as shown in Figure 4c. Thus, our SET achieves impressive performance in the four basic parameters that define an ideal transistor, i.e., high ON current, low OFF current, steep slope switching, and high transconductance.

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

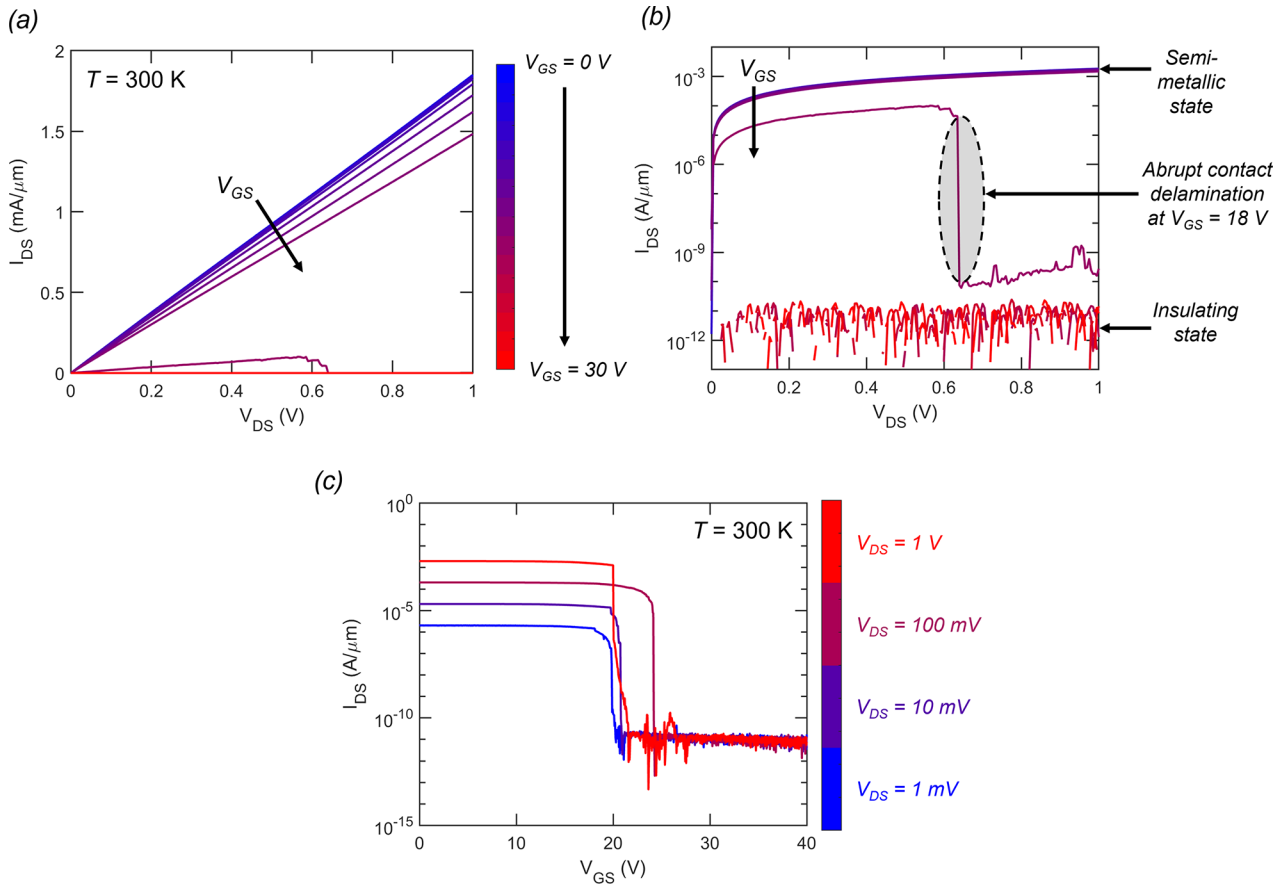


Figure 4. Experimental demonstration of high-performance in SET. Output characteristics of a representative SET, i.e., I_{DS} versus V_{DS} for different V_{GS} in (a) linear and (b) logarithmic scales. The color gradient runs blue to red for ascending values of V_{GS}. The starting material, which is semimetallic, behaves as a resistor, as evident from the linear I_{DS} versus V_{DS} characteristics. However, for V_{GS} > 10 V, the slope of the line in panel a is reduced, marking the beginning of the delamination process, which manifests itself as an increase in the resistance. At V_{GS} = 18 V, there is an abrupt drop in I_{DS} in panel b, which is when the 1T′-$MoTe_2$ flake abruptly loses electrical contact with Ni owing to cracking/delamination. For all subsequent (higher) values of V_{GS}, the device stays in the OFF-state with current levels of ∼1 pA/μm. Our device exhibits ON-state currents of ∼1.8 mA/μm at V_{DS} = 1 V. (c) Ultra-low voltage operation of SET.

Note that a training or forming process is needed before the SET can demonstrate steep switching. This process involves poling the PZT by applying a high electric field across it. We found that applying V_G = −60 V for 10 s produced good results for some devices. After this, the $MoTe_2$ channel was subjected to repeated transfer sweeps with V_{GS} = 0 to 70 V and V_{DS} = 100 mV. The evolution of the transfer characteristics during this training process is captured in Figure 5a. This process was repeated until the abrupt switching from the ON to the OFF-state is observed within the gate voltage range as shown in Figure 5b. This observation can be explained by the fact that the successive transfer sweeps stress the contact interface repeatedly until structural fatigue leads to the manifestation of the effects of delamination/cracking at the contact edge. This is also why the as-fabricated devices do not show any abrupt switching behavior. We believe that the crack formation mechanism is phenomenologically similar to the one described in the literature.[29] Most of the formed SETs show abrupt switching for positive V_{GS}. However, as shown in Figure S2, few devices show the abrupt switching for negative gate voltages with an anticlockwise hysteresis between the sweeps in both directions. Once formed, SETs demonstrate robust switching behavior. Figure 5c shows the switching endurance of the SET for 1 × 10^6 cycles. During each cycle, V_{GS} was switched between 0 V and V_S and I_{DS} was read using V_{DS} = 100 mV. The cycling frequency was 100 kHz. In the ON-state, I_{DS} = ∼220 μA while the OFF-state current is determined by the noise floor of our measurement setup. The switching delay for the SET was found to be < 5 μs as shown in Figure 5d. Note that the measurement of switching delay for the SET device was limited by the capability of our electrical instrument, which can sample low-current (∼pA) only once every 5 μs. Nevertheless, formed SET devices appear promising to achieve high endurance and speed.

Note that Hou et al.[42] have shown similar results for 1T′-$MoTe_2$ anchored to lead magnesium niobate-lead titanate (PMN−PT) films using Ni contacts, but may have misinterpreted the results. They claim that in-plane strain at the interface of 1T′-$MoTe_2$ and Ni leads to a reversible phase transition in 1T′-$MoTe_2$ from a semimetallic to a semiconducting phase, which results in subnanosecond nonvolatile strain switching at the attojoule/bit level with a conductance on/off ratio of approximately 7 orders of magnitude. However, based on our study and the previous report,[29] it appears that contact delamination/cracking is the primary cause behind the abrupt switching in the SET device. In fact, this switching phenomenon is not unique to 1T′-$MoTe_2$. Figure S3 shows that near identical abrupt switching behavior is observed in an otherwise identical device where the channel material is formed by ultra-thin WSe_2, a semiconducting 2D material,

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

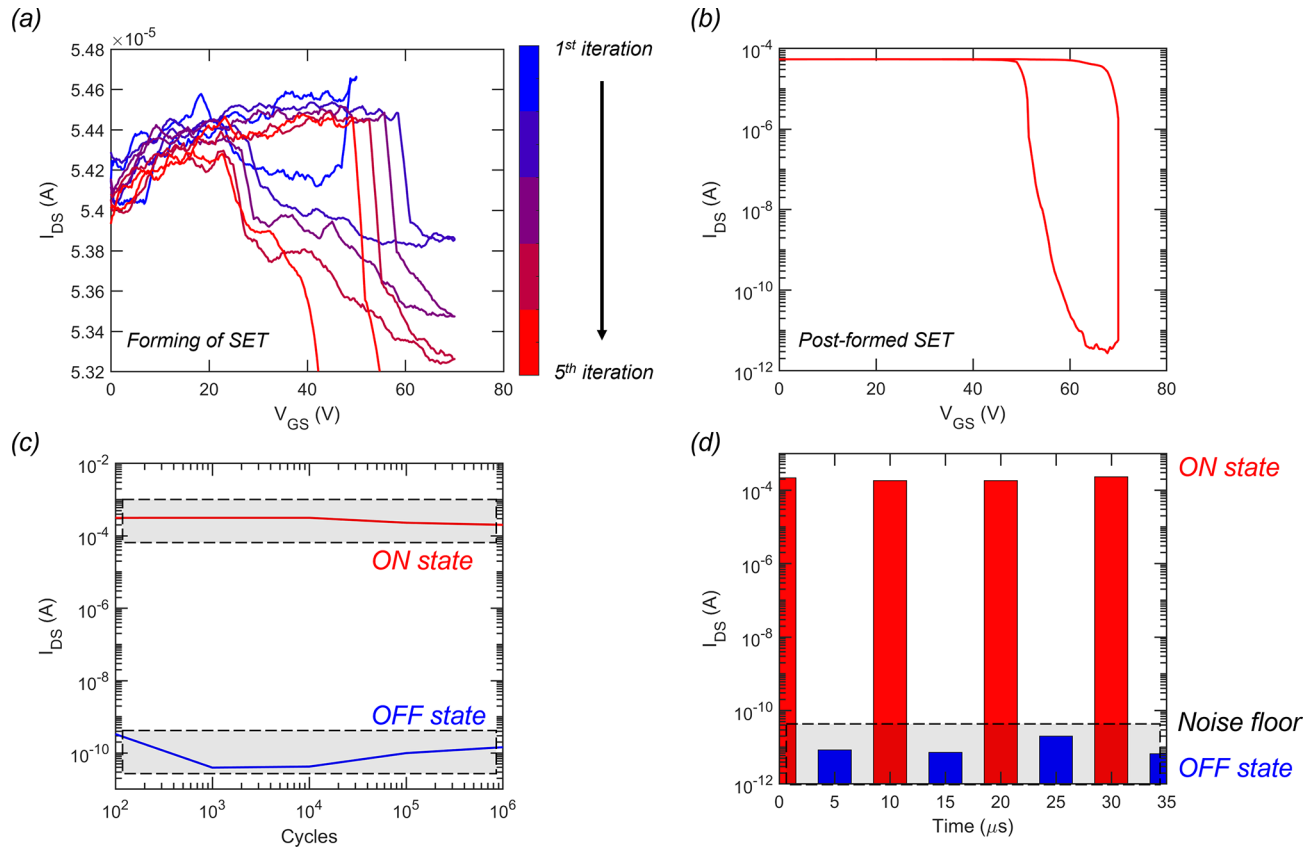


Figure 5. Forming process, endurance, and speed for SET. (a) Training or formation process for SET. (b) Transfer characteristics, (c) switching endurance, and (d) switching delay for post-trained or postformed SET.

instead of semimetallic 1T′-$MoTe_2$. As shown in Figure S3a, a similar forming process is followed where the device is subjected to high electric fields repeatedly by cycling the V_{GS} from −50 to 50 V for 30 times. Initially, the device shows ambipolar transport behavior as has been shown for WSe_2 in the literature.[43] However, on the 28th sweep, there is an abrupt drop in the I_{DS} values close to V_{GS} = 50 V. This abrupt drop becomes more pronounced as more sweeps are performed and the V_S shows a decreasing trend. Once, the forming process is complete, cycling V_{GS} within 0 to 50 V is enough to trigger the abrupt drop in I_{DS}, as shown in Figure S3b. These results further confirm that the steep switching must be attributed to the strain induced cracking/delamination of Ni at the metal/2D contact interface rather than the strain induced phase transition as claimed previously.[42] It is also possible that the cracking of the contact metal occurs elsewhere, in a region further away from the interface between the metal and the 2D material. While this contact delamination effect is not unique to 1T′-$MoTe_2$, the benefit of using this 2D material over others is that this phase of $MoTe_2$ exists in a stable semimetallic phase at room temperature. This leads to a high ON current and a high transconductance.

While the working principle of the SET may appear similar to that of the NEMS in some respects, there is an important distinction. Most NEMS demonstrations in the literature rely on the electrostatic attraction of a suspended channel using the gate electrode to switch between the ON and the OFF states.[44−46] Since the channel material must physically move across an air gap in response to an electrostatic force during the switching process, the mass of the suspended part of the channel is a limiting factor in the switching speed. However, the SET utilizes strain-induced contact delamination in an abrupt yet reversible manner in a simple structure which is very similar to existing MOSFETs. Moreover, the fabrication process for NEMS devices tends to be more complex since the channel and the gate need to be at different heights with an air gap between them, which is not the case for the SET. It is challenging to observe the interface between the $MoTe_2$ channel and the Ni contact directly where the delamination is supposed to occur, as it would require an in situ material characterization experiment. Our current hypothesis is that Ni is more likely to form a van der Waal (vdW) gapped contact with the $MoTe_2$ channel. Based on previously reported work, the adhesion between the $MoTe_2$ and the PZT substrate will be enhanced by repeated cycling of the electric field.[47] On the application of the electric field, the PZT displaces along with the $MoTe_2$ which is strongly adhered to it. As a result, the vdW gapped contact between $MoTe_2$ and Ni enlarges in spacing leading to a break in the electrical contact at the switching voltage V_S. Note that edge injection from the Ni to the $MoTe_2$ can be disregarded as the area of the edge contact is insignificant compared to the planar contact. Further investigation of the strain transduction, the contact delamination mechanisms, and the development of a theoretical framework will aid the understanding and advancement of the SET.

In conclusion, we have demonstrated a radically different switch by exploiting strain-induced contact modification to ultra-thin 1T′-$MoTe_2$. We have achieved SS < 0.68 mV/decade at room temperature for 7 orders of magnitude change

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259

in the source-to-drain current, and a high ON current of ∼1.8 mA/μm, in addition to a low OFF current, a high ON/OFF current ratio, and a high transconductance. The SET uses in-plane strain from a piezoelectric layer to induce an abrupt and controlled delamination/cracking of the contact to the 1T′-$MoTe_2$ channel. The PZT layer used for this device can be scaled down in thickness to achieve lower operating voltages. Likewise, the device dimensions can be scaled and yet strain induced cracking should occur in the metal contacts. The contact delamination mechanics that result in the switching action of the SET continue to work when $MoTe_2$ is replaced by WSe_2 as the channel. Therefore, this device should also exhibit steep slope switching with a graphene channel, which will be the focus of our future work. There are still some challenges such as device-to-device variations, which can be mitigated through large area growth of 1T′-$MoTe_2$. Nevertheless, our preliminary results are promising enough to warrant further investigation by a wider community on the SET, given that the SET has the potential to resolve some of the most difficult and fundamental challenges faced the semiconductor industry today.

■ ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at https://pubs.acs.org/doi/10.1021/acs.nanolett.2c02194.

Fabrication methods, electrical characterization of champion SET, abrupt switching for negative V_{GS}, and observation of the contact delamination phenomenon in WSe_2 SETs (PDF)

■ AUTHOR INFORMATION

Corresponding Author

Saptarshi Das − *Electrical Engineering, Engineering Science and Mechanics, Material Research Institute, and Materials Science and Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States;* orcid.org/0000-0002-0188-945X; Email: sud70@psu.edu

Author

Sarbashis Das − *Electrical Engineering, Pennsylvania State University, University Park, Pennsylvania 16802, United States;* orcid.org/0000-0003-4553-5693

Complete contact information is available at: https://pubs.acs.org/10.1021/acs.nanolett.2c02194

Notes

The authors declare no competing financial interest.

■ ACKNOWLEDGMENTS

The work was supported by the Army Research Office (ARO) through Contract Number W911NF1920338 and the National Science Foundation (NSF) through a CAREER Award under grant no. ECCS-2042154.

■ REFERENCES

(1) Thompson, S. E.; Parthasarathy, S. Moore's law: the future of Si microelectronics. *Mater. Today* **2006**, *9* (6), 20−25.

(2) Sze, S. M.; Sze, S. *Modern Semiconductor Device Physics*; Wiley, 1998.

(3) Myers, G. J. *Advances in Computer Architecture*; John Wiley & Sons, Inc., 1982.

(4) Ma, X.; Arce, G. R. *Computational Lithography*; John Wiley & Sons, 2011.

(5) Borkar, S. Design challenges of technology scaling. *IEEE micro* **1999**, *19* (4), 23−29.

(6) Lotfi-Kamran, P.; Sarbazi-Azad, H. Dark Silicon and the History of Computing. In *Advances in Computers*; Hurson, A. R., Sarbazi-Azad, H., Eds.: Elsevier, 2018; Vol. *110*, Chapter 1, pp 1−33.

(7) Meindl, J. D.; Chen, Q.; Davis, J. A. Limits on silicon nanoelectronics for terascale integration. *Science* **2001**, *293* (5537), 2044−2049.

(8) Ionescu, A. M.; Riel, H. Tunnel field-effect transistors as energy-efficient electronic switches. *Nature* **2011**, *479* (7373), 329−37.

(9) Appenzeller, J.; Lin, Y. M.; Knoch, J.; Avouris, P. Band-to-Band Tunneling in Carbon Nanotube Field-Effect Transistors. *Phys. Rev. Lett.* **2004**, *93* (19), 196805.

(10) Choi, W. Y.; Park, B.-G.; Lee, J. D.; Liu, T.-J. K. Tunneling field-effect transistors (TFETs) with subthreshold swing (SS) less than 60 mV/dec. *IEEE Electron Device Lett.* **2007**, *28* (8), 743−745.

(11) Borg, B. M.; Dick, K. A.; Ganjipour, B.; Pistol, M.-E.; Wernersson, L.-E.; Thelander, C. InAs/GaSb heterostructure nanowires for tunnel field-effect transistors. *Nano Lett.* **2010**, *10* (10), 4080−4085.

(12) Ganjipour, B.; Wallentin, J.; Borgstrom, M. T.; Samuelson, L.; Thelander, C. Tunnel field-effect transistors based on InP-GaAs heterostructure nanowires. *ACS Nano* **2012**, *6* (4), 3109−3113.

(13) Sarkar, D.; et al. A subthermionic tunnel field-effect transistor with an atomically thin channel. *Nature* **2015**, *526* (7571), 91−95.

(14) Wu, P.; et al. Complementary Black Phosphorus Tunneling Field-Effect Transistors. *ACS Nano* **2019**, *13* (1), 377−385.

(15) Wu, P.; Appenzeller, J. Reconfigurable Black Phosphorus Vertical Tunneling Field-Effect Transistor With Record High ON-Currents. *IEEE Electron Device Lett.* **2019**, *40* (6), 981−984.

(16) Cristoloveanu, S.; Wan, J.; Zaslavsky, A. A review of sharp-switching devices for ultra-low power applications. *IEEE Journal of the Electron Devices Society* **2016**, *4* (5), 215−226.

(17) Salahuddin, S.; Datta, S. Use of Negative Capacitance to Provide Voltage Amplification for Low Power Nanoscale Devices. *Nano Lett.* **2008**, *8* (2), 405−410.

(18) Ko, E.; Lee, J. W.; Shin, C. Negative Capacitance FinFET With Sub-20-mV/decade Subthreshold Slope and Minimal Hysteresis of 0.48 V. *IEEE Electron Device Lett.* **2017**, *38* (4), 418−421.

(19) Lee, M. H.; et al. Physical thickness 1.x nm ferroelectric HfZrOx negative capacitance FETs. *2016 IEEE International Electron Devices Meeting (IEDM)* **2016**, *3*−*7*, 12.1.1−12.1.4.

(20) Cheema, S. S.; et al. Enhanced ferroelectricity in ultrathin films grown directly on silicon. *Nature* **2020**, *580* (7804), 478−482.

(21) Si, M.; et al. Sub-60 mV/dec ferroelectric HZO MoS_2 negative capacitance field-effect transistor with internal metal gate: The role of parasitic capacitance. *2017 IEEE International Electron Devices Meeting (IEDM)* **2017**, *2*−*6*, 23.5.1−23.5.4.

(22) Cao, W.; Banerjee, K. Is negative capacitance FET a steep-slope logic switch? *Nat. Commun.* **2020**, *11* (1), 196.

(23) Alam, M. A.; Si, M.; Ye, P. D. ″A critical review of recent progress on negative capacitance field-effect transistors. *Appl. Phys. Lett.* **2019**, *114* (9), 090401.

(24) Shukla, K. D.; Saxena, N.; Durai, S.; Manivannan, A. Redefining the Speed Limit of Phase Change Memory Revealed by Time-resolved Steep Threshold-Switching Dynamics of AgInSbTe Devices. *Sci. Rep.* **2016**, *6* (1), 37868.

(25) Shukla, N.; et al. Ag/HfO_2 based threshold switch with extreme non-linearity for unipolar cross-point memory and steep-slope phase-FETs. *2016 IEEE International Electron Devices Meeting (IEDM)* **2016**, *3*−*7*, 34.6.1−34.6.4.

(26) Vitale, W. A.; et al. A Steep-Slope Transistor Combining Phase-Change and Band-to-Band-Tunneling to Achieve a sub-Unity Body Factor. *Sci. Rep.* **2017**, *7* (1), 355.

(27) Riverola, M.; Uranga, A.; Torres, F.; Barniol, N. Fabrication and characterization of a hammer-shaped CMOS/BEOL-embedded nanoelectromechanical (NEM) relay. *Microelectron. Eng.* **2018**, *192*, 44−51.
(28) International Roadmap for Devices and Systems (IRDS). IEEE. https://irds.ieee.org/editions/2020.
(29) Liu, Z. Q.; Liu, J. H.; Biegalski, M. D.; Hu, J.-M.; Shang, S. L.; Ji, Y.; Wang, J. M.; Hsu, S. L.; Wong, A. T.; Cordill, M. J.; et al. Electrically reversible cracks in an intermetallic film controlled by an electric field. *Nat. Commun.* **2018**, *9*, 41.
(30) Schulman, D. S. *Contact, Interface, And Strain Engineering of Two-Dimensional Transition Metal Dichalcogenide Field Effect Transistors*; The Pennsylvania State University: State College, PA, 2019.
(31) Zhang, X.; et al. Low contact barrier in 2H/1T′ $MoTe_2$ in-plane heterostructure synthesized by chemical vapor deposition. *ACS Appl. Mater. Interfaces* **2019**, *11* (13), 12777−12785.
(32) Lotgering, F. K. Topotactical reactions with ferrimagnetic oxides having hexagonal crystal structures—I. *Journal of Inorganic and Nuclear Chemistry* **1959**, *9* (2), 113−123.
(33) Kazi, I. H.; Wild, P.; Moore, T.; Sayer, M. Characterization of sputtered nichrome (Ni−Cr 80/20 wt.%) films for strain gauge applications. *Thin Solid Films* **2006**, *515* (4), 2602−2606.
(34) Gandhi, R.; Chen, Z.; Singh, N.; Banerjee, K.; Lee, S. Vertical Si-Nanowire n-Type Tunneling FETs With Low Subthreshold Swing (≤50 mV/decade) at Room Temperature. *IEEE Electron Device Lett.* **2011**, *32* (4), 437−439.
(35) Krishnamohan, T.; Kim, D.; Raghunathan, S.; Saraswat, K. Double-Gate Strained-Ge Heterostructure Tunneling FET (TFET) With record high drive currents and ≪60mV/dec subthreshold slope. *2008 IEEE International Electron Devices Meeting* **2008**, *15−17*, 1−3.
(36) Then, H. W.; et al. Experimental observation and physics of "negative" capacitance and steeper than 40mV/decade subthreshold swing in $Al_{0.83}In_{0.17}$ N/AlN/GaN MOS-HEMT on SiC substrate. *2013 IEEE International Electron Devices Meeting* **2013**, *9−11*, 28.3.1−28.3.4.
(37) Subramanian, V.; et al. Planar Bulk MOSFET Versus FinFETs: An Analog/RF Perspective. *IEEE Trans. Electron Devices* **2006**, *53* (12), 3071−3079.
(38) Hu, C. 3D FinFET and other sub-22nm transistors. *2012 19th IEEE International Symposium on the Physical and Failure Analysis of Integrated Circuits* **2012**, *2−6*, 1−5.
(39) Lin, J.; Cai, X.; Wu, Y.; Antoniadis, D. A.; del Alamo, J. A. Record Maximum Transconductance of 3.45 mS/μm for III-V FETs. *IEEE Electron Device Lett.* **2016**, *37* (4), 381−384.
(40) Haratipour, N.; Koester, S. J. Ambipolar black phosphorus MOSFETs with record n-channel transconductance. *IEEE Electron Device Lett.* **2016**, *37* (1), 103−106.
(41) Chang, L.; Choi, Y.-K.; Ha, D.; Ranade, P.; Xiong, S.; Bokor, J.; Hu, C.; King, T.-J.; et al. Extremely scaled silicon nano-CMOS devices. *Proc. IEEE* **2003**, *9* (11), 1860−1873.
(42) Hou, W.; et al. Strain-based room-temperature non-volatile $MoTe_2$ ferroelectric phase change transistor. *Nature Nanotechnol.* **2019**, *14* (7), 668−673.
(43) Das, S.; Appenzeller, J. WSe_2 field effect transistors with enhanced ambipolar characteristics. *Applied Physics Letters* **2013**, *103* (10), 103501.
(44) Kim, J.-H.; Chen, Z. C. Y.; Kwon, S.; Xiang, J. Three-Terminal Nanoelectromechanical Field Effect Transistor with Abrupt Subthreshold Slope. *Nano Lett.* **2014**, *14* (3), 1687−1691.
(45) Huynh Van, N.; Muruganathan, M.; Kulothungan, J.; Mizuta, H. Fabrication of a three-terminal graphene nanoelectromechanical switch using two-dimensional materials. *Nanoscale* **2018**, *10* (26), 12349−12355.
(46) Feng, X.; Matheny, M.; Zorman, C. A.; Mehregany, M.; Roukes, M. Low voltage nanoelectromechanical switches based on silicon carbide nanowires. *Nano Lett.* **2010**, *10* (8), 2891−2896.
(47) Du, H.; Xue, T.; Xu, C.; Kang, Y.; Dou, W. Improvement of mechanical properties of graphene/substrate interface via regulation of initial strain through cyclic loading. *Optics and Lasers in Engineering* **2018**, *110*, 356−363.

https://doi.org/10.1021/acs.nanolett.2c02194
Nano Lett. 2022, 22, 9252−9259