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Digital Keying Enabled by Reconfigurable 2D Modulators

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Energy, area, and bandwidth efficient communication primitives are essential to sustain the rapid increase in connectivity among internet-of-things (IoT) edge devices. While IoT edge-sensing, edge-computing, and edge-storage have witnessed innovation in materials and devices, IoT edge communication is yet to experience such transformation. The aging silicon (Si)-based complementary metal–oxide–semiconductor (CMOS) technology continues to remain the mainstay of communication devices where they are used to implement amplitude, frequency, and phase shift keying (amplitude-shift keying [ASK]/frequency-shift keying [FSK]/phase-shift keying [PSK]). Keying allows digital information to be communicated over a radio channel. While CMOS-based keying devices have evolved over the years, their hardware footprint and energy consumption are major concerns for resource constrained IoT communication. Furthermore, separate circuit designs and hardware elements are needed for each keying scheme and achieving multibit modulation to improve bandwidth efficiency remains a challenge. Here, a reconfigurable modulator is introduced that exploits unique ambipolar transport and programmable Dirac voltage in ultrathin $MoTe_2$ field-effect transistors to achieve ASK, FSK, and PSK modulation. Furthermore, by integrating two programmed $MoTe_2$ field-effect transistors, multibit data modulation is demonstrated, which improves the bandwidth efficiency by 200%. Finally, a frequency quadrupler is also realized exploiting the unique "double-well" transfer characteristic.

1. Introduction

Digital modulation or keying is the cornerstone of modern communication and plays an indispensable role in wired and wireless data transmission between consumer devices, appliances, and back-end infrastructure in today's world. Various types of keying exist including the most basic amplitude-shift keying (ASK), frequency-shift keying (FSK), and phase-shift keying (PSK).[1] Each keying scheme requires a specific modulator circuit and silicon-based complementary metal–oxide–semiconductor (CMOS) technology is most commonly used to design such modulators. For example, the well-known 555 timer circuit is used to implement binary ASK and FSK although other modulator designs exist. Over the years CMOS circuits used in ASK,[2–5] FSK,[6,7] and PSK[8] have evolved to become more efficient and adaptable to a wide variety of applications ranging from wearable electronics to space electronics. However, achieving multibit keying to improve bandwidth efficiency remains a hardware challenge. One approach is to combine two or more keying schemes, for example, amplitude and phase shift keying (APSK), where both the amplitude and the phase of the radio wave is modulated. However, it comes at the cost of increased complexity and energy expenditure for the modulator circuit.[9] Therefore, in the current era of internet of things (IoT) where the number of interconnected edge devices is rapidly increasing, the need for innovation in low-power and compact modulators that offer high bandwidth efficiency is urgent and immediate.

In recent years, there has been an increased focus on utilizing novel materials and device properties to implement complex functionalities in hardware. Examples include acceleration of image processing algorithms exploiting the vector matrix multiplication capability of memristor-based crossbar arrays,[10,11] probabilistic neural networks using Gaussian synapses enabled by heterointegration of 2D semiconductors,[12] collision avoidance using in-sensor compute functionality of photosensitive monolayer 2D field-effect transistors (FETs),[13] and biomimetic audiomorphic computation using novel split-gate transistor designs.[14] However, the field of digital communication has, so far, not witnessed this kind of an effort leaving a large scope for innovations to improve the area, energy, and bandwidth efficiency of digital modulators.

In this work, we demonstrate a low-power, reconfigurable, and compact modulator based on molybdenum ditelluride ($MoTe_2$) field-effect transistor (FET). $MoTe_2$ is a 2D transition metal dichalcogenide (TMD) material. TMDs have the general formula MX_2 where M is the metal atom (M = Mo, W) and

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X is the chalcogen atom (X = S, Se, Te). $MoTe_2$ is semiconducting in the 2H phase and has a direct bandgap of 1.1 eV when thinned down to a monolayer.[15] When used as the channel in a FET, $MoTe_2$ shows ambipolar transport characteristics which can be tuned by charge-transfer,[16] laser,[17,18] or UV irradiation.[19] $MoTe_2$ has been used as an ambipolar FET for inverter and amplifier circuits,[20–22] as a PN diode for on-chip optoelectronics,[23] and as a photodetector for silicon photonic integrated circuits.[24,25] Consistent with previously published work, our $MoTe_2$ FETs demonstrate ambipolar transport, i.e., the presence of both electron and hole conduction and also utilize a gate stack, which allows analog and nonvolatile programming of the Dirac voltage. Exploiting these unique properties, we have been able to achieve ASK, FSK, and PSK modulation schemes using a single $MoTe_2$ FET greatly reducing the energy and area overhead compared to state-of-the-art implementations using silicon CMOS-based circuits. Additionally, using a pair of programmed $MoTe_2$ FETs with different Dirac voltages, we have been able to demonstrate up to 3-bit ($M = 8$) modulation using a combination of ASK, FSK, and PSK schemes to enhance the bandwidth efficiency. Furthermore, our modulator can also be used as a frequency quadrupler. Our demonstration of multipurpose $MoTe_2$-based modulators highlight the importance of material and device level innovations as the driver for energy-, area-, and bandwidth-efficient IoT edge communication.

2. Digital Keying using Ambipolar Characteristics

Figure 1 explains the operation of ambipolar $MoTe_2$ FETs. As shown in Figure 1a, the channel is formed by a flake of multilayer molybdenum ditelluride ($MoTe_2$) which is a 2D transition metal dichalcogenide (TMDC). The gate dielectric is 50 nm of Al_2O_3. The back-gate stack of this modulator utilizes Pt/TiN/p^{++} Si layers which allow reconfigurability via nonvolatile programmability of the threshold voltage, as will be explained later. The degenerately doped (p^{++}) silicon forms the back-gate contact. The source and drain contacts are formed by a Ni (40 nm)/Au (30 nm) metal stack. Details about the fabrication and characterization processes of these devices can be found in the Experimental Section. Figure 1b shows the scanning electron microscopy (SEM) image of the as-fabricated device, taken from a top-down view, where the outline of the $MoTe_2$ flake is clearly visible underneath the source/drain contacts. Atomic force microscopy (AFM) scan of the $MoTe_2$ flake revealed the thickness to be ≈10 nm (around 15 monolayers). Figure 1c shows the Raman spectroscopy performed on the $MoTe_2$ flake.

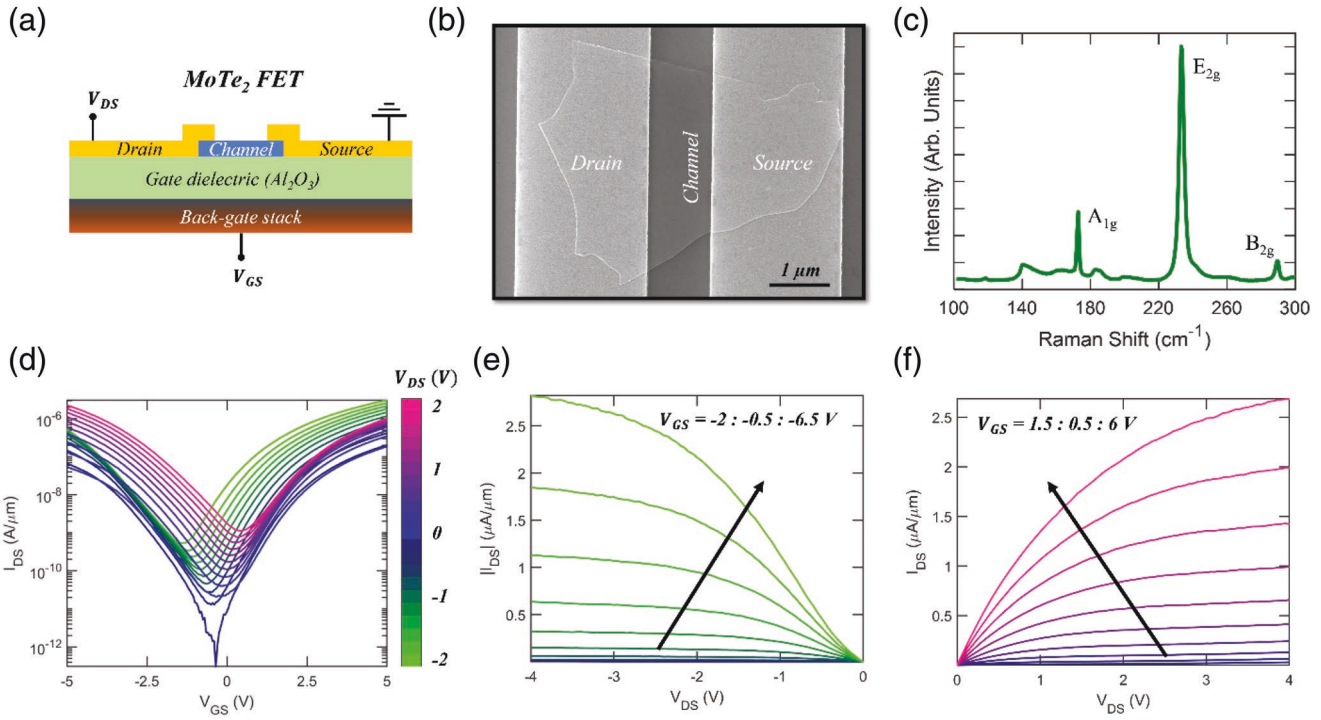


Figure 1. Ambipolar transport in $MoTe_2$ field-effect transistor (FET). a) Schematic of a 2D FET with ≈10 nm (multilayer) molybdenum ditelluride ($MoTe_2$) as the semiconducting channel, Ni as the source/drain contacts, and 50 nm Al_2O_3 as the gate dielectric layer. The back-gate electrode comprises Pt/TiN/p^{++}-Si layers. The back-gate stack also offers analog and nonvolatile programming capability for the $MoTe_2$ FET. b) Top-down scanning electron microscopy (SEM) image of the $MoTe_2$ FET with c) Raman spectroscopy performed on the $MoTe_2$ flake. The prominent peak of the E_{2g} mode is found to be at 233 cm^{-1} while the weaker A_{1g} mode has a peak at 172 cm^{-1} and the B_{2g} peak is at 289 cm^{-1}, confirming that the flake is multilayer and in the semiconducting 2H phase. d) Transfer characteristics, i.e., the source-to-drain current (I_{DS}) versus source-to-gate voltage (V_{GS}) for different source-to-drain voltage (V_{DS}) for the $MoTe_2$ FET measured under vacuum (≈10^{-6} Torr). $MoTe_2$ FET shows ambipolar transport, i.e., the presence of distinct electron and hole branches. The inflection point where I_{DS} is minimum is referred to the Dirac point and the corresponding values of gate voltage and drain current are denoted by V_{Dirac} and I_{Dirac} respectively. e,f) Output characteristics of the $MoTe_2$ FET for positive (e) and negative (f) values of V_{GS} and V_{DS}. The n-branch current goes up to 2.6 μA μm^{-1} for $V_{DS} = 4$ V and $V_{GS} = 6$ V, while the p-branch current goes up to 2.7 μA μm^{-1} for $V_{DS} = -4$ V and $V_{GS} = -6.5$ V.

The prominent peak of the E_{2g} mode is found to be at 233 cm^{-1} while the weaker A_{1g} mode has a peak at 172 cm^{-1} and the B_{2g} peak is at 289 cm^{-1}, confirming that the flake is multilayer and in the semiconducting 2H phase.[26]

Figure 1d shows the transfer characteristics, i.e., the source-to-drain current (I_{DS}) versus source-to-gate voltage (V_{GS}) for different source-to-drain voltage (V_{DS}) of a representative $MoTe_2$ FET in the logarithmic scale at room temperature measured under vacuum (≈10^{-6} Torr). The V_{GS} runs from −5 to 5 V while the V_{DS} is from −2 to 2 V. The $MoTe_2$ FET shows ambipolar transfer characteristics as indicated by the I_{DS} which has distinct electron and hole branches for positive and negative values of V_{GS} respectively. The inflection point, where I_{DS} is minimum is referred to as the Dirac voltage (V_{Dirac}) and the minimum current is referred to as Dirac current, I_{Dirac}. The position of V_{Dirac} and the magnitude of I_{Dirac} depends on the relative position of the conduction and valence band of $MoTe_2$ and the Fermi level of the metal contact. Given that both electron and hole conductions are observed in $MoTe_2$, it can be ascertained that the Fermi level of our Ni contact is aligned to the middle of the bandgap of $MoTe_2$, which is consistent with other reports from the literature.[27] Applying positive and negative values of V_{GS} will lead to injection of carriers into the conduction and the valence bands respectively, as shown using the energy band diagrams in Figure S1 (Supporting Information). Figure 1e,f shows the output characteristics, i.e., I_{DS} vs V_{DS} for positive and negative V_{GS} values, respectively. In Figure 1e, for V_{DS} = 4 V, and V_{GS} = 6 V, the n-branch current reaches up to 2.6 μA μm^{-1}. Similarly, in Figure 1f, for V_{DS} = −4 V and V_{GS} = −6.5 V, the p-branch current reaches up to 2.7 μA μm^{-1}. Current saturation is observed for both the n- and the p-branch.

Figure 2 demonstrates the working of the $MoTe_2$ FET as a reconfigurable modulator to implement ASK, FSK, and PSK. For all three types of modulation, the analog carrier is a sinusoidal wave, while the data to be transmitted is digital. Figure S2 (Supporting Information) shows how ASK, FSK, and PSK modulated waveforms can be generated by mixing the analog carrier and the digital data. Figure 2a shows the circuit diagram for the implementation of ASK, FSK, and PSK using the ambipolar $MoTe_2$ FET. The input signal (v_{GS}), which is the superposition of the carrier wave, $c(t)$, digital data, $d(t)$, and the constant bias, V_{key}, is applied to the gate terminal of the $MoTe_2$ FET, whereas the drain current gives the modulated output waveform as i_{DS}. As we will discuss below, V_{key}, allows switching between various modulation schemes exploiting the unique ambipolar transfer characteristics of the $MoTe_2$ FET. Also note that, we have used a sinusoidal signal of amplitude 400 mV and frequency 10 kHz as $c(t)$, whereas for $d(t)$, logic levels "0" and "1" are represented by 0 V and V_{DD} = 2 V, respectively.

For ASK, we use V_{key} = 3.45 V, which shifts the logic levels "0" and "1" to V_{GS} = 3.45 V and 5.45 V, respectively, as shown in Figure 2b. Note that the slopes of the transfer characteristics or the transconductance (g_m) values of the $MoTe_2$ FET are different at these two operating V_{GS}. For example, g_m = 3.53 μS at V_{GS} = 5.45 V and g_m = 118 nS at V_{GS} = 3.45 V. This leads to different amplitude of $i_{DS}(t)$ for the same $c(t)$ but different $d(t)$ corresponding to the logic levels "1" and "0", which represents the ASK modulation as shown in Figure 2c,d, respectively. Note that, we chose V_{key} such that the device operates in the n-branch of the transfer characteristics, where an increase in V_{GS} leads to an increase in the I_{DS} and vice versa making sure that g_m is positive and $i_{DS}(t)$ is in-phase with $c(t)$. Figure 2e shows the power spectral density (PSD) of $c(t)$ and $i_{DS}(t)$ corresponding to both logic levels obtained by taking the fast Fourier transform (FFT) of Figure 2c,d. Note that the frequency of $i_{DS}(t)$ remains the same as $c(t)$. Furthermore, the amplitude of higher harmonics is insignificant indicating near linear device operation. Figure S3a,b (Supporting Information), respectively, show an example of a binary input bitstream fed into the $MoTe_2$ FET-based modulator and the corresponding output signal that follows ASK modulation.

For FSK, we use V_{key} = 2.45 V, which shifts the logic levels "0" and "1" to V_{GS} = 2.45 and 4.45 V, respectively, as shown in Figure 2f. At V_{GS} = 4.45 V, the device operates in the n-branch of the transfer characteristics like in the previous case ensuring that the frequency of $i_{DS}(t)$ is same as $c(t)$ as shown in Figure 2g. However, at V_{GS} = 2.45 V, i.e., at the Dirac point, I_{DS} is at its minimum value. At this operating point, both increase as well as decrease in V_{GS} lead to an increase in the I_{DS}. As such the frequency of i_{DS} becomes double that of $c(t)$, akin to a full-wave rectification process as shown in Figure 2h. Figure 2i shows the PSD of $c(t)$ and $i_{DS}(t)$ corresponding to both logic levels by taking the FFT of Figure 2g,h. Clearly, logic level "1" and "0" are represented by two different frequencies validating the FSK modulation for V_{key} = 2.45 V. Note that due to the difference in g_m values for V_{GS} = 4.45 and 2.45 V, there will be an inadvertent ASK. Figure S4a,b (Supporting Information), respectively, show an example of a binary input bitstream fed into the $MoTe_2$ FET-based modulator and the corresponding output signal that follows FSK modulation. Due to the unwanted ASK occurring in the FSK modulated signal, the outputs for both logic levels are shown with different scale bars.

Finally, for PSK, we use V_{key} = 1.45 V, which shifts the logic levels "0" and "1" to V_{GS} = 1.45 and 3.45 V, respectively, as shown in Figure 2j. At V_{GS} = 3.45 V, the device operates in the n-branch of the transfer characteristics, where g_m is positive and hence $i_{DS}(t)$ is in phase with $c(t)$ as shown in Figure 2k. However, at V_{GS} = 1.45 V, the device operates in the p-branch of the transfer characteristics, where an increase in V_{GS} leads to a decrease in the I_{DS} and vice versa making g_m negative and hence $i_{DS}(t)$ is out of phase with $c(t)$ as shown in Figure 2l. Figure 2m shows the phase (ϕ) of $c(t)$ and $i_{DS}(t)$ corresponding to both logic levels shown in Figure 2k,l. Clearly, logic level "1" and "0" are represented by two different phases validating PSK modulation for V_{key} = 1.45 V. Note that the amplitude and frequency for $i_{DS}(t)$ corresponding logic level "1" and "0" remains the same owing to the symmetry in the transfer characteristics of $MoTe_2$ FET. Figure S5a,b (Supporting Information), respectively, show an example of binary input bitstream fed into the $MoTe_2$ FET-based modulator and the corresponding output signal that follows PSK modulation.

The fact that V_{Key} can be adjusted to switch between different modulation schemes, greatly simplifies the hardware design for the $MoTe_2$ FET-based modulator when compared to silicon CMOS-based mixing circuits. Also note that the average energy consumption per bit (E_{bit}) can be estimated using Equation (1)

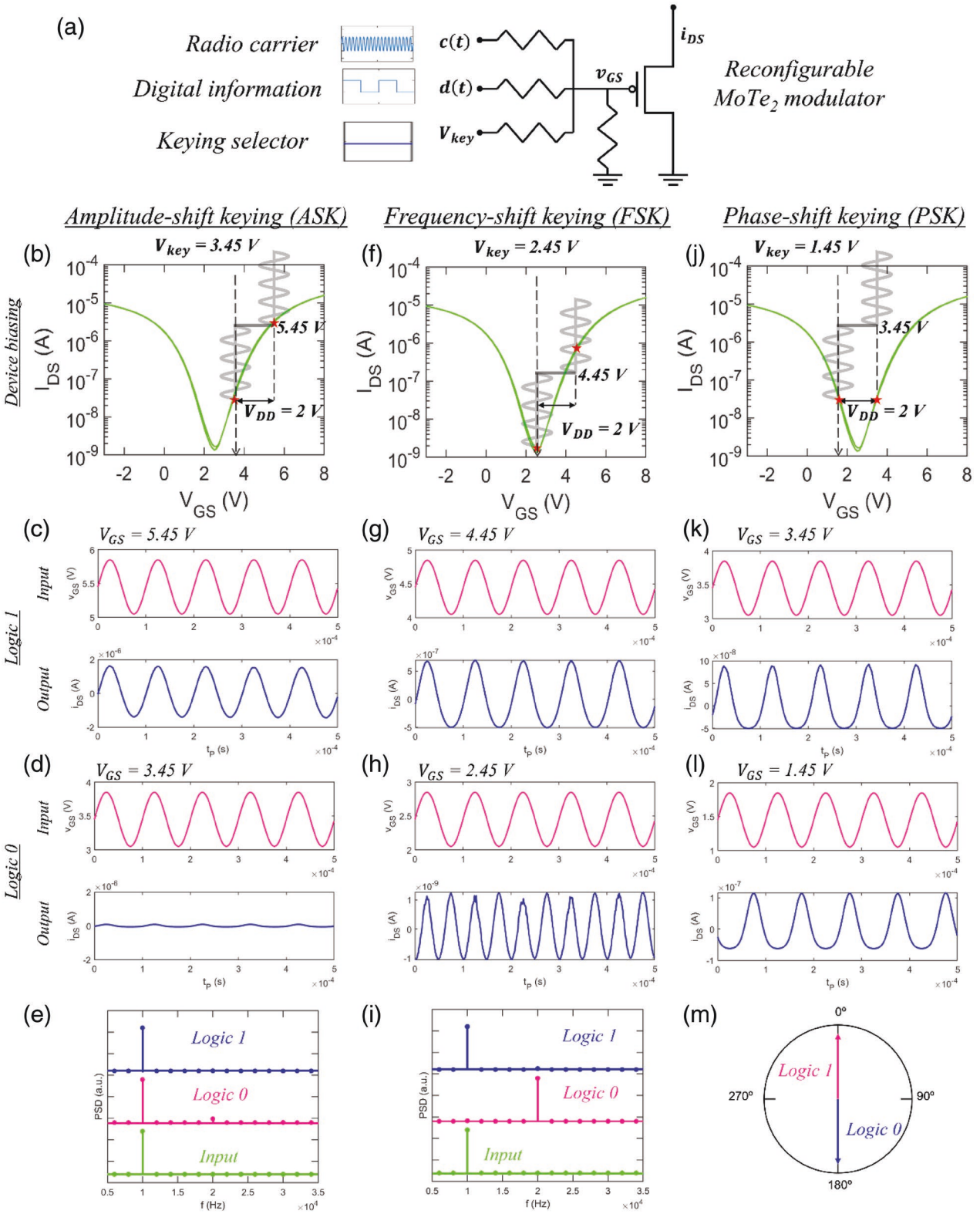


Figure 2. $MoTe_2$ FET-based reconfigurable modulator. a) Circuit schematic of the $MoTe_2$-FET-based modulator for ASK, FSK, and PSK. b) Modulator configuration for ASK using V_{key} = 3.45 V and c,d) corresponding input (v_{GS}) and output (i_{DS}) waveforms for logic "1" (c) and logic "0" (d). e) The power spectral density (PSD) of $c(t)$ and $i_{DS}(t)$ confirms the absence of frequency distortion. f) Modulator configuration for FSK using V_{key} = 2.45 V. Corresponding v_{GS} and i_{DS} waveforms for g) logic "1" and h) logic "0" and i) the PSD of $c(t)$ and $i_{DS}(t)$. j) Modulator configuration for PSK using V_{key} = 1.45 V. Corresponding v_{GS} and i_{DS} waveforms for k) logic "1" and l) logic "0" and m) the phase of $i_{DS}(t)$ in comparison to $c(t)$.

$$E_{\text{bit}} = \frac{1}{2} C_G \left[p V_{\text{key}}^2 + (1-p)\left(V_{\text{key}} + V_{DD}\right)^2 \right] + \frac{\sqrt{\overline{i_{DS}^2}}\, V_{DS}}{f_c}; C_G = \varepsilon_0 \varepsilon_{\text{ox}} WL / t_{\text{ox}} \quad (1)$$

where, C_G, $\varepsilon_0 = 8.85 \times 10^{-12}$ F m^{-1} is the vacuum permittivity, $\varepsilon_{\text{ox}} = 10$, and $t_{\text{ox}} = 50$ nm are, respectively, the relative permittivity and thickness of Al_2O_3, $W = 3.5$ µm and $L = 1$ µm are, respectively, the channel width and length of the $MoTe_2$ FET, and p is the probability of obtaining "1" in $d(t)$. For, $p = 0.5$, we estimated $E_{\text{bit}} \approx 70$, 9, and 7 pJ, for ASK, FSK, and PSK, respectively. Also note that the footprint of the active device is ≈3.5 µm^2.

The $MoTe_2$ modulator described above can also be used for encoding 2-bit of binary data combining the ASK and the PSK schemes, which can improve the bandwidth efficiency by 100%. If we use $V_{\text{key}} = -0.55$ V, and represent the logic levels, "00", "01", "10", and "11", using 0, 2, 4, and 6 V, respectively, then the corresponding V_{GS} values will be –0.55, 1.45, 3.45, and 5.45 V, respectively, as shown in **Figure 3**a. Figure 3b shows the input signal to the $MoTe_2$ FET-based modulator when the different logic levels are superimposed with $c(t)$ and Figure 3c shows the corresponding $i_{DS}(t)$. Figure 3d shows the phase for $c(t)$ and $i_{DS}(t)$. Clearly, each logic level is represented by a different point in the amplitude-phase space in Figure 3e. In other words, the same $MoTe_2$ FET-based modulator can be configured for APSK modulation. The above results reaffirm the design simplicity and energy, area, and bandwidth efficiency of $MoTe_2$ FET-based reconfigurable modulator.

3. Non-Volatile Analog Memory

Next, we show analog and nonvolatile programmability of $MoTe_2$ FETs, which can be used to design modulators that can encode 3-bit binary data improving the bandwidth efficiency even further. When the back-gate stack of the $MoTe_2$ FET is subjected to successive positive "program" (V_P) voltage pulses of amplitude 14 V and negative "erase" (V_E) voltage pulses of amplitude -14 V, each applied for $\tau_{P/E} = 100$ ms, the transfer characteristics exhibit positive and negative shifts, respectively, as shown in **Figure 4**a,b, for $n = 20$ pulses. The corresponding V_{Dirac} as a function of n is shown in Figure 4c,d. The shift in the transfer characteristics can be explained using the phenomenon of charge trapping and detrapping at and near the $MoTe_2$/Al_2O_3 interface. Note that trap states can originate from defects/imperfections in the dielectric and/or adsorbed species at the

2D/dielectric interface as reported in various earlier studies.[28–30] These states can also be engineered at desired energetic locations by introducing intentional defects in the 2D channel material.[31,32] Carrier occupancy in these trap states follow Fermi–Dirac distribution. As illustrated using the energy band diagrams in Figure S6 (Supporting Information), at equilibrium, i.e., in the absence of any gate bias, the trap states with energy levels above the Fermi energy (E_F) are empty, whereas the ones below E_F are filled. When the $MoTe_2$ FET is subjected to a negative "erase" (V_E) voltage pulse, electrons are released (detrapped) from these trap states leaving them positively charged. This leads to the screening of the back-gate bias, which is reflected as a shift in the V_{Dirac} following Equation (2)

$$\Delta V_{\text{Dirac}} = -\frac{Q_T}{C_{\text{ox}}}; C_{\text{ox}} = \frac{C_G}{WL} = \frac{\varepsilon_0 \varepsilon_{\text{ox}}}{t_{\text{ox}}} \quad (2)$$

where Q_T is the magnitude of effective positive charge at or near the 2D/dielectric interface. Similarly, when the $MoTe_2$ FET is subjected to a positive "program" (V_P) voltage pulse, electrons are

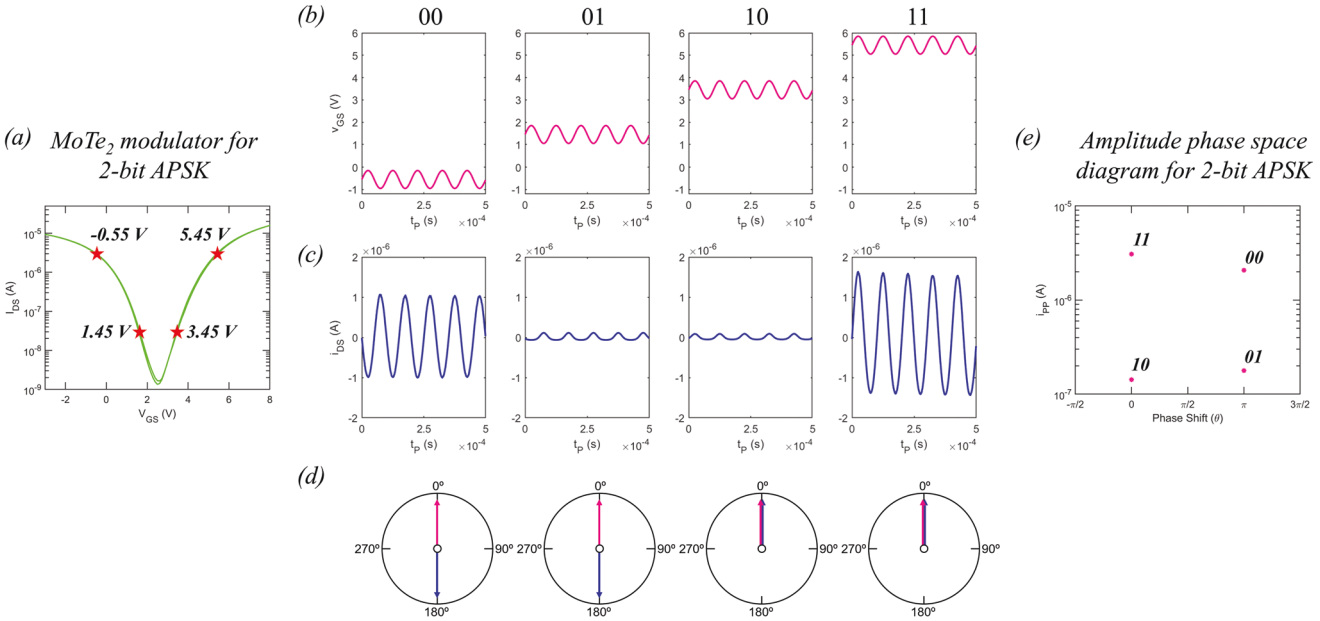


Figure 3. $MoTe_2$ FET-based modulator for 2-bit amplitude phase shift keying (APSK). a) Biasing of the MoTe2 modulator to enable 2-bit APSK. Here, we use $V_{\text{key}} = -0.55$ V, and represent the logic levels, "00", "01", "10", and "11", using 0, 2, 4, and 6 V, respectively, such that the corresponding V_{GS} values will be –0.55, 1.45, 3.45, and 5.45 V, respectively. b) The input signal to the $MoTe_2$ FET based modulator when the different logic levels are superimposed with $c(t)$ and c) the corresponding $i_{DS}(t)$. d) The phase for $c(t)$ (in pink) and $i_{DS}(t)$ (in blue). e) Each logic level is represented by a different point in the amplitude-phase space confirming APSK modulation.

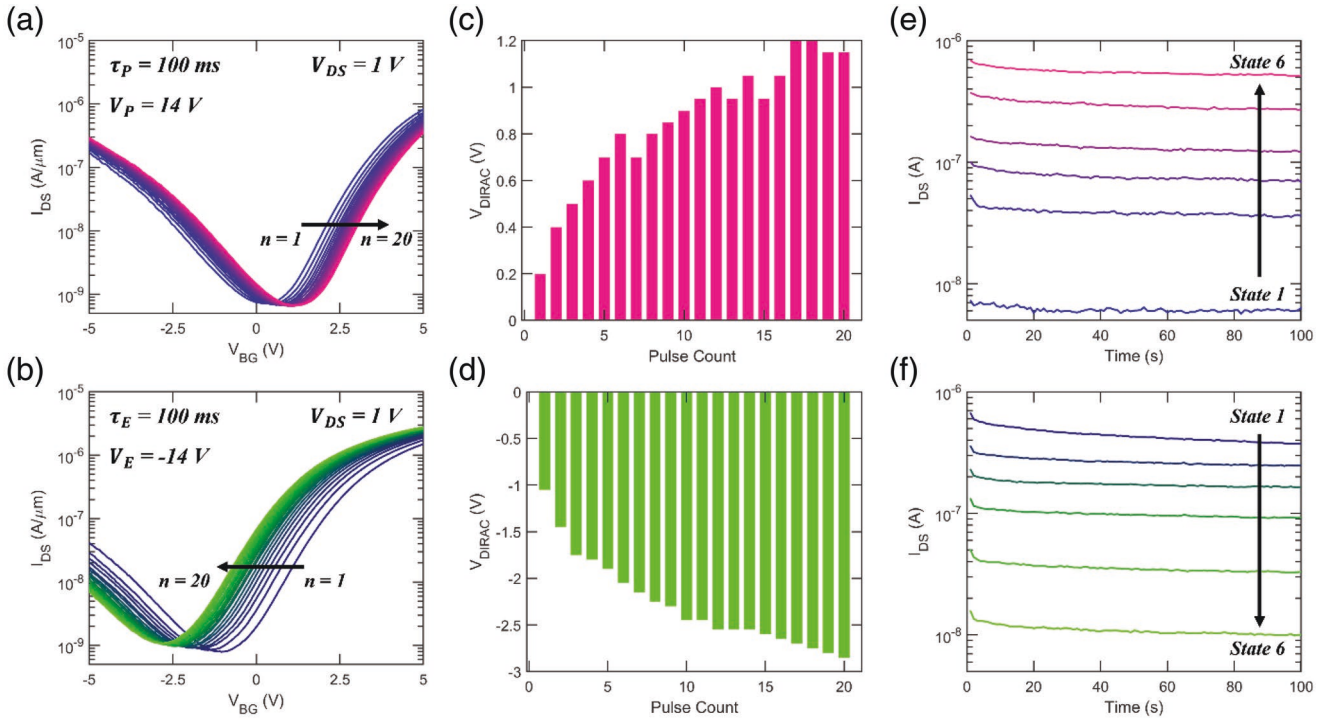


Figure 4. Analog and nonvolatile programming of $MoTe_2$ FET. a,b) Transfer characteristics of the $MoTe_2$ FET measured after the application of successive positive "program" (V_P) voltage pulses of amplitude 14 V (a) and negative "erase" (V_E) voltage pulses of amplitude –14 V (b), each for $\tau_{P/E}$ = 100 ms, for n = 20 pulses. The corresponding V_{Dirac} as a function of n for c) programming and d) erase pulses. The shift in the transfer characteristics can be explained using the phenomenon of charge trapping and detrapping at and near the $MoTe_2/Al_2O_3$ interface. e,f) Nonvolatile retention of 6 representative programmed (e) and erased (f) states for 100 s.

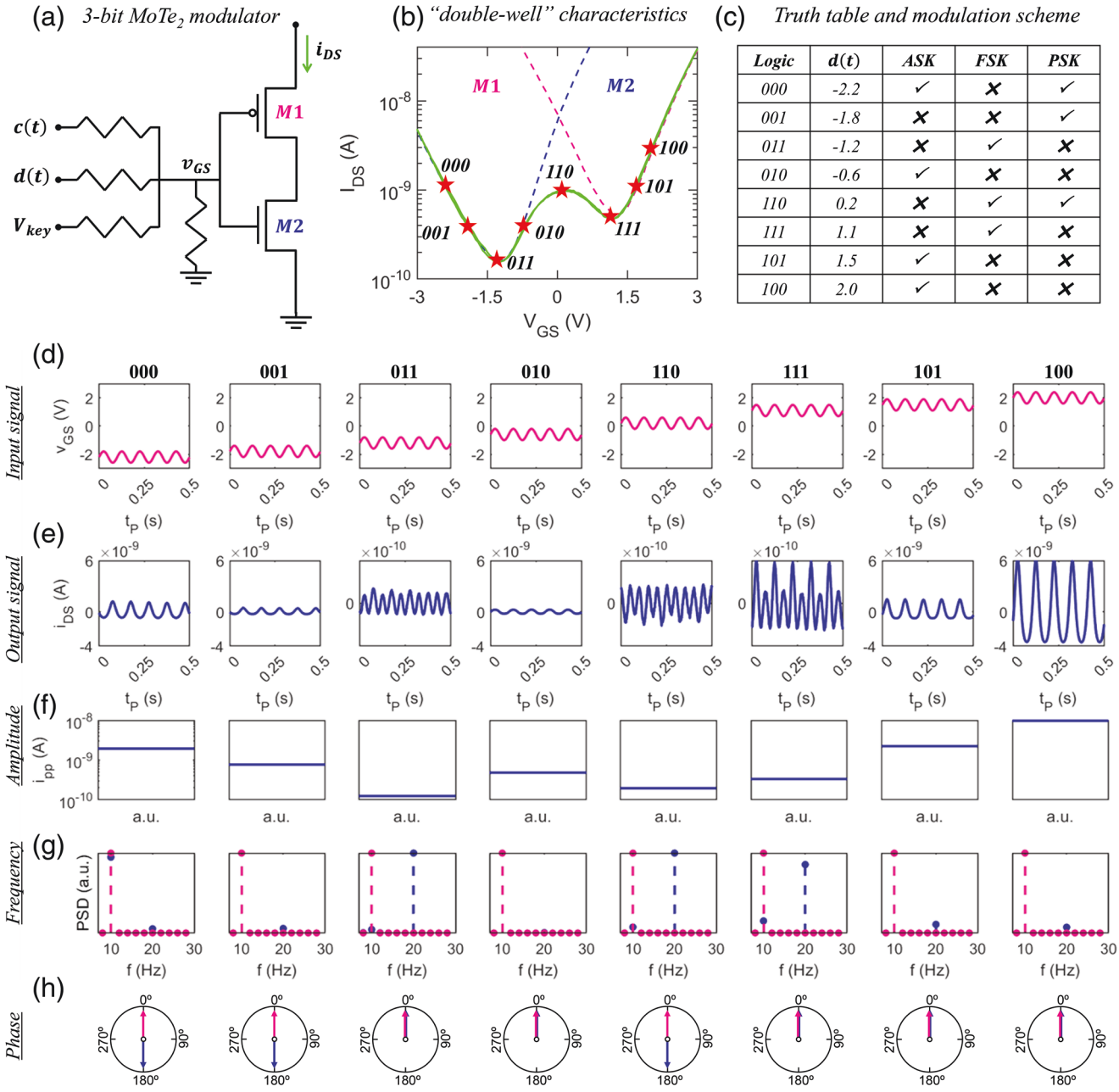
captured back (trapped) into the trap states restoring the V_{Dirac}. Note that the number of electrons getting trapped/detrapped can be controlled by the pulse number, magnitude, and duration, which enable us to have an analog control of the V_{Dirac} of the $MoTe_2$ FET. Interestingly, the trapping and detrapping processes were found to be nonvolatile as shown in Figure 4e,f for 6 representative programmed and erased states for at least 100 s.

4. Multibit Keying using "Double-Well" Characteristics

As mentioned earlier, to encode 3-bit binary data, $M = 8$ unique combinations of amplitude, frequency, and phase for the output current, $i_{DS}(t)$, are required, which is difficult to achieve using the ambipolar transfer characteristics of a single $MoTe_2$ FET. However, when two $MoTe_2$ FETs, $M1$ and $M2$, that are programmed to have different V_{Dirac} are connected in series as shown in **Figure 5**a, the transfer characteristics change significantly as shown in Figure 5b. Note that, while there is some device-to-device variation in the V_{Dirac} for the as-fabricated $MoTe_2$ FETs, most of them lie within V_{GS} –0.5 to 0.5 V, which is insufficient for the design of the multibit modulator. Therefore, programming capability is critical to have a larger shift in V_{Dirac} for each $MoTe_2$ FET. The transfer characteristics of $M1$ are shifted to the positive side by programming with positive gate voltage pulses, while those of $M2$ are shifted to the negative side by using negative gate voltage pulses as shown using the dotted lines in Figure 5b. The difference in I_{Dirac} between $M1$ and $M2$ can be ascribed to different thicknesses of the corresponding exfoliated $MoTe_2$ flake leading to slightly different bandgap and/or Fermi level alignment with the metal contacts. When connected in series, I_{DS} shows an asymmetric "double-well" feature over the range of the applied V_{GS}. Note that having a common back-gate means that the voltage sweeps applied to the gates of $M1$ and $M2$ are identical.

For $V_{GS} < 0$ V, $M2$ dominates the transfer curve since it is in a low conductance state, whereas, for $V_{GS} > 0$ V, $M1$ dominates the transfer curve since it is now in the low conductance state. This leads to a very interesting "double-well" transfer characteristic where there is one peak and two valleys in the values of I_{DS}. As we will elucidate next, different biasing points chosen along this highly nonmonotonic transfer characteristics can give rise to different values of amplitude, frequency, and phase for i_{DS} for the same $c(t)$, which forms the basis for multibit modulation.

The truth table, corresponding voltage biases, and the combination of different schemes for the 3-bit modulator are shown in Figure 5c and are marked in Figure 5b. Note that we are using a Gray code to represent 3-bit binary values. Here, the binary numeral system is such that two successive values differ in only one bit, which aids in error correction in digital communication. Figure 5d,e, respectively, show the v_{GS} representing different logic levels and the corresponding modulated i_{DS}. While most of the modulations are in accordance with our previous discussion, we would like to specifically highlight the



Logic	d(t)	ASK	FSK	PSK
000	-2.2	✓	✗	✓
001	-1.8	✗	✗	✓
011	-1.2	✗	✓	✗
010	-0.6	✓	✗	✗
110	0.2	✗	✓	✓
111	1.1	✗	✓	✗
101	1.5	✓	✗	✗
100	2.0	✓	✗	✗

Figure 5. 3-Bit modulation based on "double-well" characteristics of $MoTe_2$ FETs. a) Circuit schematic of a 3-bit modulator by integrating two $MoTe_2$ FETs, *M*1 and *M*2, that are programmed to have different V_{Dirac}. b) Transfer characteristics of the modulator with unique "double-well feature. The dotted lines show the transfer characteristics of *M*1 (pink) and *M*2 (blue). For $V_{GS} < 0$ V, *M*2 dominates the transfer curve, whereas for $V_{GS} > 0$ V, *M*1 dominates the transfer curve, respectively. This leads to the asymmetric "double-well" modulator characteristic with one peak and two valleys in the values of I_{DS}. c) The truth table, corresponding voltage biases, and the combination of different schemes for the 3-bit modulator, using a Gray coding scheme. d) The input (v_{GS}) and e) the corresponding output (i_{DS}) waveforms for different logic levels. f) Peak-to-peak amplitude (i_{pp}), g) PSD pink: $c(t)$ blue: $i_{DS}(t)$, and h) phase relative to $c(t)$ for $i_{DS}(t)$ corresponding to different logic levels. Clearly, through the combination of one or more keying schemes, 3-bit modulation can be achieve based on the integration of two preprogrammed ambipolar $MoTe_2$ FETs.

modulation for logic level "100", as it corresponds to $V_{GS} = 0$ V, i.e., the inflection point on the "anti-ambipolar" region of the transfer characteristics. It is similar to the logic level "010" and "101", represented by $V_{GS} = -1.5$ and 1.1 V, respectively, which correspond to the inflection points on the two "ambipolar" regions of the transfer characteristics and therefore lead to full-wave rectification of $c(t)$ resulting in frequency doubling in $i_{DS}(t)$. However, the $i_{DS}(t)$ corresponding to logic level "100" is out of phase when compared to $i_{DS}(t)$ corresponding to logic level, "010" and "101". Figure 5f–h, respectively, shows the peak-to-peak amplitude (i_{pp}), PSD, and phase relative to $c(t)$ for $i_{DS}(t)$ corresponding to different logic levels. Clearly, through the

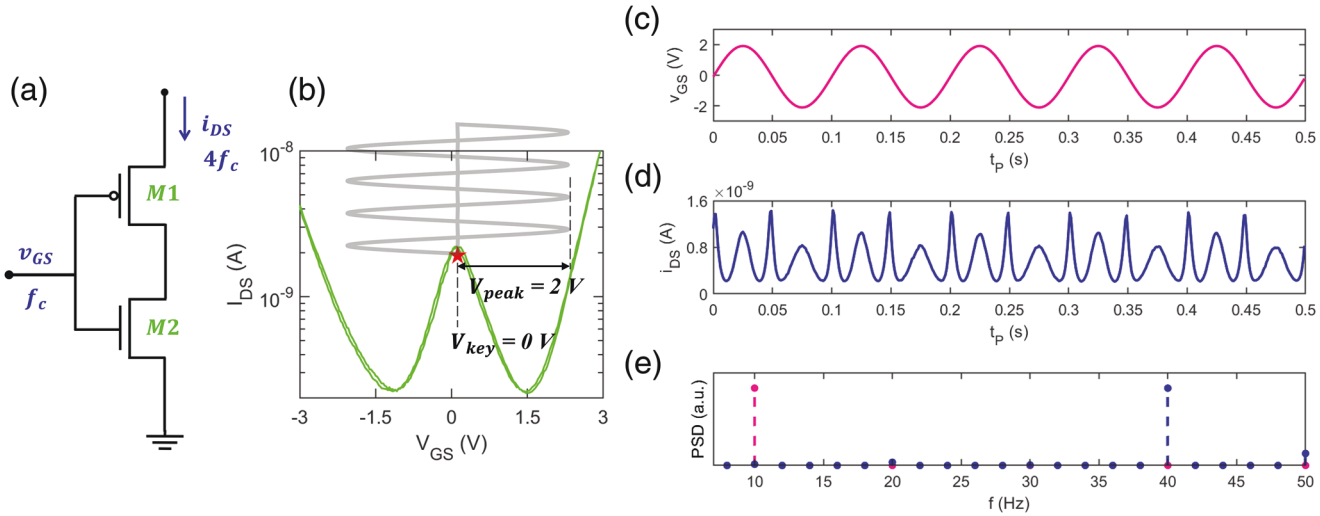


Figure 6. Frequency quadrupler based on a $MoTe_2$ modulator. a) Circuit schematic and b) symmetric "double-well" transfer characteristics for the $MoTe_2$ FETs based frequency quadrupler. Here, *M*1 and *M*2 are chosen such that their I_{Dirac} values are approximately the same. The V_{Dirac} for *M*1 and *M*2 are programmed and shifted toward positive and the negative directions, respectively. c) The input (v_{GS}) and d) the corresponding output (i_{DS}) waveforms for the frequency quadrupler. e) The PSD of $c(t)$ and i_{DS} (t) confirm the successful realization frequency quadrupling.

combination of one or more keying schemes, we have been able to demonstrate a 3-bit modulator based on the integration of two preprogrammed ambipolar $MoTe_2$ FETs. Naturally, the modulator has a small footprint of ≈7 μm^2, consumes miniscule energy of ≈70 pJ bit^{-1} for keying, and offers 200% more bandwidth compared to any of the binary ASK, FSK, or PSK schemes.

Finally, we exploit the "double-well" characteristics of two integrated $MoTe_2$ FETs for frequency quadrupling. Note that frequency multipliers are used extensively in frequency synthesizers and communications circuits. It is often more economical to develop a lower frequency signal with low-power consumption using less expensive devices, and then use cascaded frequency multipliers to generate an output frequency in the microwave or millimeter wave range. **Figure 6**a shows the circuit schematic for the frequency quadrupler. In order to synthesize a frequency quadrupler, *M*1 and *M*2 are chosen such that their I_{Dirac} values are approximately the same. After programming *M*1 and *M*2 to the positive and the negative directions respectively, and using the same circuit layout as before, the resulting transfer characteristic is found to be symmetric about V_{GS} = 0 V as shown in Figure 6b. As has been shown previously, by choosing the DC bias, V_{Key}, at the peak or the valleys of the anti-ambipolar characteristic, a full wave rectification effect is obtained since i_{DS} swings to both the p- and the n-branches, which leads to frequency doubling. The same effect is utilized here except the sinusoidal carrier signal is of larger amplitude, V_{pp} = 2 V. V_{pp} is sufficiently large such that i_{DS} swings past the valleys on both the positive and the negative sides. Every time v_{GS} crosses a peak or a valley in the i_{DS}, a peak in the i_{DS} is obtained. In one complete cycle of v_{GS}, the peak and the valleys are traversed for a total of 4 times. This leads to an output current, $i_{DS}(t)$, whose frequency is quadruple of the input carrier wave, $c(t)$ as shown in Figure 6c,d. The PSD of $c(t)$ and i_{DS} are shown in Figure 6e, which further confirm the successful realization of a frequency quadrupler.

5. Conclusion

We have demonstrated a reconfigurable $MoTe_2$ FET as a multipurpose modulator. The ambipolar characteristics of $MoTe_2$ have been harnessed to achieve ASK, FSK, and PSK modulation using a single device that greatly reduces the modulator footprint and energy consumption. We have also shown that the same $MoTe_2$ FET can be used for APSK modulation of 2-bit binary data improving the bandwidth efficiency by 100%. The $MoTe_2$ FETs also possesses arbitrarily programmable analog memory states, which can be used to adjust their Dirac voltage. By integrating two preprogrammed $MoTe_2$ FETs, we demonstrate unique "double-well" transfer characteristics, which can be exploited for 3-bit data modulation, increasing the bandwidth efficiency to 200%. Finally, we demonstrate a frequency quadrupler using the $MoTe_2$ modulator. Our work uses the unique transport characteristics of $MoTe_2$ FET(s) and its programmability to implement diverse digital communication primitives in a compact and reconfigurable device. This work highlights the importance of material and device level innovations to achieve energy, area, and bandwidth efficiency for emerging IoT edge communication.

6. Experimental Section

Flakes of 2H $MoTe_2$ were micromechanically exfoliated on the Al_2O_3/Pt/TiN/p^{++} Si substrate. The source and the drain contacts were defined using electron beam lithography. First, the sample was spin coated with methyl methacrylate (MMA) followed by A3 poly(methyl methacrylate) (PMMA). Then the sample was exposed and subsequently developed by using a 1:1 mixture of MIBK and IPA for 60 s followed by IPA for 45 s. Using e-beam evaporation, 40 nm of nickel (Ni) and 30 nm of gold (Au) were deposited. Finally, liftoff was performed by immersing the sample in acetone for 30 min followed by IPA for 30 min which removed the evaporated metal from the sample except the source/drain patterns. Electrical characterization was performed under high vacuum (≈10^{-6} Torr) using a Lakeshore CRX-VF probe-station and a Keysight B1500 parameter analyzer.

Supporting Information

Supporting Information is available from the Wiley Online Library or from the author.

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Conflict of Interest

The authors declare no conflict of interest.

Author Contributions

S.D. conceived the idea and designed the experiments. S.D. fabricated the devices and performed the measurements. All authors contributed to the preparation of the manuscript.

Data Availability Statement

The data that support the findings of this study and the codes used for plotting the data are available from the corresponding author upon reasonable request.

Keywords

ambipolar transport, digital modulators, double-well characteristics, $MoTe_2$ field-effect transistors

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