

Logic Locking of Integrated Circuits Enabled by Nanoscale MoS₂-Based Memtransistors

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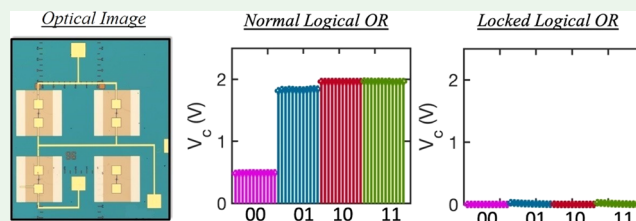
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ABSTRACT: With an ever-increasing globalization of the semiconductor chip manufacturing supply chain coupled with soaring complexity of modern-day integrated circuits (ICs), intellectual property (IP) piracy, reverse engineering, counterfeiting, and hardware trojan insertion have emerged as severe threats that have compromised the security of critical hardware components. Logic locking (LL) is an IP protection technique that can mitigate these threats by locking a given IC with a secret key. Earlier LL demonstrations based on traditional silicon complementary metal-oxide-semiconductor (CMOS) technology and emerging memristors require significant hardware investment in the form of additional input gates and extensive CMOS peripherals, rendering them area- and energy-inefficient. In this article, we demonstrate multiple two-dimensional (2D) nanoscale memtransistor-based programmable logic gates such as AND, NAND, OR, XOR, and NOT gates, each of which can be locked/unlocked without requiring peripherals and at minuscule energy expenditure (<1 pJ). We also show that SAT-solver is unsuccessful in breaking into any of the ISCAS'85 benchmark circuits that utilize our LL scheme. The massive resilience to SAT-attack is attributed to the prowess of programmable 2D memtransistors which enable device-level LL of all the gates in each of the benchmark circuits. Given that 2D transistors are drawing increasing attention of chip manufacturing corporations like Intel, TSMC, etc., to replace and/or augment silicon at aggressively scaled technology nodes, our demonstration of area- and energy-efficient LL can be considered as a step toward the realization of secure ICs enabled by 2D nanoscale memtransistors.

KEYWORDS: integrated circuits, two-dimensional material, logic locking, security, in-memory computing



INTRODUCTION

The increasing cost and complexity of integrated circuits (ICs) have spawned an era of fabless semiconductor companies with extensive reliance on globalized and distributed IC design flows.¹ In this highly interconnected yet physically dispersed ecosystem, untrusted parties can easily obtain access to intellectual properties (IPs), giving rise to major security threats such as IP piracy, counterfeiting, and overbuilding.^{2–4} As a result, such hardware-compromised chips are becoming more pervasive in the semiconductor industry, raising significant concerns for the governments, consumers, and businesses involved.^{5–7} As per a report published by the Senate Armed Services Committee, the presence of more than a million counterfeit components in US military defense systems has severely impacted their security and reliability in mission-critical applications involving military airplanes, missiles and warfare systems, and communication.⁸ Furthermore, ICs may be recycled, remarked, reverse engineered, or even sold illegally.⁹ Additional threats involving trojan insertion and illegal ownership claims over an IP further compound the problem. Therefore, protecting an IC/IP design from potentially unscrupulous groups and above-mentioned attack

threats present within the supply chain is of paramount importance.

A potential solution to mitigate these security threats is logic locking (LL), wherein a circuit design is locked using a secret key. To retrieve the correct circuit functionality (correct logical outputs), a valid key must be provided to this locked design, one which is only known to the original designer. While a number of alternative countermeasures such as IC camouflaging,¹⁰ split manufacturing,¹¹ and IC metering¹² have also been proposed, LL, in particular, has received significant attention from the hardware security research community due to its versatility in protecting the IP. Conventional literature has implemented LL by introducing additional logic elements such as XOR/XNOR¹³ and AND/OR¹⁴ gates into the original design at random locations, thereby maximizing the hamming

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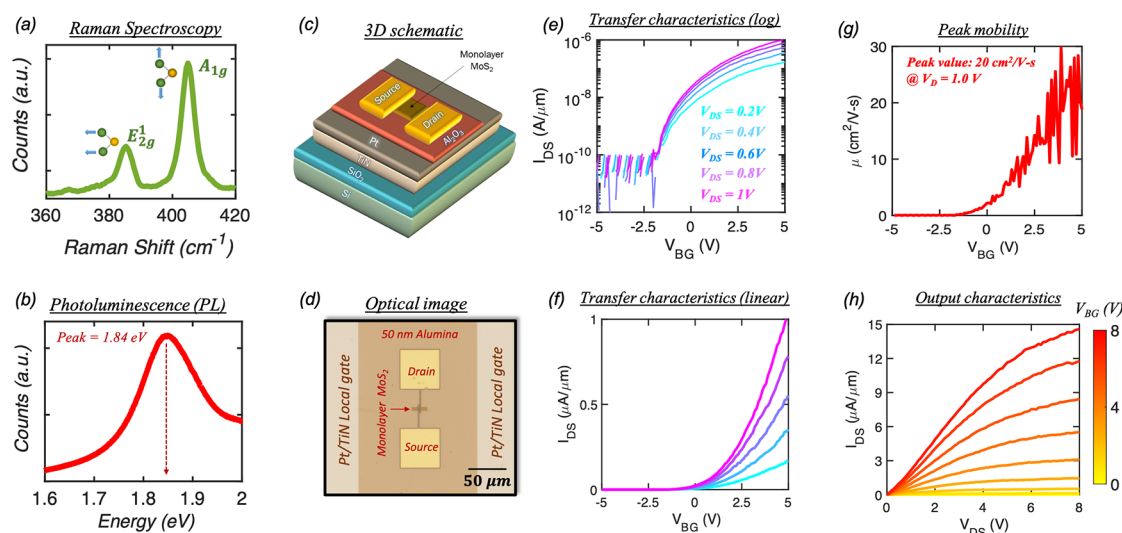


Figure 1. Characterization of monolayer MoS₂-based 2D memtransistor. (a) Raman spectra and (b) photoluminescence (PL) spectra of a representative MoS₂ channel using a 532 nm laser. (c) Three-dimensional (3D) schematic and (d) optical image of a representative monolayer MoS₂-based 2D memtransistor with a local back-gate stack comprising atomic layer deposition (ALD)-grown 50 nm Al₂O₃ with a 40/30 nm Pt/TiN electrode deposited using sputtering on SiO₂/p⁺⁺-Si substrate. Transfer characteristics, i.e., source-to-drain current (I_{DS}) versus back-gate voltage (V_{BG}), at different drain-to-source bias (V_{DS}) values in (e) logarithmic and (f) linear scale, respectively, for a representative MoS₂ memtransistor with a channel length of 1 μ m and a channel width of 5 μ m. (g) Mobility versus V_{BG} extracted using the peak transconductance method. (h) Output characteristics, i.e., I_{DS} versus V_{DS} , at different V_{BG} values for the same MoS₂ memtransistor.

distance between the incorrect and correct outputs. Yet another technique involves introducing additional logic (black) states into the state transition graph where only the correct sequence of key-bits derived by an on-chip tamper-proof memory allows the design to operate correctly.^{15,16} Recently, a key destruction scheme based on a Ta/HfO₂ memristive crossbar array was also demonstrated for locking/unlocking.¹⁷ While promising, nearly all of the above-mentioned approaches employ additional peripheral logic elements, which ultimately increase the area overhead and consume significant amounts of energy. Additionally, most of the proposed schemes have only been simulated, with few experimental demonstrations. Therefore, to keep up with ever-shrinking technological nodes as per the International Technology Roadmap for Semiconductors (ITRS)¹⁸ and continued outsourcing of IC manufacturing to reduce development costs, innovative area- and energy-efficient security solutions are critical for securing ICs in this highly globalized and untrustworthy fabrication process.

In this regard, two-dimensional (2D) materials such as transition-metal dichalcogenides (TMDCs) have been intensely investigated in recent years for a plethora of diverse nanoscale applications beyond Moore's law.¹⁹ In particular, field effect transistors (FETs) fabricated from atomically thin TMDCs have shown immense potential for aggressive channel length scaling by suppressing the source-to-drain tunneling current, thereby improving the overall device performance and functionality.²⁰ With thicknesses <1 nm, monolayer TMDCs are resilient to short channel effects as a result of improved gate electrostatic and offer near-ideal switching characteristics for logic transistor applications.²¹ Recent experimental demonstrations of high-performance nanoscale FETs based on large-area (wafer-scale)-grown 2D TMDCs confirm these facts.^{22–25} Note that ICs based on 2D FETs have also been demonstrated for various analog, digital, memory, sensing, and neuromorphic applications.^{19,26–42} The above discussion clearly indicates that commercial implementation of 2D

technology is imminent; hence, it is important to mitigate the security threats that 2D FETs will encounter. Recently, we have demonstrated a wide range of security primitives including true random number generators, physically unclonable functions, IC camouflaging, watermarking, and anti-counterfeit solutions based on nanoscale 2D materials and devices.^{43–47} However, LL of 2D ICs is yet to be accomplished.

Here, we introduce 2D nanoscale memtransistors as in-memory compute primitives for the realization of LL in 2D ICs. Unlike two-terminal memristors, 2D memtransistors are three-terminal devices, with the additional gate terminal permitting both nonvolatile and analog programming of conductance states and electrostatic control of the 2D channel.^{48,49} By exploiting this in-memory compute capability, we were able to demonstrate LL of different logic gates, including NOT, AND, NAND, OR, and XOR gates, with no additional overhead, thereby offering an efficient hardware security solution to thwart IC piracy and overbuilding. The locking mechanism within these circuits results from the intentional application of a programming or erase pulse ($V_{P/E}$) to the local back-gate of our 2D nanoscale memtransistors, which shifts the threshold voltage (V_{TH}) and thereby clamps the output of the circuit in either a logic "1" or logic "0" state. The correct functionalities of these locked circuits can then only be recovered when the 2D memtransistor is reset back to its original baseline state through the application of an opposite polarity of voltage pulse ($V_{E/P}$) compared to the one used to originally lock the circuit. We also show that satisfiability (SAT) solver is unsuccessful in breaking into any of the ISCAS'85 benchmark circuits that utilize our LL scheme. The SAT-attack resilience is attributed to the prowess of the programmable 2D memtransistors that enable device-level LL of all of the gates in each of the benchmark circuits.

RESULTS AND DISCUSSION

Characterization of Monolayer MoS₂-Based 2D Memtransistor. MoS₂ is a layered semiconductor from the TMDC family having a general formula of MX₂, where M represents the transition metal (M = Mo, W) and X represents a chalcogen (X = S, Se, Te). With a weak out-of-plane van der Waals (vdW) coupling between successive layers and a strong in-plane bonding within each layer, monolayers can be easily separated from their bulk crystal with unparalleled electronic properties, thus making them attractive for developing next-generation area- and energy-efficient circuits. While prior studies on TMDCs have been primarily based on exfoliated multilayer and single-crystal flakes, practical realization of high-volume manufacturing of 2D-based dense logic integration technology requires high-quality large-area growth of these materials. The large-area monolayer MoS₂ used in our work was grown on a sapphire substrate at 950 °C via a previously described metal–organic chemical vapor deposition (MOCVD) technique.⁸⁵ The use of an epitaxial substrate and elevated growth temperatures allowed for the formation of a uniform, high-quality 2D film, which is critical for ensuring good device performance and low device-to-device variation. Raman and photoluminescence (PL) spectroscopy were used to assess the material quality using a 532 nm laser. Figure 1a shows the Raman spectra of a representative MoS₂ channel. The two characteristic peaks, i.e., the in-plane E_{2g} peak and the out-of-plane A_{1g} peak, were observed at 385 and 405 cm⁻¹, respectively; the peak separation of ~20 cm⁻¹ is characteristic of a monolayer MoS₂ film.³⁵ Furthermore, as shown in Figure 1b, a PL peak was observed at 1.85 eV; this was attributed to the direct bandgap transition at the K-point in the Brillouin zone in monolayer MoS₂ and is completely subdued in bulk MoS₂.

Figure 1c,d, respectively, show the 3D schematic and optical image of a representative 2D MoS₂ memtransistor with a channel length (*L*) of 1 μm and a channel width (*W*) of 5 μm. Details on the MoS₂ film transfer and memtransistor fabrication can be found in the Methods section. Figure 1e,f, respectively, show the transfer characteristics, i.e., source-to-drain current (*I*_{DS}) as a function of applied back-gate voltage (*V*_{BG}), of a representative MoS₂ FET measured at different source-to-drain biases (*V*_{DS}) in the logarithmic and linear scales. Clearly, n-type-dominated carrier transport is observed due to the pinning of the metal Fermi level near the conduction band facilitating enhanced electron injection; this observation is consistent with our earlier reports.⁵⁰ In addition, an excellent ON/OFF current ratio of ~10⁵ is observed. A threshold voltage (*V*_{TH}) of ~0 V was extracted using linear scale estimation and the field effect mobility (*μ*_{FE}) in Figure 1g extracted from the peak transconductance ($g_m = \frac{dI_{DS}}{dV_{BG}}$) was 20 cm²/(V·s). Finally, Figure 1h shows the output characteristics, i.e., *I*_{DS} versus *V*_{DS}, for different *V*_{BG} values. *I*_{ON} was found to be ~15 μA/μm for *V*_{DS} = 8 V at *V*_{BG} = 8 V, indicating the superior performance of our 2D memtransistors.

Programmability in MoS₂ Memtransistors. In this section, we demonstrate the ability of our MoS₂ FETs to be programmed to any given desirable conduction state, which is central to our LL scheme, as a result of the application of two types of voltage pulses to the local back-gate: a negative programming pulse (*V*_P) and a positive erase pulse (*V*_E). Figure 2a,b show the transfer characteristics of a representative

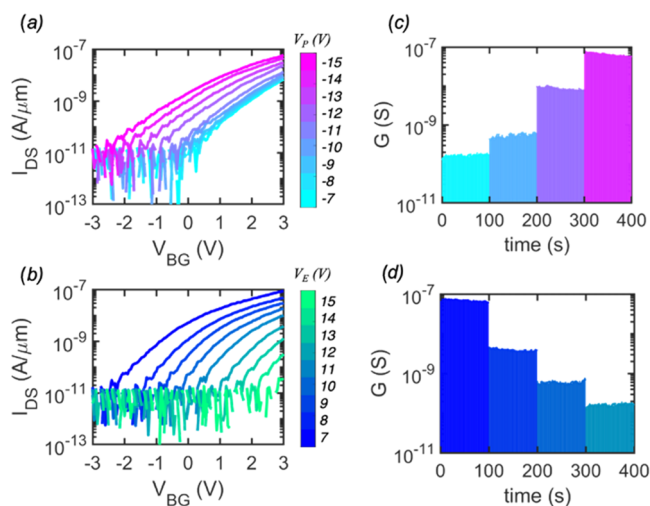


Figure 2. Programmability in MoS₂ 2D memtransistors. Transfer characteristics showing analog (a) programming and (b) erase operations in a representative 2D memtransistor when subjected to negative “Write” (*V*_P) and positive “Erase” (*V*_E) voltage pulses of different magnitudes ranging from 7 to 15 V that are applied to the local back-gate. Both the pulse widths were fixed for a duration of 100 ms. The respective shifts in the threshold voltages (*V*_{TH}) are attributed to the carrier detrapping/trapping at the MoS₂ and the local gate stack interface, thereby allowing us to modulate a given device to a desired conduction state, i.e., a high-conduction state (HCS) or a low-conduction state (LCS). Nonvolatile retention for four representative (c) programmed and (d) erased states for a total duration of 100 s.

MoS₂ FET following the application of *V*_P and *V*_E, respectively, at magnitudes ranging from 7 to 15 V and with the same pulse width (*τ*_{P/E}) of 100 ms. The respective negative and positive shifts observed in the *V*_{TH} of the memtransistor are the result of charge trapping and detrapping at and/or near the MoS₂/Al₂O₃ interface, as has been described in our earlier works.^{46,51} Note that the increase in the shift of *V*_{TH} with increasing magnitude of *V*_P and *V*_E is attributed to the greater number of charges getting trapped and detrapped, respectively, at the channel/dielectric interface. Analysis of the stability of the programmed memory states clearly shows the non-volatile retention of our devices, as evident from the plots in Figure 2c,d. Additionally, the programming/erase energy expenditure, calculated based on $E_W = 1/2 C_g (V_{P/E})^2$, where $C_g = WLe_0\epsilon_{ox}/t_{ox}$ is the gate capacitance, $\epsilon_0 = 8.85 \times 10^{-12}$ F/m is the vacuum permittivity, and $\epsilon_{ox} = 10$ and $t_{ox} = 50$ nm are the relative dielectric constant and thickness of Al₂O₃ dielectric gate, respectively, was found to be miniscule (<1 pJ). Supporting Information S1 shows the associated band diagrams explaining the charge trapping and detrapping process.

Demonstration of Logic Locking (LL) in 2D-Memtransistor-Based Logic Families. Logic gates are fundamental building blocks of digital integrated circuits (ICs) and play a critical role in modern computing architectures and microprocessors. Here, we successfully integrate MoS₂ memtransistors fabricated on separate local back-gate islands to create five different logical functionalities (inverter, AND gate, NAND gate, OR gate, and XOR gate) and demonstrate their respective locking schemes. Figure 3a,b show an optical image and a circuit diagram, respectively, of our fabricated inverter. An inverter is a logic circuit that outputs a voltage representing the opposite logic level to its input. The inverter

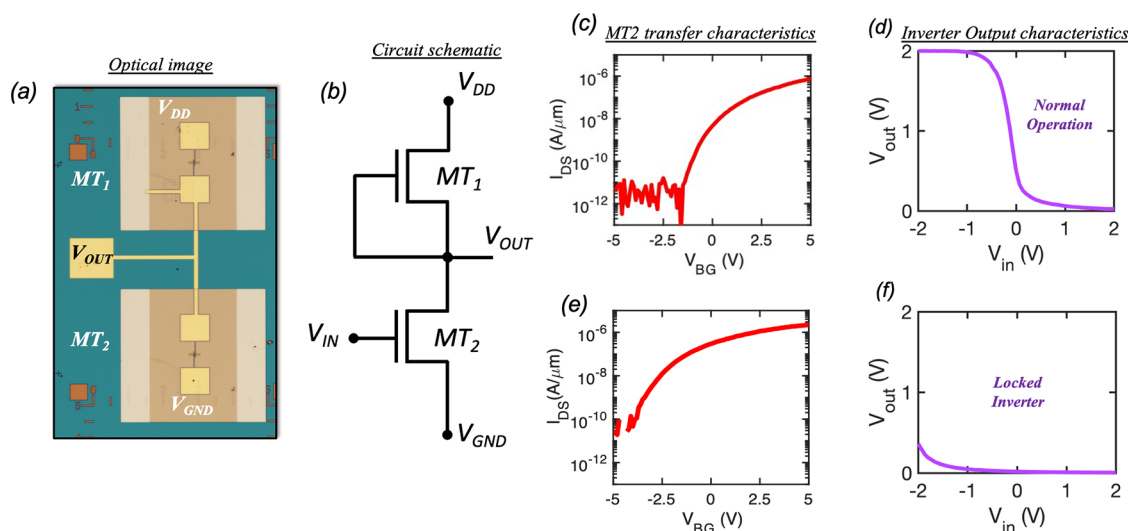


Figure 3. Demonstration of LL in MoS₂ inverter. (a) Optical image and (b) circuit diagram of an inverter consisting of two memtransistors, MT₁ and MT₂. Note that MT₁ operates in depletion mode (the gate is shorted to the source), whereas MT₂ operates in enhancement mode. (c) Baseline transfer characteristics of MT₂ and (d) the corresponding output characteristics of an inverter showing normal operation, where V_{out} represents the opposite logic of the V_{in} . (e) Transfer characteristics of MT₂ post application of a program pulse of -12 V and (f) the corresponding locked inverter output, where V_{out} is clamped to V_{GND} .

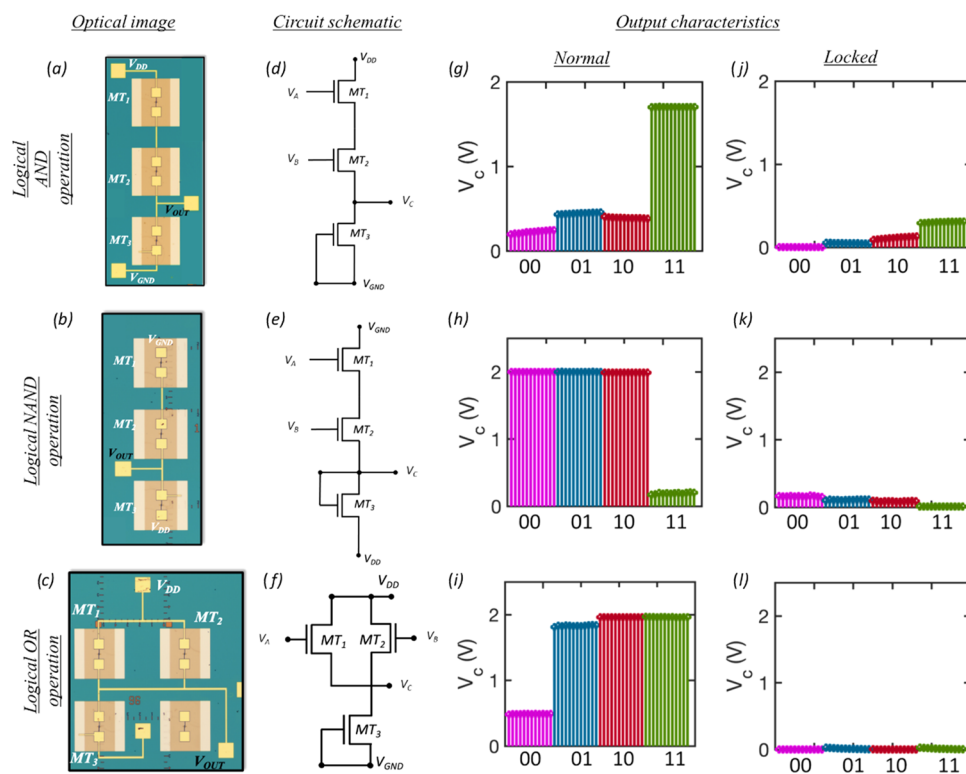


Figure 4. Demonstration of LL for 2D memtransistor-based AND, NAND, and OR gates. (a–c) Optical images and (d–f) the corresponding circuit diagram of AND, NAND, and OR gates comprising three monolithic integrated MoS₂ memtransistors, MT₁, MT₂, and MT₃. Output characteristics of the respective logic functionalities under (g–i) normal (unlocked) and (j–l) locked operations.

demonstrated in this work was constructed using a depletion-mode (D-mode) memtransistor (MT₁), formed by shorting the gate and source terminals, and an enhancement-mode (E-mode) memtransistor (MT₂). For our demonstration, a specific supply voltage, $V_{DD} = 2$ V, was chosen for operating the circuits. Thus, a voltage level close to 2 V represents the logic state “1”, while a voltage level close to 0 V represents the logic state “0”. We first determined the baseline state of MT₂

by measuring its transfer characteristics, as shown in Figure 3c. Next, we evaluated the logic functionality of the inverter by plotting the input (V_{in}) versus the output (V_{out}) voltage transfer curve, as shown in Figure 3d. When $V_{in} = 0$ V (logic state “0”) is applied to the gate terminal of MT₂, the E-mode memtransistor becomes nonconductive in comparison to the D-mode memtransistor, resulting in $V_{out} = V_{DD} = 2$ V (logic state “1”). However, for $V_{in} = 2$ V (logic state “1”), the E-mode

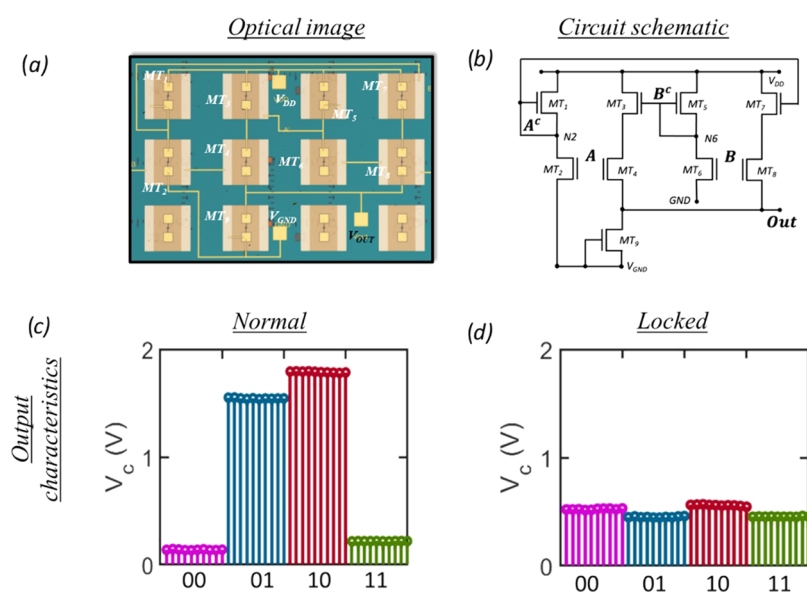


Figure 5. Demonstration of LL for 2D memtransistor-based XOR gate. (a) Optical image and (b) the corresponding circuit diagram of XOR gate comprising nine monolithic integrated MoS₂ memtransistors. Output characteristics for the XOR logic functionality under (c) normal (unlocked) and (d) locked operations.

memtransistor, MT₂, becomes more conductive than the D-mode memtransistor, MT₁, effectively clamping the V_{out} to 0 V (logic state “0”). Thus, to lock the inverter, it is evident that MT₂ must remain more conductive than MT₁ at all times. This is achieved by applying V_p = −14 V to the gate terminal of MT₂, which shifts its V_{TH} to a more negative value, as shown in Figure 3e. This ensures that MT₂ now remains in the ON-state irrespective of V_{in}; as a result, the V_{out} from the inverter remains permanently clamped to 0 V (logic level “0”), as shown in Figure 3f. Once locked, the inverter can only be unlocked by bringing MT₂ back to its original baseline state through the application of a positive V_E.

Figure 4a–c show the optical images, and Figure 4d–f show the corresponding circuit diagrams, for 2D memtransistor-based AND, NAND, and OR gates, respectively. Each circuit consists of two E-mode memtransistors (MT₁ and MT₂) and one D-mode memtransistor (MT₃). Figure 4g–i show the output characteristics of all three logic gates under standard operating conditions, and Figure 4j–l show their corresponding locked states. For an AND gate operating on logical multiplication rule, the output, V_C, will always remain at a low level (logic state “0”) when the input for any one of the E-mode transistors, V_{A/B}, is 0 V, as shown in Figure 4g. This is because MT₃ is highly conductive when either MT₁ or MT₂ is in a low conductive state, clamping V_C to 0 V. In contrast, V_C will only be clamped to V_{DD} = 2 V (logic state “1”) when both MT₁ and MT₂ have V_{A/B} = 2 V, i.e., are in a high conductance state. Thus, to lock the circuit functionality as shown in Figure 4j, we provide a V_p of magnitude 15 V to the local back-gate of MT₁, shifting its V_{TH} to a high positive value (see Supporting Information S2 for the transfer characteristics of MT₁ in unlocked and locked states) and setting it to a high-resistance state. This is equivalent to having an open-circuit condition for MT₁ since it always remains OFF, irrespective of the input provided. As a result, all V_{A/B} combinations for the AND gate provide low V_C values (logic state “0”), thereby locking the circuit.

The LL mechanism of a NAND gate is inverse to that of an AND gate stemming from the fact that a standard NAND

operation is nothing more than inverted AND logic. As shown in Figure 4h, the V_C of the circuit is clamped to V_{DD} = 2 V (logic state “1”) when either or both MT₁ and MT₂ remain nonconductive, i.e., for V_{A/B} = 0 V; only when V_{A/B} is high (logic state “1”) for both MT₁ and MT₂ does V_C = 0 V. To lock the NAND gate, V_E = −14 V is applied to the local back-gates of MT₁ and MT₂ (see Supporting Information S3) since both need to be highly conductive to clamp V_C to 0 V, as shown in Figure 4k.

Next, for an OR gate that operates on the logical addition rule, MT₁ and MT₂ are connected in series with MT₃. As shown in Figure 4i, the V_C of this circuit remains at 0 V (logic state “0”) when V_{A/B} = 0 V (logic state “0”) for both MT₁ and MT₂. When either of the two inputs is high, V_C becomes clamped to V_{DD} (logic state “1”) because one of the two E-mode memtransistors (MT₁ and MT₂) gets connected to MT₃. This circuit can thus be locked by providing a V_p to both MT₁ and MT₂, making them highly resistive (see Supporting Information S4). The locked OR gate is shown in Figure 4l. The original logic functionality can then only be restored by providing an erase pulse, V_E, to both MT₁ and MT₂, as described earlier for the other gates.

Finally, Figure 5a,b, respectively, show the optical image and corresponding circuit schematic for a XOR gate that operates on the exclusive OR rule, i.e., a true output is obtained when the two inputs are dissimilar. Note that the circuit comprises 9 2D memtransistors. The memtransistor pairs MT₁ and MT₂, and MT₅ and MT₆ operate as NOT gates. These NOT gates are employed to invert the bits A and B into $\bar{A}$ and $\bar{B}$, respectively. Next, the inputs A and $\bar{B}$ are applied to the gates of MT₃ and MT₄ whereas $\bar{A}$ and B are applied to the gates of MT₇ and MT₈, respectively. Also note that the series connections of MT₃ and MT₄ and MT₇ and MT₈ are connected in parallel and the entire block is connected in series with MT₉. The overall circuit accomplishes XOR logic for inputs A and B, i.e., $V_C = \bar{A}B + A\bar{B}$, as shown in Figure 5c. V_C = 2 V (logic state “1”) when input logics are different. However, when the input logics are similar, V_C = 0 V (logic state “0”). This circuit can be locked by providing a V_E = −14

Table 1. Resiliency of ISCAS'85 Benchmarks

circuit	number of gates						decamouflaged by SAT (?)
	AND	OR	NAND	NOR	XOR	NOT	
c17	0	0	6	0	0	0	no
c432	31	44	64	19	18	99	no
c499	96	6	0	0	104	40	no
c880	129	96	60	61	0	157	no
c1355	96	6	416	0	0	40	no
c1908	145	125	347	0	0	432	no
c2670	488	129	254	12	0	321	no
c3540	766	205	274	25	0	778	no
c5315	1196	410	454	19	0	607	no
c6288	256	0	0	2128	0	32	no
c7552	1178	386	1028	40	0	922	no

V to both MT_2 and MT_6 , making them highly conductive and thus clamping V_C to 0 V as shown in Figure 5d.

Resilience to SAT-Attack. To evaluate the effectiveness of our proposed approach, we performed LL on the ISCAS'85 benchmark circuits. ISCAS'85 has been traditionally used as a popular benchmark suite to estimate the prowess of different LL techniques. The suite consists of 11 circuits with multi-input, multi-output basic logic gates, the distribution of which is outlined in Table 1. Utilizing our proposed programmable 2D memtransistor devices, we successfully locked all of the AND, OR, NAND, NOR, XOR, and NOT gates in each of the benchmark circuits. Subsequently, a SAT-attack was executed on the benchmark circuits and the corresponding resilience was observed. A SAT-attack utilizes the notion of Boolean satisfiability to compute attack patterns, refining the key space for the circuit in an iterative manner.⁵² Once the SAT-attack was launched on each of the logic-locked circuit, a time limit of 24 h was assigned to the SAT-solver to recover the key values of the circuit. As observed from the results, the solver was unsuccessful in breaking into any of the ISCAS'85 benchmark circuits, which is outlined in the last column of Table 1. This massive resilience to SAT-attack was attributed to the prowess of the programmable 2D memtransistors enabling device-level LL of all of the gates in each of the benchmark circuits. Even the small circuits with a limited number of logic gates were rendered unbreakable to the SAT-solver within the specified time limit. Since the circuits in the ISCAS'85 benchmark demonstrated substantial resilience to SAT-attacks, we restricted ourselves from experimenting with the larger ISCAS'89 benchmark. However, it is highly likely that the ISCAS'89 circuits will also be unbreakable under SAT-attack, owing to the 100% locking enabled by our proposed device-level technique. Hence, the proposed LL scheme with 2D memtransistor devices renders a circuit to be unbreakable under SAT-attacks, thereby bolstering our hypothesis of high resilience against reverse engineering. Supporting Information S5 gives a detailed explanation of the SAT-attack algorithm.

Superiority of 2D-Memtransistor-Based LL over Alternative Approaches. Finally, we benchmark and highlight the superiority of our proposed LL technique against the existing solutions. While LL techniques over the years have primarily focused on providing efficient hardware security solutions by eliminating their vulnerability to several attack models, they have often come at the cost of requiring additional peripheral components. For example, the recently proposed SARlock⁵³ and Anti-SAT⁵⁴ techniques have demonstrated impressive resilience against SAT-attacks.

However, these techniques require integration of comparator/mask blocks and/or multiple XOR/XNOR/multiplexer key gates as peripheral elements to achieve the required resilient obfuscation. In comparison, the proposed LL scheme based on programmable 2D memtransistors eliminates the need of any peripheral components by enabling individual device-level locking of all of the gates in any given circuit. Table 2 compares and summarizes our proposed technique

Table 2. Benchmarking 2D-Memtransistor-Based LL with Existing Alternative Solutions

logic locking technique	mechanism	peripheral components	resilience to SAT-attacks
random logic locking (RLL) ¹³	inserting XOR key gates at random locations	yes	no
fault-based logic locking (FLL) ⁵⁵	inserting XOR key gates at lower testable points	yes	no
strong logic locking (SLL) ⁵⁶	interference-based key-gate insertion	yes	no
SARlock ⁵³	flipping circuit to corrupt input pattern	yes	yes
Anti-SAT ⁵⁴	additional Anti-SAT combination blocks	yes	yes
TT-Lock ⁵⁷	flipping output pattern for a wrong key	yes	yes
2D-memtransistor-based logic locking (this work)	individual device programmability	no	yes

against some of the present state-of-the-art LL solutions in terms of the locking mechanism, requirement of peripheral components and their resilience to SAT-attacks.

CONCLUSIONS

In conclusion, we have experimentally demonstrated a new technique of locking basic digital logic designs (AND, NAND, OR, XOR, and NOT gates) composed of programmable monolayer MoS_2 memtransistors. This programmability is attributed to charge trapping and detrapping in the local back-gate oxide and/or at the Al_2O_3/MoS_2 interface and offers excellent retention properties. The circuits are locked/unlocked through the application of either a programming pulse V_P or an erase pulse V_E to the local back-gates of their constituent memtransistors at a miniscule energy expenditure of <1 pJ. Moreover, our LL solution when implemented on all of the ISCAS'85 benchmark circuits is demonstrated to be

highly resilient to SAT-attack models and is superior to other alternative solutions by eliminating the requirement of involving any additional peripheral components. Our approach of harnessing material properties and device phenomena at the nanoscale architecture can offer attractive solutions for solving critical hardware security problems, such as IP overbuilding and piracy, that stem from the globalized and interconnected nature of today's semiconductor supply chain system and resource-constrained edge devices.

METHODS

Large-Area Monolayer MoS₂ Film Growth. Metal-organic chemical vapor deposition (MOCVD) was used to deposit a monolayer of MoS₂ on an epi ready 2'' c-sapphire substrate. In order to accomplish a uniform monolayer growth of the film, a cold-wall horizontal reactor with an inductively heated graphite susceptor and wafer rotation was used. Molybdenum hexacarbonyl Mo(CO)₆ and hydrogen sulfide (H₂S) were used as the precursors. Mo(CO)₆ was used to deliver 1.1×10^{-3} sccm of metal precursor at 10 °C and 650 Torr in a stainless-steel bubbler, while 400 sccm of H₂S was employed for the same procedure. The monolayer film growth was achieved in 18 min in an H₂ ambient at 950 °C and 50 Torr. Prior to the growth initialization, the substrate was first heated to 1000 °C in H₂ for a total of 10 mins. Post MoS₂ growth, the substrate was cooled to 300 °C in H₂S in order to halt any further decomposition of the film. These details can also be found in our earlier works.⁵⁸

Fabrication of Local Back-Gate Islands. The 285 nm SiO₂ on p⁺⁺-Si substrate was first spin-coated with two different photoresists: 1) A Lift-Off-Resist (LOR 5A) and 2) a Series Photoresist (SPR 3012) which were baked at 185 °C and 95 °C, respectively. This bilayer resist was subsequently patterned using a Heidelberg Maskless Aligner (MLA 150) for defining the local back-gate islands followed by a developing process step in MF CD26 microposit culminating with a final deionized (DI) water rinse. The 20/50 nm TiN/Pt back-gate electrodes were then deposited with a reactive sputtering technique. Using acetone and Photo Resist Stripper (PRS 3000), the photoresist was removed and cleaned with a 2-propanol (IPA) solution with a final DI water rinse. Next, a 50 nm Al₂O₃ layer was grown as the back-gate dielectric over the entire substrate using atomic layer deposition (ALD). Next, in order to access the individual local back-gate electrodes, etch patterns were defined along two sides of each island using the same bilayer photoresist combination and an MLA exposure processes previously described. The Al₂O₃ was subsequently dry-etched in the exposed regions using a BCl₃ reactive ion etch (RIE) chemistry at 5 °C for 80 s. The RIE process was conducted in four cycles of 20 s with a short cooldown period between each cycle in order to minimize any unwanted heating in the substrate and ensuring a uniform/controlled etch rate. The photoresist was subsequently removed to access the individual local back-gate electrodes using the previously discussed resist stripping process.

MoS₂ Film Transfer to Local Back-Gate Islands. The MOCVD-grown monolayer MoS₂ film was first transferred from the sapphire growth substrate to the SiO₂/p⁺⁺-Si application substrate consisting of the local back-gate islands to build the 2D memtransistors. To accomplish this, a (PMMA)-assisted wet transfer process was employed where, the as-grown MoS₂ film on the sapphire substrate was first spin-coated with poly(methyl-methacrylate) or PMMA and left to sit for 24 h in order to ensure good PMMA/MoS₂ adhesion. Next, using a razor blade the corners of this spin-coated film were scratched followed by an immersion in a 2 M NaOH solution at 90 °C. Capillary action causes NaOH to be selectively drawn toward the substrate/MoS₂ interface, due to the hydrophilic nature of sapphire and hydrophobic nature of MoS₂ and PMMA. This separates the PMMA/MoS₂ stack from the sapphire substrate. The separated film is then fished out from the NaOH solution using a clean glass slide which is rinsed in three separate water baths for a total of 15 min each before the final transfer onto the application substrate. Finally, to remove the moisture and promote film adhesion to ensure a pristine

interface the substrate was baked at 50 °C and 70 °C for 10 min each. The PMMA was subsequently removed using acetone and the film was cleaned using an IPA solution.

Fabrication of 2D Memtransistors. To define the channel regions of the MoS₂ memtransistors discussed in this work, the application substrate, with the MoS₂ substrate was first spin-coated with PMMA and baked at 180 °C for 90 s. Using an electron beam (e-beam) lithography, the resist was then exposed and subsequently developed with a 1:1 mixture of 4-methyl-2-pentanone (MIBK) and IPA for a total time of 60s and 45s, respectively. Subsequently etching of the exposed monolayer film was carried out using a sulfur hexafluoride (SF₆) RIE at 5 °C for 30 s. This was followed by rinsing of the sample in acetone and IPA in order to remove the developed e-beam resist. For defining the source and drain contacts pads, the sample was again spin-coated with methyl methacrylate (MMA) and A3 PMMA resist followed by a second round of E-beam lithography with a similar resist development process step as previously stated. Nickel (Ni, 40 nm) and gold (Au, 30 nm) were deposited as contact pads using a Temescal E-beam evaporation tool to form the source and the drain electrodes. Finally, in order to remove the excess evaporated Ni/Au a lift-off procedure was performed by immersing the sample in acetone for 30 min followed by IPA for another 30 min.

Multidevice Integration. To define the connections between respective memtransistors, the same resist, e-beam lithography, and development processes were used as discussed previously. E-beam evaporation was used to deposit 60 nm Ni and 30 nm Au to serve as the interconnect metals. The greater thicknesses compared to the source/drain contacts were due to the need for a conformal coating of metal over/along the sidewalls formed in previous processing. Finally, the e-beam resist was rinsed away via a lift-off process using acetone and IPA.

Electrical Characterization. Electrical characterization of the fabricated devices was performed in a Lake Shore CRX-VF probe station under atmospheric conditions using a Keysight B1500A parameter analyzer.

Data Availability. The datasets generated during and/or analyzed during the current study are available from the corresponding author upon reasonable request.

Code Availability. The codes used for plotting the data are available from the corresponding authors upon reasonable request.

ASSOCIATED CONTENT

Supporting Information

The Supporting Information is available free of charge at <https://pubs.acs.org/doi/10.1021/acsanm.2c02807>.

Band diagram describing the underlying mechanism of charge trapping and detrapping at the 2D channel/dielectric interface; transfer characteristics of enhancement mode memtransistor for AND gate for pre- and post-erase voltage pulse application; transfer characteristics of enhancement mode memtransistors MT₁ and MT₂ for NAND gate for pre- and post-programming voltage pulse application; transfer characteristics of enhancement mode memtransistors MT₁ and MT₂ for OR gate for pre- and post-erase voltage pulse application; and description of SAT-Attack algorithm along with a flowchart (PDF)

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Notes

The authors declare no competing financial interest.

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REFERENCES

- (1) Force, T. *High Performance Microchip Supply*, Annual Report; Defense Technical Information Center (DTIC): USA; 2005.
- (2) Rostami, M.; Koushanfar, F.; Karri, R. A primer on hardware security: Models, methods, and metrics. *Proc. IEEE* **2014**, *102*, 1283–1295.
- (3) Torrance, R.; James, D. In *The State-of-the-Art in Semiconductor Reverse Engineering*, Proceedings of the 48th Design Automation Conference, 2011; pp 333–338.
- (4) James, R. Intel's 22-nm Trigate Transistors Exposed, Chipworks Real Chips Blog, 2012. http://www.electroiq.com/blogs/chipworks_real_chips_blog/2012/04/intel-s-22-nm-trigate-transistors-exposed.html.
- (5) Oriero, E.; Hasan, S. R. Survey on recent counterfeit IC detection techniques and future research directions. *Integration*. **2019**, *66*, 135–152.
- (6) Tehranipoor, M.; Wang, C. *Introduction to Hardware Security and Trust*; Springer Science & Business Media, 2011.
- (7) Sethumadhavan, S.; Waksman, A.; Suozzo, M.; Huang, Y.; Eum, J. Trustworthy hardware from untrusted components. *Commun. ACM* **2015**, *58*, 60–71.
- (8) Inquiry into Counterfeit Electronic Parts in the Department of Defense Supply Chain. Washington DC. 2012, Available: <https://www.armed-services.senate.gov/download/inquiry-into-counterfeit-electronic-parts-in-the-department-of-defense-supply-chain> (accessed May 20, 2022).
- (9) Yasin, M.; Rajendran, J. J.; Sinanoglu, O.; Karri, R. In *On improving the security of logic locking*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2016; pp 1411–1424.
- (10) Rajendran, J.; Sam, M.; O Sinanoglu, O.; Karri, R. In *Security Analysis of Integrated Circuit Camouflaging*, Proceedings of the 2013 ACM SIGSAC conference on Computer & communications security, 2013; pp 709–720.
- (11) Jarvis, R. W.; McIntyre, M. G. Split Manufacturing Method for Advanced Semiconductor Circuits. U.S. Patent US7,195,931, 2007.
- (12) Alkabani, Y.; Koushanfar, F. In *Active Hardware Metering for Intellectual Property Protection and Security*, USENIX security symposium, 2007; pp 1–20.
- (13) Roy, J. A.; Koushanfar, F.; I L Markov, I. L. Ending piracy of integrated circuits. *Computer* **2010**, *43*, 30–38.
- (14) Dupuis, S.; Ba, P.-S.; Di Natale, G.; Flottes, M.-L.; Rouzeyre, B. In *A Novel hardware Logic Encryption Technique for Thwarting Illegal Overproduction and Hardware Trojans*, IEEE 20th International On-Line Testing Symposium (IOLTS), 2014; pp 49–54.
- (15) Chakraborty, R. S.; Bhunia, S. In *HARPOON: An Obfuscation-Based SoC Design Methodology for Hardware Protection*, IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems, 2009; pp 1493–1502.
- (16) Chakraborty, R. S.; Bhunia, S. In *Security against Hardware Trojan through a Novel Application of Design Obfuscation*, IEEE/ACM International Conference on Computer-Aided Design-Digest of Technical Papers, 2009; pp 113–116.
- (17) Jiang, H.; Li, C.; Zhang, R.; Yan, P.; Lin, P.; Li, Y.; Yang, J. J.; Holcomb, D.; Xia, Q. A provable key destruction scheme based on memristive crossbar arrays. *Nat. Electron.* **2018**, *1*, 548–554.
- (18) Hoefflinger, B. ITRS: The international technology roadmap for semiconductors. *Chips* **2011**, *2020*, 161–174.
- (19) Das, S.; Sebastian, A.; Pop, E.; McClellan, C. J.; Franklin, A. D.; Grasser, T.; Knobloch, T.; Illarionov, Y.; Penumatcha, A. V.; Appenzeller, J.; Chen, Z.; Zhu, W.; Asselberghs, L.; Li, L. J.; Avci, U. E.; Bhat, N.; Anthopoulos, T. D.; Singh, R. Transistors based on two-dimensional materials for future integrated circuits. *Nat. Electron.* **2021**, *4*, 786–799.
- (20) Wang, J.; Lundstrom, M. In *Does source-to-drain tunneling limit the ultimate scaling of MOSFETs?*, International Electron Devices Meeting, 2002; pp 707–710.
- (21) Lin, Y. F.; Xu, Y.; Wang, S. T.; Li, S. L.; Yamamoto, M.; Aparecido-Ferreira, A.; Li, W.; Sun, H.; Nakaharai, S.; Jian, W. B.; Ueno, K.; Tsukagoshi, K. Ambipolar MoTe₂ transistors and their applications in logic circuits. *Adv. Mater.* **2014**, *26*, 3263–3269.
- (22) Shen, P.-C.; Su, C.; Lin, Y.; Chou, A.-S.; Cheng, C.-C.; Park, J.-H.; Chiu, M.-H.; Lu, A.-Y.; Tang, H.-L.; Tavakoli, M. M.; Pitner, G.; Ji, X.; Cai, Z.; Mao, N.; Wang, J.; Tung, V.; Li, J.; Bokor, J.; Zettl, A.; Wu, C.-I.; Palacios, T.; Li, L.-J.; Kong, J. Ultralow contact resistance between semimetal and monolayer semiconductors. *Nature* **2021**, *593*, 211–217.
- (23) English, C. D.; Smithe, K. K. H.; Xu, R. L.; Pop, E. In *Approaching Ballistic Transport in Monolayer MoS₂ Transistors with Self-Aligned 10 nm Top Gates*, IEEE International Electron Devices Meeting (IEDM), 2016; pp 561–564.
- (24) Price, K. M.; Schauble, K. E.; McGuire, F. A.; Farmer, D. B.; Franklin, A. D. Uniform Growth of Sub-5-Nanometer High-κ Dielectrics on MoS₂ Using Plasma-Enhanced Atomic Layer Deposition. *ACS Appl. Mater. Interfaces* **2017**, *9*, 23072–23080.
- (25) Sebastian, A.; Pendurthi, R.; Choudhury, T. H.; Redwing, J. M.; Das, S. Benchmarking monolayer MoS₂ and WS₂ field-effect transistors. *Nat. Commun.* **2021**, *12*, No. 693.
- (26) Zhu, K.; Wen, C.; Aljarb, A. A.; Xue, F.; Xu, X.; Tung, V.; Zhang, X.; Alshareef, H. N.; Lanza, M. The development of integrated circuits based on two-dimensional materials. *Nat. Electron.* **2021**, *4*, 775–785.
- (27) Wachter, S.; Polyushkin, D. K.; Bethge, O.; Mueller, T. A microprocessor based on a two-dimensional semiconductor. *Nat. Commun.* **2017**, *8*, No. 14948.
- (28) Polyushkin, D. K.; Wachter, S.; Mennel, L.; Paur, M.; Paliy, M.; Iannaccone, G.; Fiori, G.; Neumaier, D.; Canto, B.; Mueller, T.

Analogue two-dimensional semiconductor electronics. *Nat. Electron.* **2020**, *3*, 486–491.

(29) Sebastian, A.; Pannone, A.; Subbulakshmi Radhakrishnan, S.; Das, S. Gaussian synapses for probabilistic neural networks. *Nat. Commun.* **2019**, *10*, No. 4199.

(30) Subbulakshmi Radhakrishnan, S.; Sebastian, A.; Oberoi, A.; Das, S.; Das, S. A biomimetic neural encoder for spiking neural network. *Nat. Commun.* **2021**, *12*, No. 2143.

(31) Jayachandran, D.; Oberoi, A.; Sebastian, A.; Choudhury, T. H.; Shankar, B.; Redwing, J. M.; S Das, S. A low-power biomimetic collision detector based on an in-memory molybdenum disulfide photodetector. *Nat. Electron.* **2020**, *3*, 646–655.

(32) Schranghamer, T. F.; Oberoi, A.; Das, S. Graphene memristive synapses for high precision neuromorphic computing. *Nat. Commun.* **2020**, *11*, No. 5474.

(33) Das, S.; Dodda, A.; Das, S. A biomimetic 2D transistor for audiomorphic computing. *Nat. Commun.* **2019**, *10*, No. 3450.

(34) Radisavljevic, B.; Whitwick, M. B.; Kis, A. Integrated circuits and logic operations based on single-layer MoS₂. *ACS Nano* **2011**, *5*, 9934–9938.

(35) Radisavljevic, B.; Whitwick, M. B.; Kis, A. Small-signal amplifier based on single-layer MoS₂. *Appl. Phys. Lett.* **2012**, *101*, No. 043103.

(36) Wang, H.; Yu, L.; Lee, Y.-H.; Shi, Y.; Hsu, A.; Chin, M. L.; Li, L.-J.; Dubey, M.; Kong, J.; Palacios, T. Integrated circuits based on bilayer MoS₂ transistors. *Nano letters.* **2012**, *12*, 4674–4680.

(37) Sanne, A.; Ghosh, R.; Rai, A.; Yogeesh, M. N.; Shin, S. H.; Sharma, A.; Jarvis, K.; Mathew, L.; Rao, R.; Akinwande, D.; Banerjee, S. Radio frequency transistors and circuits based on CVD MoS₂. *Nano Lett.* **2015**, *15*, 5039–5045.

(38) Wang, L.; Chen, L.; Wong, S. L.; Huang, X.; Liao, W.; Zhu, C.; Lim, Y. F.; Li, D.; Liu, Z.; Chi, D.; Ang, K.-W. Electronic devices and circuits based on wafer-scale polycrystalline monolayer MoS₂ by chemical vapor deposition. *Adv. Electron. Mater.* **2019**, *5*, No. 1900393.

(39) Lembke, D.; Bertolazzi, S.; Kis, A. Single-layer MoS₂ electronics. *Acc. Chem. Res.* **2015**, *48*, 100–110.

(40) Amani, M.; Burke, R. A.; Proie, R. M.; Dubey, M. Flexible integrated circuits and multifunctional electronics based on single atomic layers of MoS₂ and graphene. *Nanotechnology* **2015**, *26*, No. 115202.

(41) Gao, L.; Liao, Q.; Zhang, X.; Liu, X.; Gu, L.; Liu, B.; Du, J.; Ou, Y.; Xiao, J.; Kang, Z.; Zhang, Z.; Zhang, Y. Defect-engineered atomically thin MoS₂ homogeneous electronics for logic inverters. *Adv. Mater.* **2020**, *32*, No. 1906646.

(42) Liu, X.; Islam, A.; Yang, N.; Odhner, B.; Tupta, M. A.; Guo, J.; Feng, P.X.-L. Atomic Layer MoTe₂ Field-Effect Transistors and Monolithic Logic Circuits Configured by Scanning Laser Annealing. *ACS Nano* **2021**, *15*, 19733–19742.

(43) Oberoi, A.; Dodda, A.; Liu, H.; Terrones, M.; Das, S. Secure Electronics Enabled by Atomically Thin and Photosensitive Two-Dimensional Memtransistors. *ACS Nano* **2021**, *15*, 19815–19827.

(44) Wali, A.; Kundu, S.; Arnold, A. J.; Zhao, G.; Basu, K.; Das, S. Satisfiability attack-resistant camouflaged two-dimensional heterostructure devices. *ACS Nano* **2021**, *15*, 3453–3467.

(45) Wu, P.; Reis, D.; Hu, X. S.; Appenzeller, J. Two-dimensional transistors with reconfigurable polarities for secure circuits. *Nat. Electron.* **2021**, *4*, 45–53.

(46) Wali, A.; Ravichandran, H.; Das, S. A Machine Learning Attack Resilient True Random Number Generator Based on Stochastic Programming of Atomically Thin Transistors. *ACS Nano* **2021**, *15*, 17804–17812.

(47) Dodda, A.; Subbulakshmi Radhakrishnan, S.; Schranghamer, T. F.; Buzzell, D.; Sengupta, P.; Das, S. Graphene-based physically unclonable functions that are reconfigurable and resilient to machine learning attacks. *Nat. Electron.* **2021**, *4*, 364–374.

(48) Feng, G.; Jiang, J.; Zhao, Y.; Wang, S.; Liu, B.; Yin, K.; Niu, D.; Niu, D.; Li, X.; Li, X.; Chen, Y.; Chen, Y.; Duan, H.; Duan, H.; Yang, J.; Yang, J.; He, J.; He, J.; Gao, Y.; Gao, Y.; Wan, Q. A sub-10 nm vertical organic/inorganic hybrid transistor for pain-perceptual and

sensitization-regulated nociceptor emulation. *Adv. Mater.* **2020**, *32*, No. 1906171.

(49) Xie, D.; Wei, L.; Xie, M.; Jiang, L.; Yang, J.; He, J.; Jiang, J. Photoelectric visual adaptation based on 0D-CsPbBr₃-quantum-dots/2D-MoS₂ mixed-dimensional heterojunction transistor. *Adv. Funct. Mater.* **2010**, *31*, No. 2010655.

(50) Das, S.; Chen, H. Y.; Penumatcha, A. V.; Appenzeller, J. High performance multilayer MoS₂ transistors with scandium contacts. *Nano Lett.* **2013**, *13*, 100–105.

(51) Sebastian, A.; Das, S.; Das, S. An Annealing Accelerator for Ising Spin Systems Based on In-Memory Complementary 2D FETs. *Adv. Mater.* **2022**, *34*, No. 2107076.

(52) Subramanyan, P.; Ray, S.; Malik, S. In *Evaluating the Security of Logic Encryption Algorithms*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2015; pp 137–143.

(53) Yasin, M.; Mazumdar, B.; Rajendran, J. J.; Sinanoglu, O. In *SARLock: SAT Attack Resistant Logic Locking*, IEEE International Symposium on Hardware Oriented Security and Trust (HOST), 2016; pp 236–241.

(54) Xie, Y.; Srivastava, A. In *Mitigating SAT Attack on Logic Locking*, International Conference on Cryptographic Hardware and Embedded Systems, 2016; pp 127–146.

(55) Rajendran, J.; Zhang, H.; Zhang, C.; Rose, G. S.; Pino, Y.; Sinanoglu, O.; Karri, R. Fault analysis-based logic encryption. *IEEE Trans. Comput.* **2015**, *64*, 410–424.

(56) Rajendran, J.; Pino, Y.; Sinanoglu, O.; Karri, R. In *Security Analysis of Logic Obfuscation*, Proceedings of the 49th Annual Design Automation Conference, 2012; pp 83–89.

(57) Yasin, M.; Sengupta, A.; Schafer, B. C.; Makris, Y.; Sinanoglu, O.; Rajendran, J. et al. *What to Lock? Functional and Parametric Locking*, Proceedings of the on Great Lakes Symposium on VLSI 2017, 2017; pp 351–356.

(58) Xuan, Y.; Jain, A.; Zafar, S.; Lotfi, R.; Nayir, N.; Wang, Y.; Choudhury, T. H.; Wright, S.; Feraca, J.; Rosenbaum, L.; Redwing, J. M.; Crespi, V.; Duin, A. C. T. V. Multi-scale modeling of gas-phase reactions in metal-organic chemical vapor deposition growth of WSe₂. *J. Cryst. Growth* **2019**, *527*, No. 125247.